TM 11-7010-200-34-2

TECHNICAL MANUAL

MAINTENANCE INSTRUCTIONS

IS/1000
HIGH CAPACITY MAGNETIC
DISK CONTROLLER, TYPE
OL-169/UYQ( )

HEADQUARTERS, DEPARTMENT OF THE ARMY

NOVEMBER 1979

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NG: NONE

USAR: NONE

For explanation of abbreviations see, AR 310-50.

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SECTION 1
INTRODUCTION

1.1 PURPOSE

This technical manual provides the information necessary for maintenance, servicing and repair of the High Capacity Magnetic Disk Controller.

1.2 SCOPE

The information given in this manual provides the following:

- A brief functional description of the hardware.
- Preventive maintenance procedures to be performed periodically.
- Corrective maintenance procedures.
- Reference information pertinent to field maintenance.

The information in this manual is presented with the assumption that the user is thoroughly familiar with solid state logic, standard test equipment, and is skilled in common maintenance procedures and troubleshooting techniques. In addition, the user should be familiar with the maintenance documentation shipped with the GTE/IS system.

The scope of this manual is limited to correction of mechanical faults, isolation of faults to the assembly level and correction of faults to the extent of replacing the assembly. Not covered in this manual are repair, system planning and engineering.

1.3 DOCUMENTATION

The following paragraphs define the publications and conventions that support this manual.

1.3.1 Publications

- A0003 IS/1000 Maintenance Manual.
- E0006 IS/1000 User's Manual.
- H0011 IS/1000 I/O Interface Reference Manual.
- Manuals supplied with vendor-furnished equipment.

1.3.2 Abbreviations and Conventions

Table 1-1 defines abbreviations found in this publication.

The following conventions are observed throughout the text:

- The $-sign preceding a number signifies that it is in hexadecimal notation.

Table 1-1. Abbreviations (Sheet 1 of 2)

Abbreviations	Meaning
A	Ampere.
ac	Alternating current.
bpi	Bits per inch.
bps	Bits per second.
CPU	IS/1000 Central Processing Unit.
CR	Carriage return.
CRC	Cyclic redundancy check.
CRCC	Cyclic redundancy check character.
CROM	Control Read Only Memory.
DA	Direct Access
DMA	Direct memory access.
DROM	Decode read only memory
EDF	Execute Device Function.
FF	Flip-flop.
GTE/IS	General Telephone and Electronics Information Systems, Inc.
HSPT	High-speed paper tape.
Hz	Hertz.
IC	Integrated circuit.
I/O	Input/Output
IOA	Interface (Input/Output) Assembly.
DCI	Disk Controller Interface.
IOL	Interface (Input/Output) Logic
kHz	Kilohertz.
LSB	Least-significant bit.
LSI	Large Scale Integration.
ma	Milliampere.
MDC	Magnetic Disk Controller.
MDS	Magnetic Disk System.

Table 1-1. Abbreviations (Sheet 2 of 2)

Abbreviations	Meaning
MHz	Megahertz.
mil	0.001 inch.
MSB	Most-significant bit.
MSI	Medium Scale Integration.
MUX	Multiplex
mv	Millivolt.
ns	Nanosecond.
op code	Operation code.
PC	Printed circuit.
PDC	Programmable Device Controller.
PDP	Power Distribution Panel.
pf	Picofarad.
PLO	Phase Locked Oscillator.
PROM	Programmable Read Only Memory.
PSQ	Power Sequencer.
RAM	Random Access Memory.
ROM	Read Only Memory.
SMX	Simplex.
SSI	Small Scale Integration.
Sync	Synchronization.
tpi	Tracks per inch.
TTL	Transistor-Transistor-Logic.
TTY	Teleprinter.
us	Microsecond.
Vac	Volts, alternating current.
Vdc	Volts, direct current.
VFO	Variable frequency oscillator.

- The names of instructions are capitalized for easy identification.
- Signal mnemonics that appear on logic diagrams and panel nomenclature are reproduced in all upper-case characters.
- TELEPRINTER MESSAGES ARE REPRODUCED IN 1430 TYPE STYLE, AS SHOWN IN THIS EXAMPLE.
- ONE and ZERO are used in text to denote binary 1 and binary 0 bit conditions, respectively.
- Values represented in teleprinter messages by letters are reproduced in scribe type style, as shown in this example.

SECTION 2
DESCRIPTION

2.1 GENERAL

This section presents a physical description, a functional description and the theory of operation of the magnetic disk controller. The disk drive itself is covered only to the extent required for a complete understanding of the controller and where necessary to explain general principles and concepts of magnetic disk data storage. The description and theory of operation are preceded by an introduction to magnetic disk storage principles. The Functional Blocks part of the functional description defines the major logic blocks of the disk controller. The Software part of the functional description lists and defines all program instructions accepted by the disk controller, as well as the operation control word codes enabling the disk controller to transfer information between the processor memory and the disk drive.

2.2 MAGNETIC DISK STORAGE PRINCIPLES

The following explanatory discussion is meant to cover the main principles, concepts and terminology relative to magnetic disk data storage in general. In the interest of concision however, concepts with a broad range of diverse applications are covered to highlight only that aspect which is pertinent to its GTE/IS application.

2.2.1 Magnetic Disk Subsystem

The GTE/IS Magnetic Disk subsystem provides high performance, high-capacity auxiliary data storage for the IS/1000 processor. The GTE/IS Magnetic Disk subsystem expands the on-line storage capacity of the IS/1000 by up to 360 million bytes. Its ability for fast, direct access to specific areas of the storage medium, enables high speed data storage and retrieval operations, making it ideally suited for real-time and/or time-sharing data processing applications.

The magnetic disk subsystem consists of a controller and from one to eight model 114 or from one to four model 215 disk drives. The storage and recovery of data by the magnetic disk subsystem, is accomplished through the recording of information on, and retrieval of information from, an IBM 2315 type disk pack or a GTE/IS approved equivalent. The disk drive contains the rotational drive, access mechanism and read/write components and circuitry to record data on, and reproduce data from, the disk pack. The controller receives commands from the IS/1000 processor, and interprets them to initiate operations with the disk drives in the subsystem. Data is transferred between the processor and disk drive using the DMA option. The controller provides data buffering to relieve the processor of stringent timing requirements. The controller also provides the processor with the status of the controller and that of all the attached disk drives in the magnetic disk subsystem.

2.2.2 Storage Medium

The storage medium used in the model 114 and the model 215 is an IBM 2316 type disk pack. The disk pack consists of eleven disks, each 14 inches in diameter and made of aluminum with a magnetic coating on both sides. The disks are stacked 0.35 of an inch apart on a vertical hub, with protective disks mounted immediately above the top and below the bottom disks. It is therefore not possible to use the top surface of the upper disk nor the bottom surface of the lower disk for data storage. Hence, the disk pack contains twenty usable recording surfaces. The bottom protective disk is slightly larger in diameter and has one index slot machined in its periphery.

The entire disk pack weighs approximately fifteen pounds and is, when removed from the drive, enclosed in dust covers for off-line storage.

2.2.3 Data Recording

2.2.3.1 Recording Mode

Data is recorded in NRZ (non-return-to-zero), double frequency, bit-serial mode. In this mode, a doubling of the frequency indicates a ONE while no frequency doubling signifies a ZERO.

2.2.3.2 Recording Format

The format according to which data is recorded on the disk is determined by the programming of the controller. In GTE/IS applications, this is in the form of records of single-sector length. Proper formatting of the data is enabled and monitored through the index notch in the protective bottom cover disk of the disk pack. When the disk pack rotates, the index slot is sensed by an electro-magnetic transducer which translates each slot passage into an electrical pulse. The train of consecutive pulses, enables the controller to format the data, determines the rotational speed of the disk pack, and signals the beginning and subsequent ending of all recording tracks at each complete revolution of the disk pack. In the GTE/IS Magnetic Disk subsystem, the Index Mark is used to start the recording of data on the disks in the form of sixteen, sector length records, with each record containing 346 bytes.

2.2.3.3 Recording Density

Data is recorded at an overall bit density of approximately 2,200 bpi, i.e., 1,100 clock bits and a possible maximum of 1,100 data bits per inch on the innermost track. Recording density for the outermost track is about 1,530 bpi, i.e., 765 clock bits and a possible maximum of 765 data bits per inch.

2.2.3.4 Recording Capacity

The recording capacity of an IBM 2316 type disk pack, when used in a model 114 disk drive, is 22,476,160 bytes, with each byte having eight data bits. The recording capacity of the same disk

pack, when used in a model 215 disk drive, is approximately 44,952,320 bytes, due to the fact that the model 215 can establish twice as many cylinders in the same disk pack.

The recording capacities per track and per cylinder are the same, i.e., 5,536 bytes and 110,720 bytes respectively, for both model disk drives.

2.2.4 Data Addressing

To be able to locate the exact same area on the disk pack repeatedly, each area on the disk pack must be made unique. This is accomplished by adopting an imaginary cylinder concept and assigning a horizontal and a vertical addressing scheme to it.

2.2.4.1 Vertical Addressing

The IBM 2316 type disk pack has twenty recording surfaces. Vertical addressing is accomplished by assigning the numbers 00 through 19 to each of the twenty disk surfaces, in consecutive order, from top to bottom. (Figure 2-1).

2.2.4.2 Horizontal Addressing

Horizontal addressing in the model 114 is accomplished by assigning the numbers 000 through 202, to 203 concentric circles on each disk surface. The concentric circles, .01 inch apart, form the centers of 203 seven mil wide recording tracks.

Horizontal addressing in the model 215 is accomplished by assigning the numbers 000 through 405, to 406 concentric circles on each disk surface. The concentric circles, .005 inch apart, form the centers of 406 four mil wide recording tracks.

In both model disk drives, the outermost cylindrical track, numbered 000, is approximately 13 inches in diameter, the innermost cylindrical track, numbered 202 or 405, is approximately 9 inches in diameter.

2.2.4.3 Cylinder Concept

Twenty recording tracks having the same horizontal address designation, lie in the same circular, vertical plane, and can therefore be thought of as a cylinder containing twenty vertically aligned tracks. Hence, it is possible to address data in any track within any cylinder by positioning the heads at that particular cylinder and selecting the head associated with the desired track. A total of 203 cylinders is available in each disk pack when used in a model 114 disk drive, and 406 cylinders are available in a disk pack when used in a model 215 disk drive.

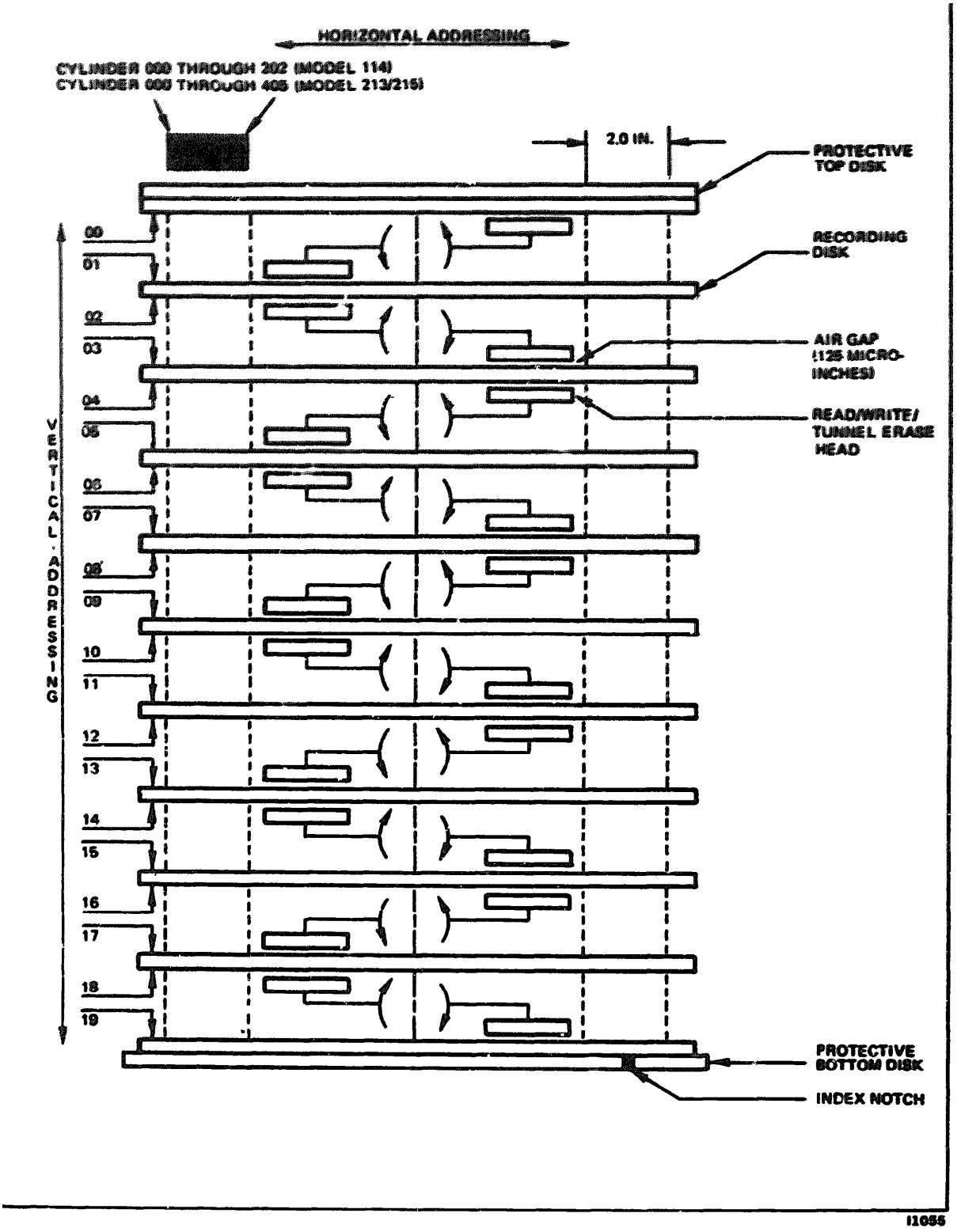


Figure 2-1. Disk Storage Addressing and Cylinder Concept

2.2.4.4 Data Access

Every area on the disk pack can be accessed through the combined, straight line travel of the read/write heads radially across the disk surfaces, and the rotational motion of the disks. Any track can be accessed specifying a cylinder address and a head address. Any sector in a track can be accessed by specifying the sector address.

2.2.5 Basic Operations

The purpose of the magnetic disk subsystem is to store information on the disk pack and to recover this same information when needed at a later time. To enable the recovery of the stored data, the subsystem must be able to:

1. Control precisely where on the disk pack the information is to be recorded.

2. Return to the exact same location on the disk pack for recovery of the recorded information.

The three basic operations of the subsystem therefore are:

1. Seek.

2. Write.

3. Read.

Although there are many commands used in conjunction with the magnetic disk subsystem, each command causes the subsystem to execute one or more or a combination of these three operations.

2.2.6 Head Positioning

Positioning of the read/write heads in the disk pack is enabled by the rotational velocity of the disks in combination with the aerodynamic properties of the head pads. The resultant physical effect is a high density air layer of about 125 microinches, which functions as an air bearing for the head pad to ride on. Each head pad is connected to a head mounting arm. Twenty such head assemblies are mounted to a movable head stack carriage, with the read/write gaps in accurate vertical alignment (Figure 2-1). An electromagnetic servocontrolled linear motor moves the carriage to position the heads at any of the 203 cylinders in the model 114, or any of the 406 cylinders in the models 213 and 215.

The heads are designated according to the corresponding disk surfaces, i.e., head 00 is opposite recording surface 00, head 01 is opposite recording surface 01, etc. After the heads have been positioned at the desired cylinder, the head carriage is held in place through electronic control by detecting any positional deviation of the heads and counteracting it electrically.

2.2.7 Cylinder Detection

During the head positioning process the travel of the heads must be monitored. Every time the heads cross a cylinder, this is registered, and the end result is then communicated to the controller. When the cylinder address has been decremented to ZERO the heads have reached the desired cylinder.

Cylinder detection in the model 114 is accomplished through a stationary vari_ble-reluctance transducer, that senses the passing of a teethed rack attached to the moving head carriage (Figure 2-2, detail B). Each tooth on the rack corresponds to a specific cylinder. Thus, the number of teeth passing the transducer translates into the number of cylinders crossed by the heads.

In models 213 and 215, cylinder detection is accomplished opto-electrically by sensing an opaque scale, coded with transparent slots. (Figure 2-2, detail B).

2.2.8 Index Mark and Rotational Speed Detection

As the disk pack rotates, a variable reluctance transducer senses the index notch in the protective bottom disk of the disk pack. The transducer generates a pulse at the detection of each notch (Figure 2-2, detail A). The index pulse is used by the controller as a homing pulse, i.e., it indicates the beginning and subsequent ending of all the tracks in the disk pack.

In addition, the index pulse is used by the disk drive itself to monitor the rotational velocity of the disk pack, which is 2,400 rpm. Attainment and maintenance of this rotational speed is extremely important in maintaining correct bit densities in the tracks. Also, when the rotational velocity of the disk pack is too low, the air bearing between the head pads and the rotating disk surfaces would collapse causing the heads to crash into the disks. Therefore, the heads are not introduced into the disk pack until the disk pack has attained 70 percent of its operational rotational speed. An emergency head retract operation is initiated when the rotational speed drops below 70 percent.

2.2.9 Data Organization

The data organization used in the IS/1000 magnetic disk subsystem is fixed record length, IBM compatible format. This formats the disk pack as shown hereunder.

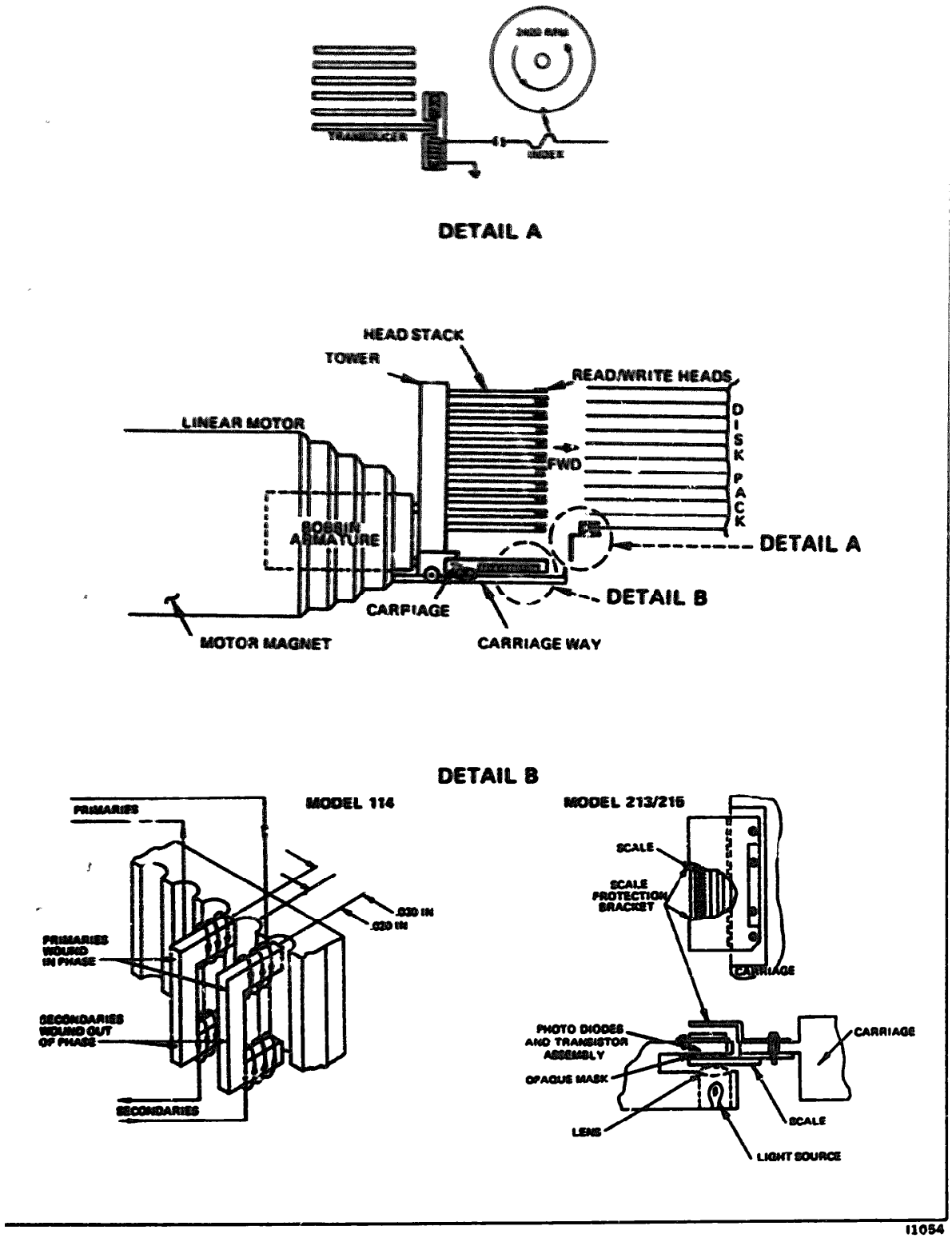


Figure 2-2. Head Positioning, Cylinder, Index, Sector and Speed Detection

Model 114 Disk Drive	
Cylinders per disk pack	203
Tracks per cylinder	20
Records per track	16
Bytes per record	346
Bytes per track	5,536
Bytes per cylinder	110,720
Bytes per disk pack	22,476,160

Models 213 and 215 Disk Drives	
Cylinders per disk pack	406
Tracks per cylinder	20
Records per track	16
Bytes per record	346
Bytes per track	5,536
Bytes per cylinder	110,720
Bytes per disk pack	44,952,320

2.3 PHYSICAL DESCRIPTION

The Magnetic Disk Controller (MDC), shown in Figure 2-3, comprises the following:

- Programmable Device Controller board.
- Disk Controller Interface board.
- Interface Assembly.
- AC Power Distribution Panel.

2.3.1 Programmable Device Controller

The programmable device controller (PDC) board, shown in Figure 2-4, is a standard IS/1000 printed circuit board. The programmable device controller logic is implemented through approximately 125 bipolar ICs of the 7400 series, and is mostly MSI technology. The PDC board is inserted in normal fashion into the IS/1000 chassis where it plugs into the I/O bus.

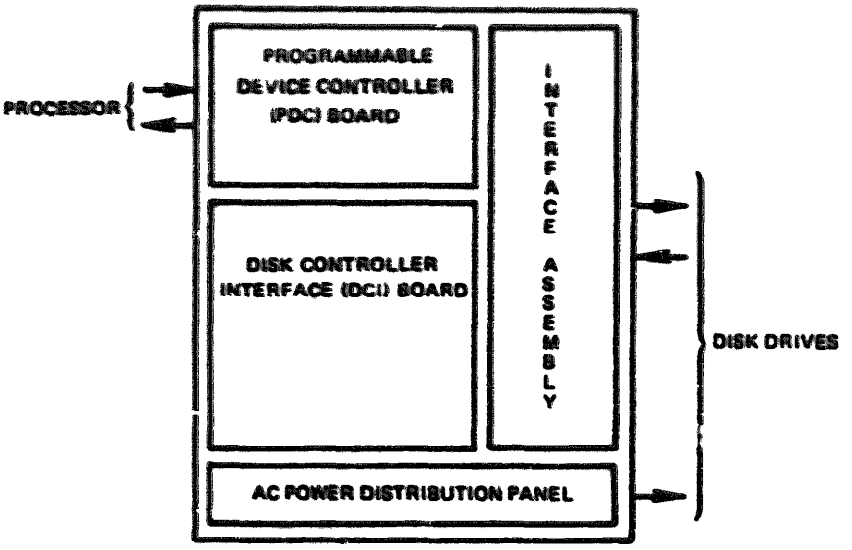


Figure 2-3. Magnetic Disk Controller (MDC), Main Logic Units 11056

Connector data for the PDC board is given in Tables 4-2, 4-3 and 4-4 of section 4, and in appendix C, engineering drawing 300337, page 4.

An IC map for the PDC board is given in appendix C, engineering drawing 300337, page 2.

2.3.2 Interface Controller

The Disk Controller Interface (DCI) board, shown in Figure 2-5, is a standard IS/1000 controller type printed circuit board. The interface controller logic is implemented through bipolar IC's of the 7400 series, and is mostly MSI technology. The DCI board is inserted in normal fashion into the IS/1000 chassis where it plugs into the I/O bus.

Connector data for the DCI board is given in Tables 4-5 through 4-8 of section 4, and in appendix C, engineering drawing 300352, page 4.

An IC map for the DCI board is given in appendix C, engineering drawing 300352, page 2.

2.3.3 Interface Assembly

The interface assembly shown in Figure 2-6, consists of an IS/1000 card chassis in which the following logic cards are inserted:

- Power Sequencer card.
- Phase Locked Oscillator card.

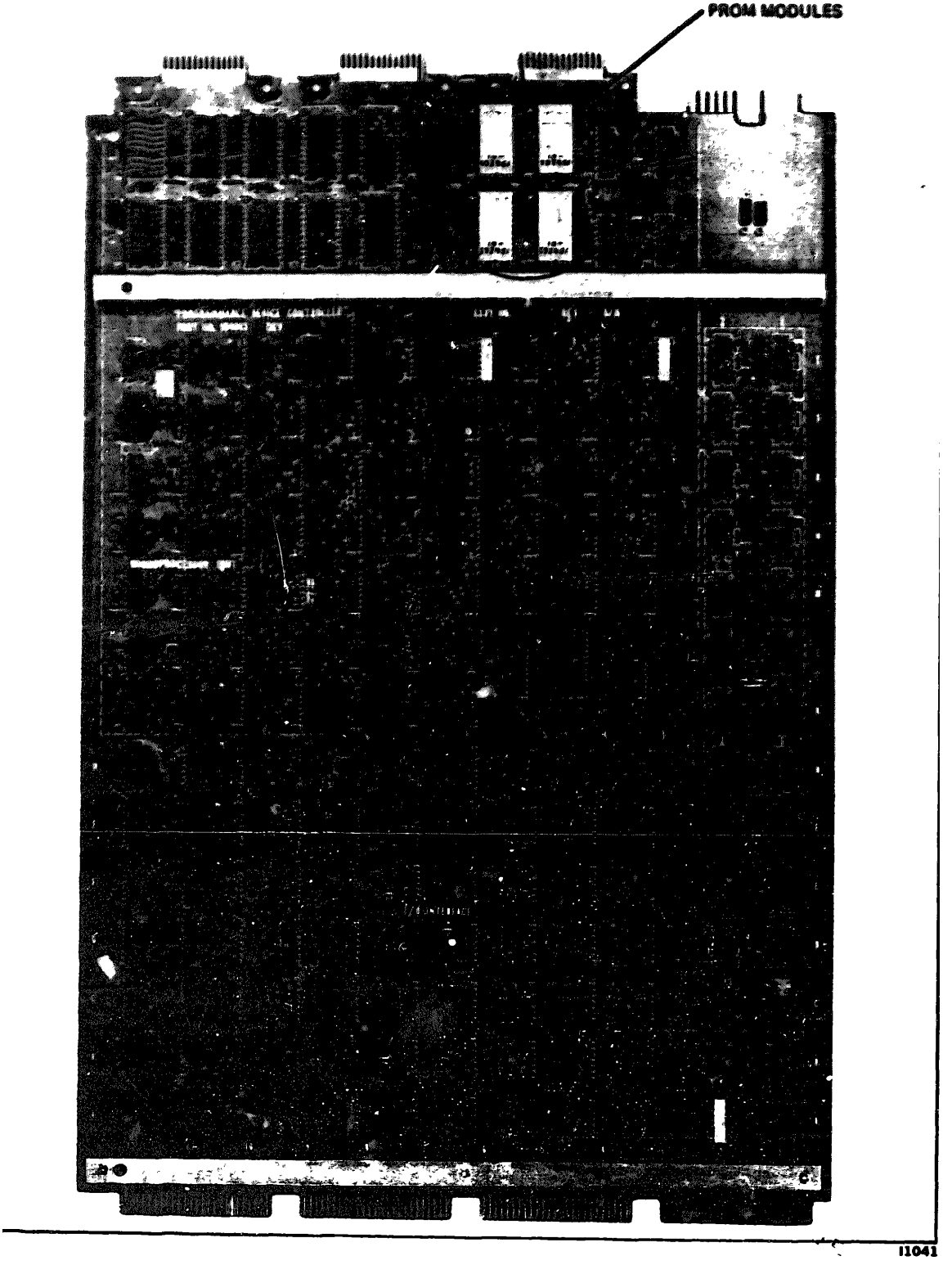


Figure 2-4. Programmable Device Controller (PDC) Board

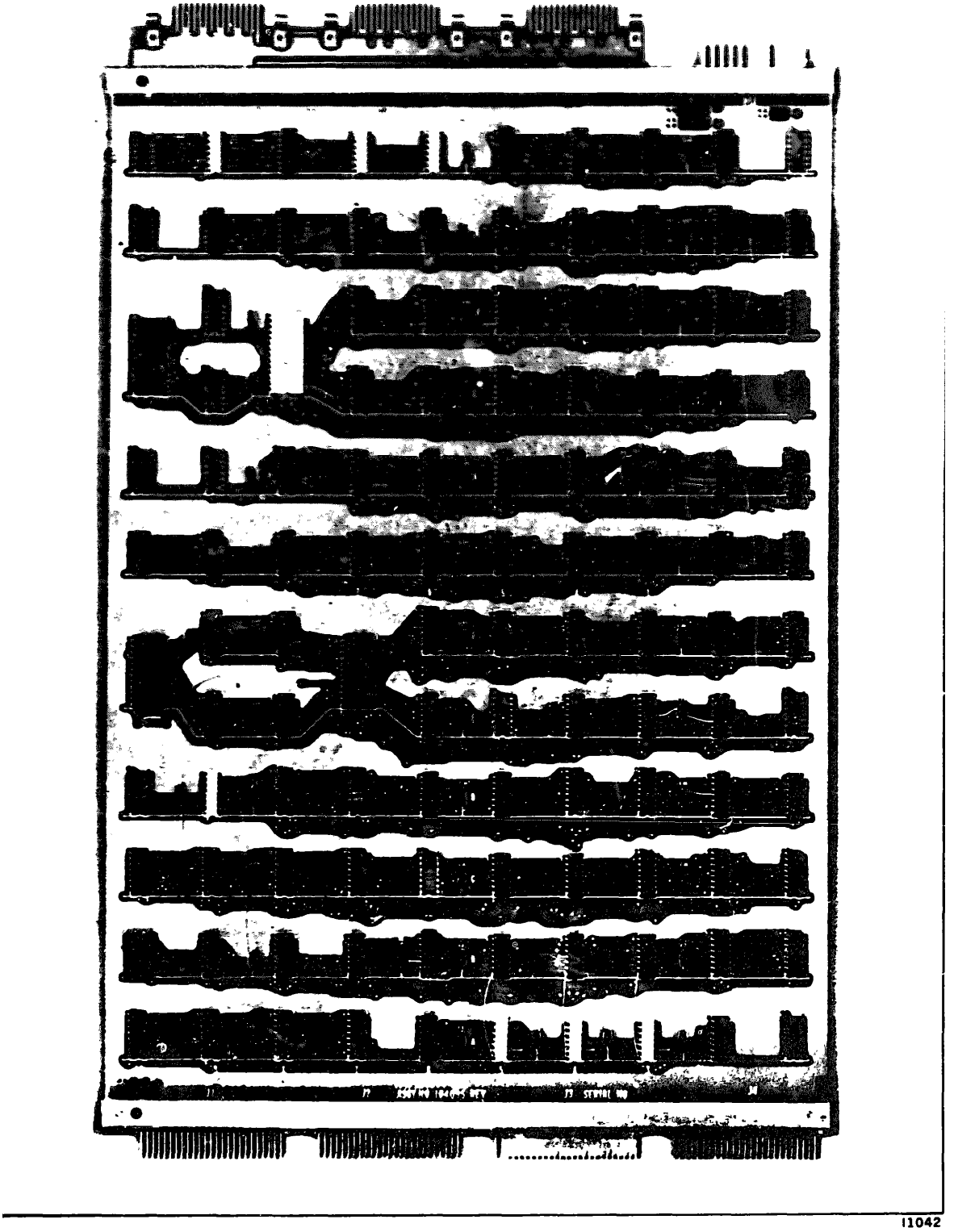


Figure 2-5. Disk Controller Interface (DCI) Board

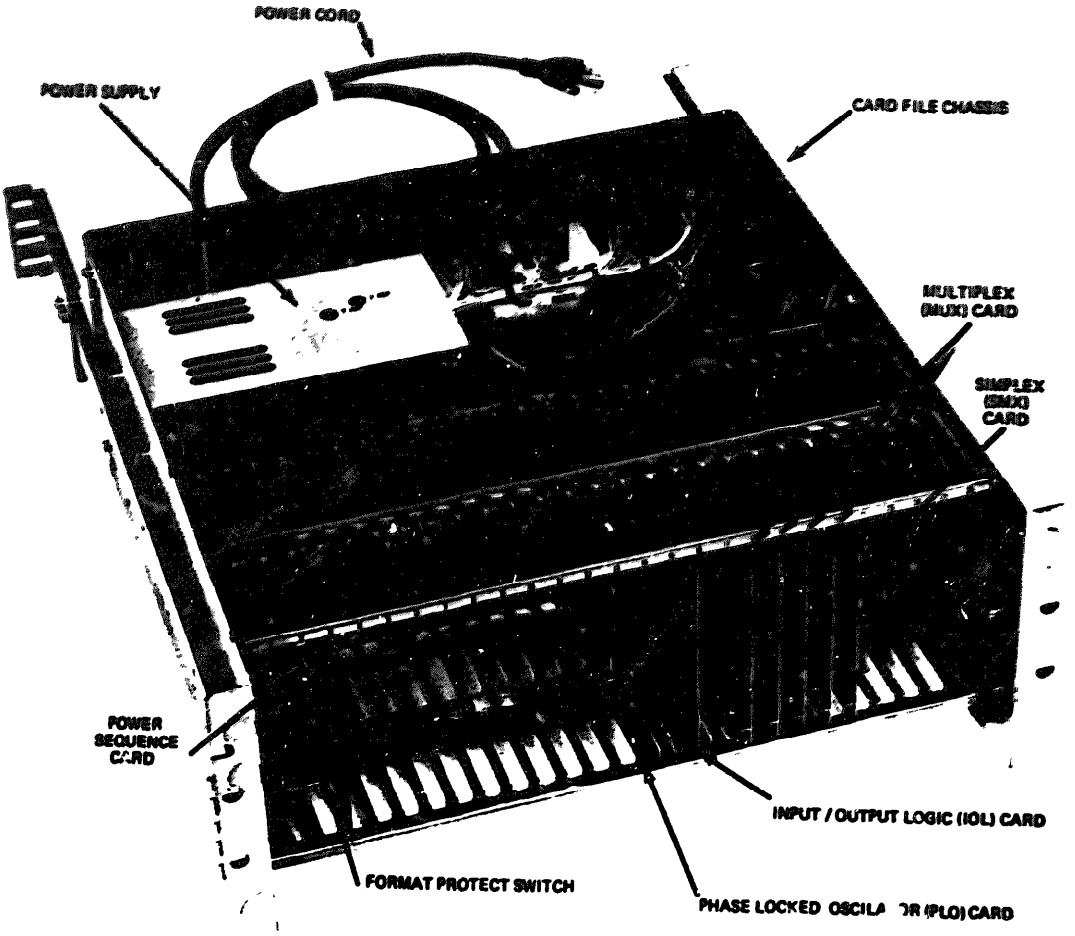


Figure 2-6. Interface Assembly, Front View

11043

- I/O Logic card.
- Simplex card(s).
- Multiplex cards.

2.3.3.1 Power Sequencer Card

The Power Sequencer (PSQ) card, is located in slot 3 of the chassis. The PSQ card contains the sequencing logic necessary for the control of the power up and power down sequences of the disk drives in the

magnetic disk subsystem. The PSQ card is shown in Figures 2-6 and 2-7. For connector data see Table 4-16, under Servicing in Section 4.

2.3.3.2 Phase Locked Oscillator Card

The Phase Locked Oscillator (PLO) card, is located in slot 14 of the chassis. The PLO card is shown in Figures 2-6 and 2-7. For connector data see Table 4-15, under Servicing in Section 4.

2.3.3.3 I/O Logic Card

The I/O Logic (IOL) card is located in slot 16 of the chassis. The I/O Logic card contains drive address decoding logic, and read and write data clock generation for data going to, or coming from, the disk drives in the disk subsystem. The IOL card is shown in Figures 2-6 and 2-7. For connector data see Table 4-14, under Servicing in Section 4.

2.3.3.4 Simplex Card

The Simplex (SMX) card(s) are located in slots 22 and 23 of the chassis. If the disk subsystem comprises from one to four drives, only one Simplex card is required, which is to be located in slot 22. If the disk subsystem contains from five to eight disk drives, two Simplex cards must be used. The Simplex card contains the logic to process write, read and select status data from and to the individual disk drives.

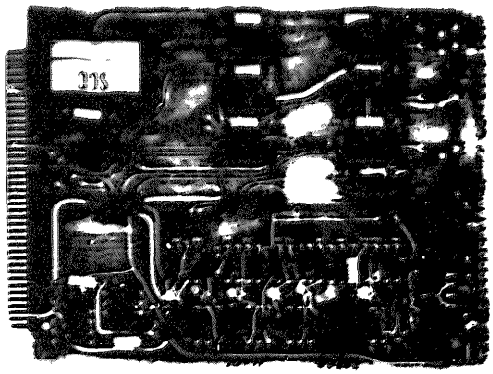
The Simplex card is shown in Figures 2-6 and 2-7. For connector data refer to Tables 4-17 and 4-18, under Servicing in Section 4.

2.3.3.5 Multiplex Card

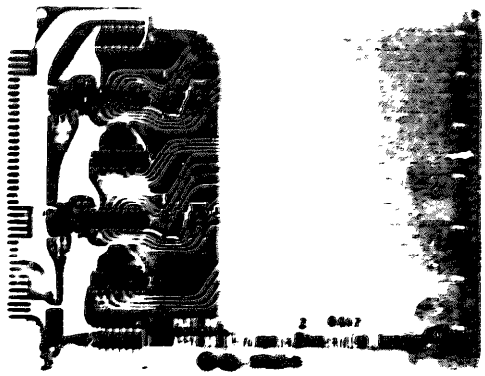
Four Multiplex (MUX) cards are located in slots 18, 19, 20 and 21 of the chassis. The Multiplex cards provide the multiplexing logic to enable controlled data exchanges between the drives and the controller, on a time shared basis. The Multiplex cards are shown in Figures 2-6 and 2-7. For connector data refer to Tables 4-19 thru 4-22, under Servicing in Section 4.

2.3.3.6 Chassis

The chassis itself fits in a standard RETMA 19 inch rack or cabinet and can be mounted away and apart from the controller boards. Mounted in a rack or cabinet, the chassis requires 7.00 inches of vertical space. In the back, the chassis contains fourteen connector sockets and a power cable. The power cable plugs into a suitable 110 Vac 60 Hz power source. Connectors designated J34 thru J41, individually connect each of up to a possible eight disk drives in the subsystem, via a DC cable. Connectors designated J31, J32 and J33, connect to the DCI board via three interface cables. The J42 designated connector connects to the first disk drive in the subsystem, via the signal cable. In the case of a multi-spindle disk subsystem, the signals of J42 are propagated from drive to drive in daisy-chain fashion.

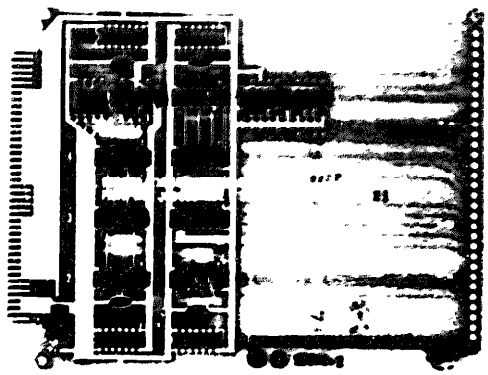


PHASE LOCKED OSCILLATOR CARD

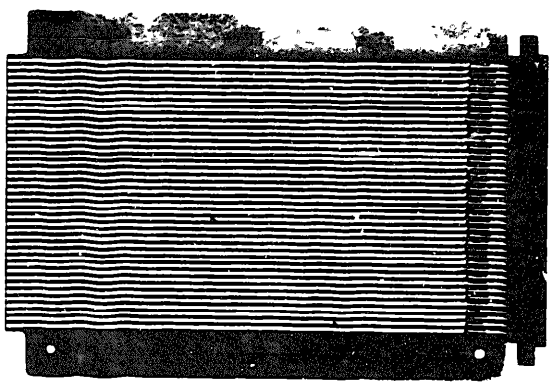


SIMPLEX CARD

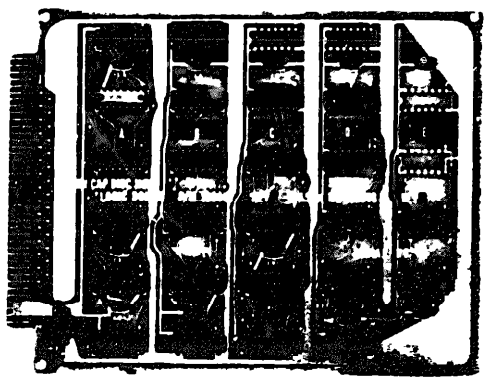
POWER SEQUENCER CARD



MULTIPLEX CARD



EXTENDER CARD



INTERFACE LOGIC CARD

I1044

Figure 2-7. Interface Assembly Logic Cards

The chassis is shown in Figure 2-8. For connector data, see Figure 4-8 in Section 4 under Cabling and Patching.

2.3.4 AC Power Distribution Panel

A power distribution panel (PDP) for three phase AC power distribution to the disk drives in the subsystem, is shown in Figure 2-9. The PDP has a ten feet long power cable that plugs into an appropriate power outlet. The AC Power Outlet connector for power distribution to the disk drives in the Subsystem, is mounted on the face panel of the assembly. A transformer providing continuous ac power to the power sequencing logic on the PS card in the interface assembly, is located in the PDP.

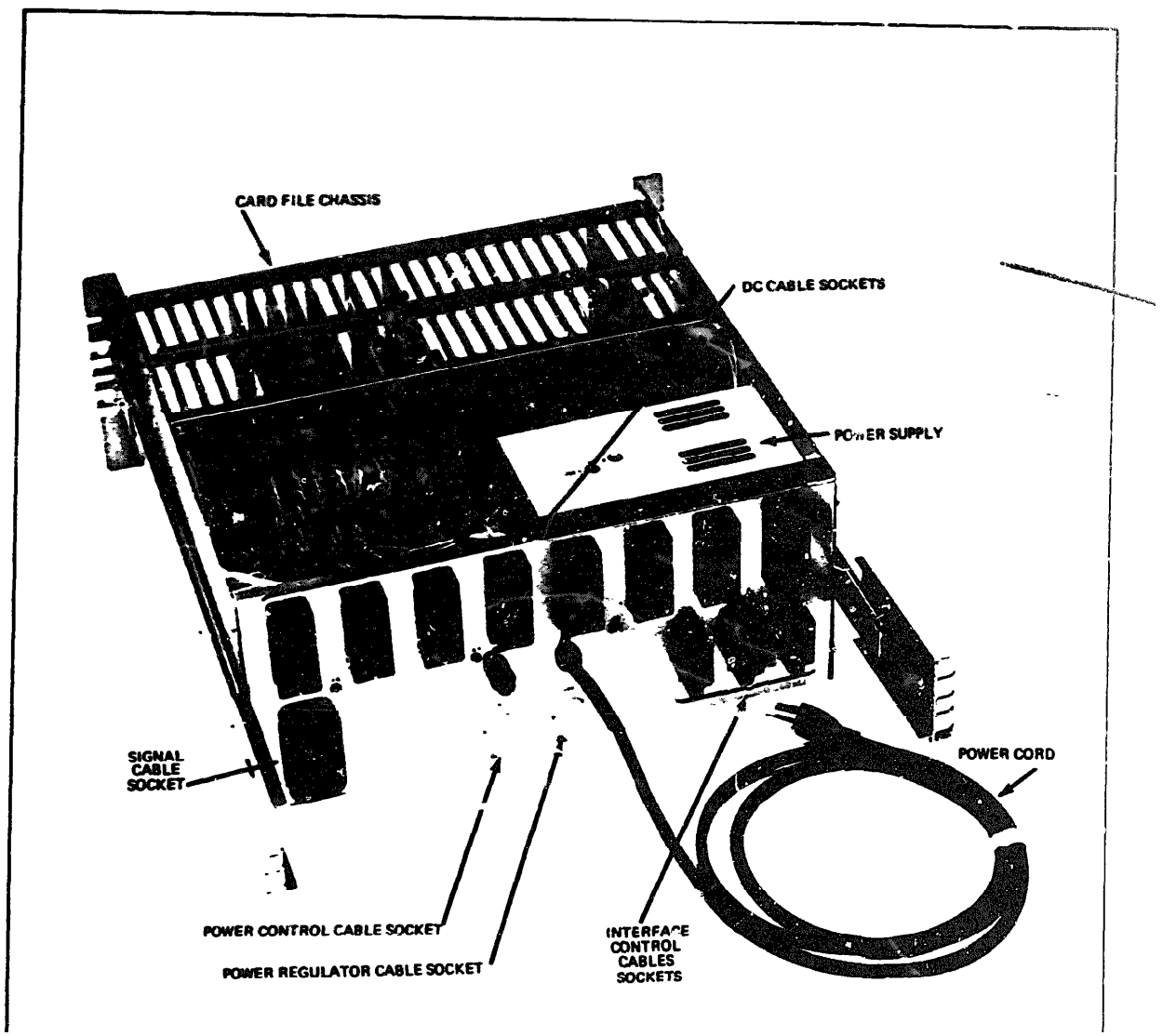


Figure 2-8. Interface Assembly, Rear View

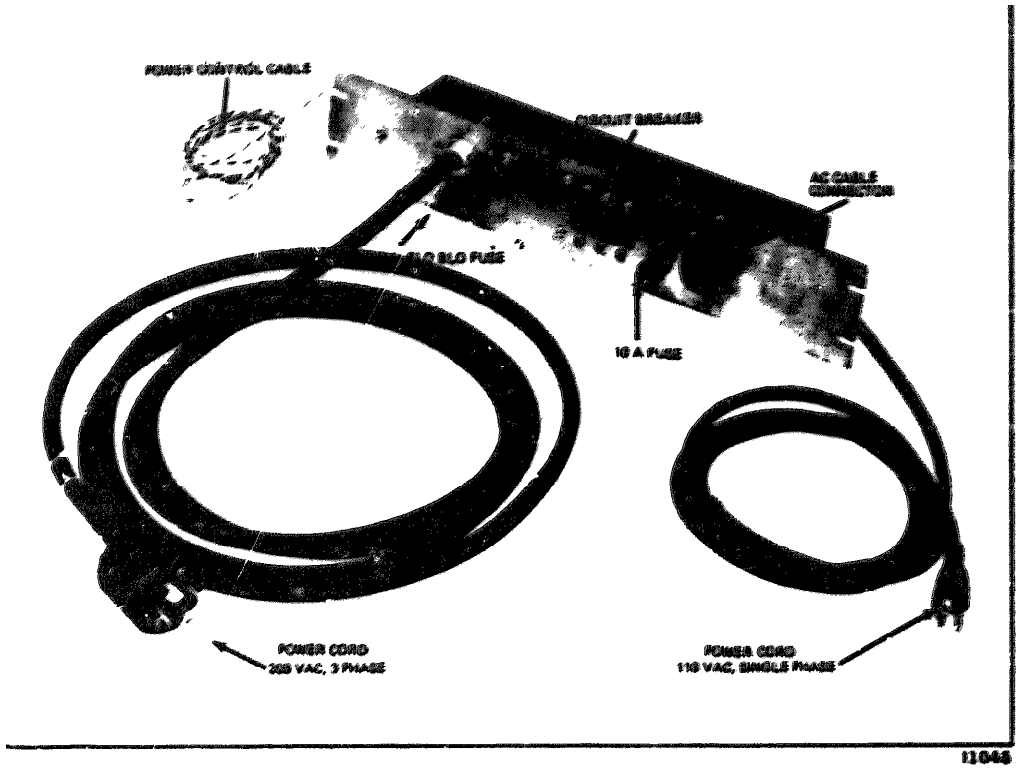


Figure 2-9. AC Power Distribution Panel (PDP)

The PDP mounts in a standard RETMA 19-inch rack or cabinet where it requires 3.5 inches of vertical rack space. Under normal circumstances, the PDP is mounted directly under the front panel of the interface assembly.

2.4 FUNCTIONAL DESCRIPTION

The following paragraphs describe the magnetic disk controller (MDC) functionally to the major logic block level. In the theory of operation the operational flow of logic in the MDC is described in the context of the MDC functioning in a magnetic disk system with at least one disk drive attached to it.

2.4.1 Functional Blocks

Figure 2-10 is a block diagram of the magnetic disk controller (MDC). The MDC basically consists of four physical and logical units:

- Programmable Device Controller (PDC).
- Disk Controller Interface (DCI)
- Interface Assembly (IOA).
- Power Distribution Panel (PDP).

A description of each major block, its sub-blocks and the functions performed, is given hereunder.

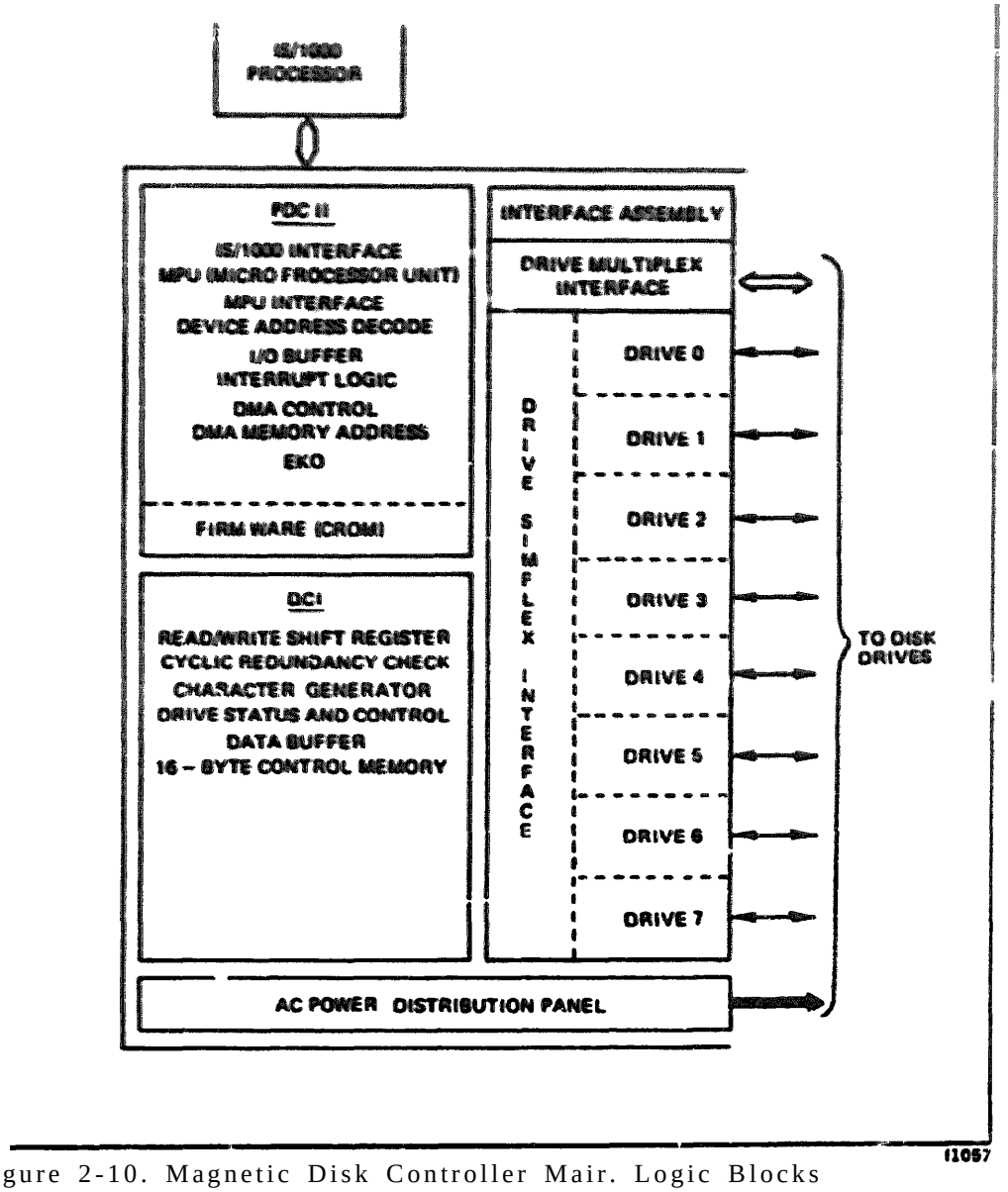


Figure 2-10. Magnetic Disk Controller Mair. Logic Blocks

2.4.2 Programmable Device Controller

The programmable device controller (PDC) is shown in Figure 2-11. As can be seen, the PDC consists of three basic blocks:

- CPU Interface.
- Control Read Only Memory (CROM).
- Microprocessor.

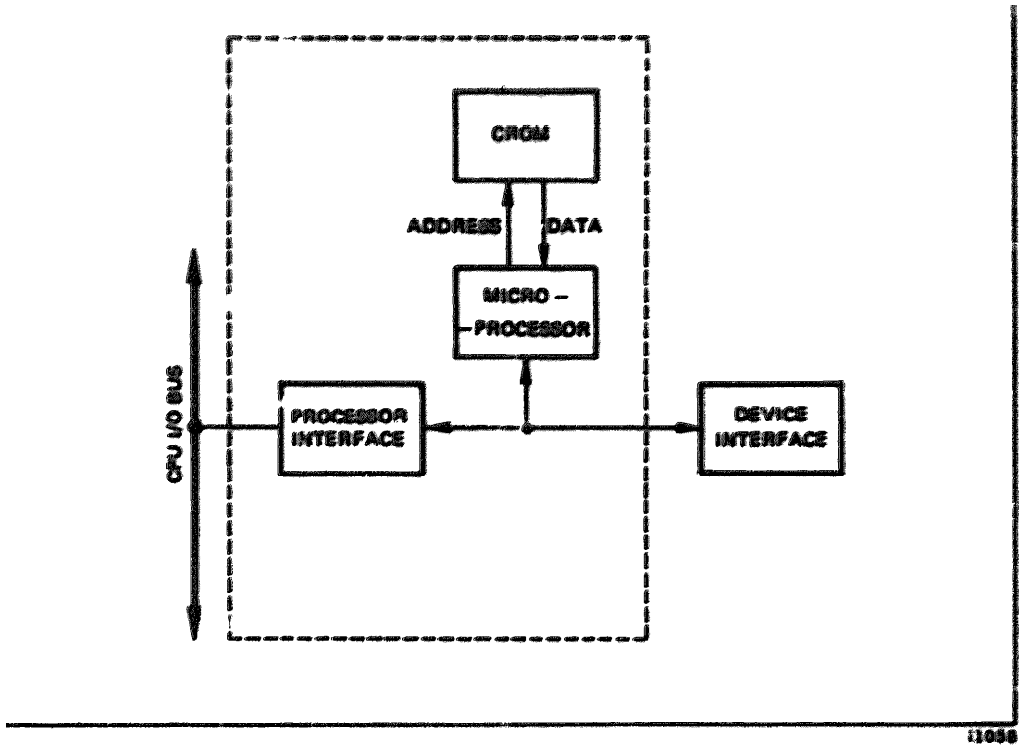


Figure 2-11. PDC Block Diagram, Logic Structure

2.4.2.1 CPU Interface

The CPU Interface comprises the logic necessary for communication between the MDC and the IS/1000 CPU and memory and consists of the following:

- **Address/Command Decoding and Interrupt Logic.**
- **Microprocessor Interface and Control Logic.**
- **DMA Registers and Sequence Logic.**

ADDRESS/COMMAND DECODING AND INTERRUPT LOGIC. The address decoding, command decoding and interrupt logic encompasses the device address patches, interrupt and ICI patches, the address compare logic, the command decode and EKO logic, and the interrupt flag, the EDF STR enable flag, the command flag, as well as the CPU I/O bus drivers and receivers.

The interrupt flag can be set and read by the microprocessor.

The EDF STR enable flag can be set, reset and read by the microprocessor.

The command flag is set when EDF STR instruction is decoded and the EDF STR flag is true. The command flag can also be set, reset and read by the microprocessor.

DMA REGISTERS AND SEQUENCE LOGIC. The DMA registers and sequence logic encompasses the DMA priority patch, the DMA sequence logic, and the DMA data, address, and mode registers.

The DMA registers and associated data paths are shown in Figure 2-12.

The DMA sequence logic provides the timing and control signals required to read data out of, or write data into, the CPU memory.

The DMA data register holds one or two bytes of data that is to be written into, or has been read out of, the CPU memory during DMA write or read operations, respectively. The DMA data register additionally accepts the initialization buffer address that is supplied with the EDF INI command during the initialization phase.

The DMA address register holds the memory address during DMA write and read operations. The contents of the DMA address register are gated on the DIB lines whenever a RDS command is decoded; hence, under special conditions, the DMA address register can also be used as a status register.

The DMA mode register contains the data specifying the type of DMA operation to be performed, i.e., read, write left (upper) byte, write right (lower) byte, or write left and right bytes. The DMA mode register also serves as a DMA-cycle-in-progress flag which can be read by the microprocessor.

MICROPROCESSOR INTERFACE AND CONTROL LOGIC. The microprocessor interface and control logic contains the drivers and receivers required to interface with the microprocessor I/O bus. In addition the logic provides the control signals necessary to write into, or read from, the DMA registers, and the interrupt, EDF STR enable, and command flags. All of the above control signals are generated through the decoding of certain preassigned addresses on the microprocessor address bus.

2.4.2.2 Control Read Only Memory

The control read only memory (CROM) stores the microcode controlling the operations of the controller. The CROM is implemented for 4,096 words of 16 bits each.

2.4.2.3 Microprocessor

The eight-bit microprocessor provides the record address conversions, function sequencing and function timing, as well as all other controls of the disk controller. The block diagram of the microprocessor is shown in Figure 2-13. Following is a description of each of the logic blocks on the diagram. Refer to Table 2-1 for performance specifications.

ALU AND ACCUMULATOR. The ALU is an 8-bit function generator which implements any of the 16 ALU functions specified by an instruction. The generation of the proper ALU controls is accomplished with an ALU decode ROM (DROM). The address for this DROM is the ALU function field of the instruction word.

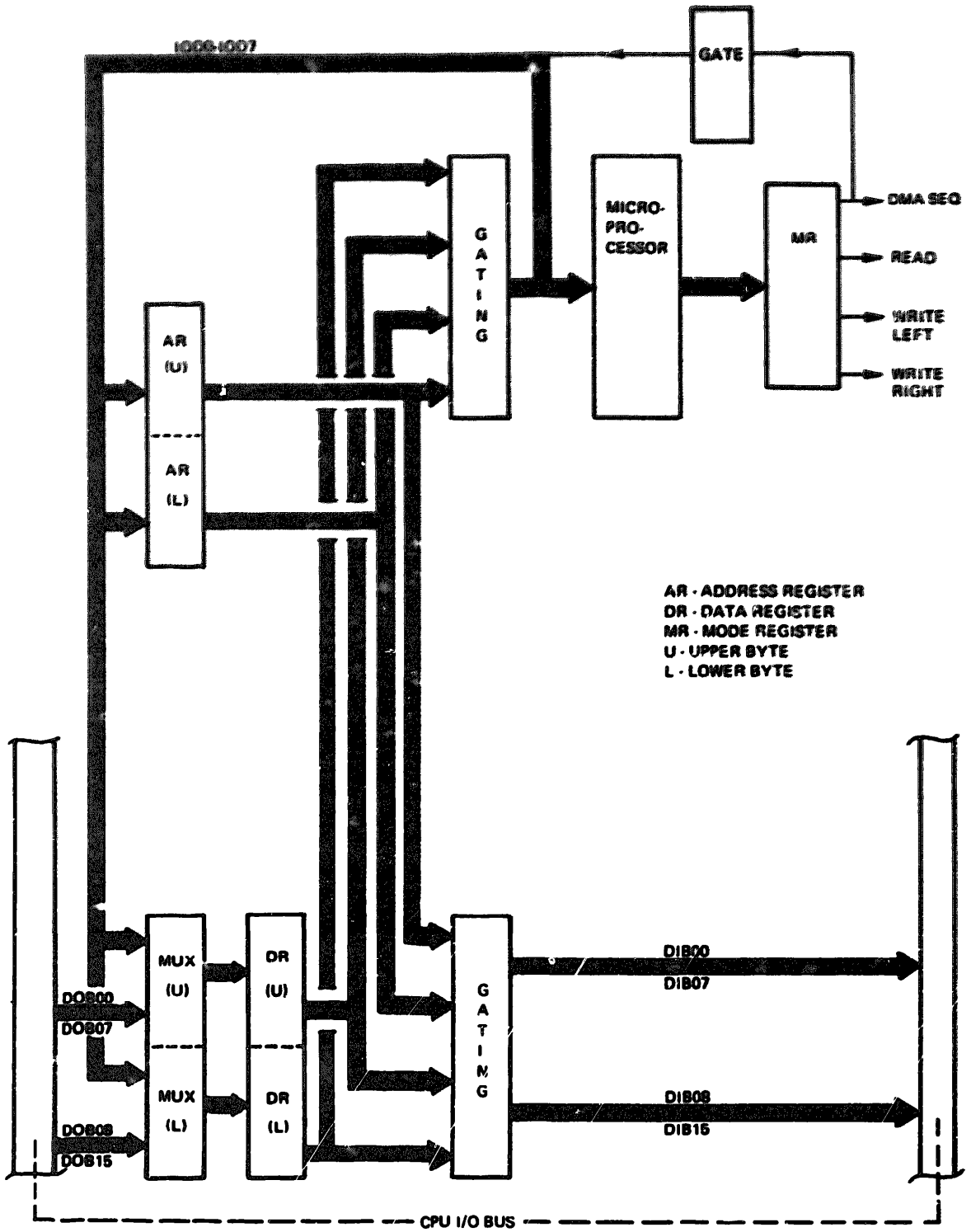


Figure 2-12. DMA Registers and Data Paths

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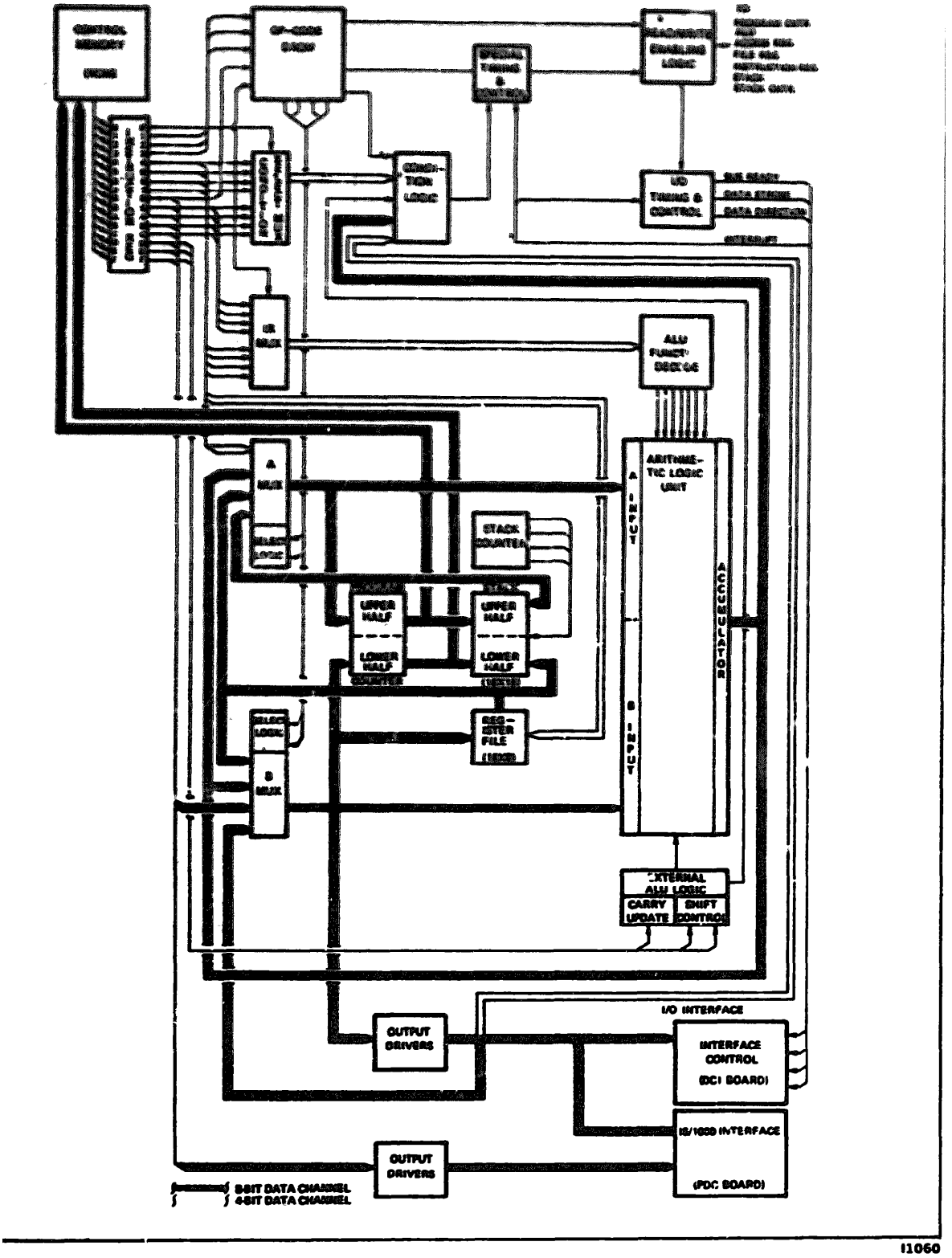


Figure 2-13. Microprocessor Block Diagram

Table 2-1. Microprocessor Performance Specifications

Feature	Specification
Cycle Time	200 ns.
CPU	8-bit ALU, micro program controlled.
Registers	1 Accumulator. 16 File Registers. 16 Stack Registers.
Instructions	23 Instruction Codes. 64 ALU Commands. 4 Unassigned Op codes.
Instruction Repertoire	Arithmetic, I/O, Branch, Data Transfer, Subroutine, Interrupt.
Control Memory	16-bit ROM, up to 64K words.
Logic	Standard bipolar TTL SSI and MSI technology ICs.
Input/Output	8-bit bidirectional data bus, data-in and data-out instructions, Test I/O instructions.
Interrupt Capability	Single line asynchronous request, enable/disable control, response into dedicated location.

The 8-bit accumulator retains the result of all ALU operations. In addition, the capability for a left or right shift of one bit position is provided in the accumulator. The serial input during left and right shifting is determined by selection bits within the shift instruction word. A carry flag capability is provided as an extension of the accumulator.

MULTIPLEXERS. The AMUX multiplexer selects the data source for the A-input, while the BMUX multiplexer selects the data source for the B-input, of the ALU. In addition, the AMUX provides the input to the upper half of the program counter, while the BMUX provides inputs to the I/O data bus, the file registers and the lower half of the program counter. As such, these multiplexers each drive a bus in the two-bus architectural philosophy on which the microprocessor is based.

STACK. The Stack consists of 16 registers of 16 bits each. The Stack registers are used only for storage of the program counter contents in the implementation of subroutine transfers. A 4-bit binary up/down counter determines the selection of a particular Stack register. This stack counter is incremented during execution of the PUSH and BRANCH instructions prior to the actual storage of the program counter. When executing a RETURN instruction (POP), the contents of the addressed Stack register is loaded into the program counter after which the counter is decremented. Visibility

of the actual data in this counter is not necessary since only the relative number of increments or decrements is pertinent to its operation.

FILE. The File contains 16 general purpose registers of 8 bits each. The File registers are addressed by a 4-bit field of the instruction word. The File is used for input and output data, and as a source for branch addresses and arithmetic operations.

PROGRAM COUNTER. The program counter is a 16-bit register providing addressing capability of up to 64K words in the main ROM. The program counter determines through its contents from which location of the ROM an instruction is fetched. Each instruction either increments the program counter or causes a new value to be loaded into the program counter during branching.

INSTRUCTION REGISTER. The instruction register holds the current instruction to be executed. The instruction is entered into the instruction register from the ROM data output bus. At the beginning of each instruction, the instruction register is updated with the new instruction on the memory data lines. The instruction word in the instruction register is used for decoding and control functions necessary in the execution of each instruction.

DECODE ROM. The DROM is a fast access (50 ns) 32 word x 16 bit ROM which generates the microinstruction containing the control bits necessary for CPU operation. The 5-bit op code portion of each instruction is used for the actual address of the DROM. The contents of the DROM thus define the operation of each instruction. The microprogram control approach allows flexibility in the instruction set selection and simplifies the microprocessor logic.

ROM. The main ROM is a semiconductor memory of up to 64K words x 16 bits. The control program residing in the ROM directs the microprocessor in the performance of its assigned tasks. The access time of the ROM must be less than 150 ns, measured from address-valid time to the memory-data-valid time at the instruction register.

CONTROL LOGIC. This logic provides the timing for all instructions, conditional testing control, and additional miscellaneous control. Logic for the implementation of the interrupt function provides the enable mask, the mask control, and control signals to the instruction register and the program counter.

I/O INTERFACE. The I/O interface provides the drivers and receivers for the bidirectional data bus. The eight device address lines (DAxx) specified in all I/O instructions, are provided at the interface in addition to the following four I/O control signals:

- Bus Ready.
- Data Strobe.
- Data Directional Line.
- Clock.

2.4.3 Device Interface Control

The Device Interface Control, consisting of the Disk Controller Interface (DCI) and the Interface Assembly (IOA), is shown in Figure 2-10. A more detailed block diagram is shown in Figure 2-14. The Device Interface Control physically consists of two entities, the DCI board and the IOA chassis. Functionally, the Device Interface Control comprises control logic for the input/output data to and from the processor, control logic for the input/output data from and to the disk drive(s), and the control logic controlling the AC power distribution to the drives by sequencing the powering up and powering down of the drives in a multiple disk drive subsystem.

2.4.3.1 Processor I/O Control Logic

The processor input/output data control function provides an avenue and the controls for the proper flow of communications in the form of commands, data, interrupts and status information, between the controller and the processor. It contains the necessary receivers, transmitters and control logic to interface the controller with the IS/1000 I/O bus lines. The processor input/output data control function comprises the following logic blocks.

DEVICE ADDRESS DECODE. The device address decode logic decodes the six I/O address lines into one device address. The device address is semi-permanently coded by means of patchboards.

EKO. The EKO logic generates and transmits the EKO Signal to the processor in response to a valid command, to signify that the controller is not busy.

I/O BUFFER. The I/O buffer stores 16 bits of I/O information.

INTERRUPT LOGIC. The interrupt logic determines the necessity of an interrupt, develops the interrupt and sends the interrupt to the processor.

DMA CONTROL. The DMA logic provides the timing and control for data transfers using the DMA feature.

2.4.3.2 Drive I/O Control Logic

The drive input/output data control function provides buffer logic between the drive interface and either the PDC or the processor interface control. The drive input/output data control function comprises the following logic blocks.

DATA BUFFER. The data buffer relieves the CPU and DMA functions from the stringent timing requirements of the data transfers.

CONTROL MEMORY. The control memory has a 16-byte storage capacity. The control memory is used to transmit Seek information to the selected drive and to compare track header data in order to locate the correct sector before a read or write operation is allowed to commence.

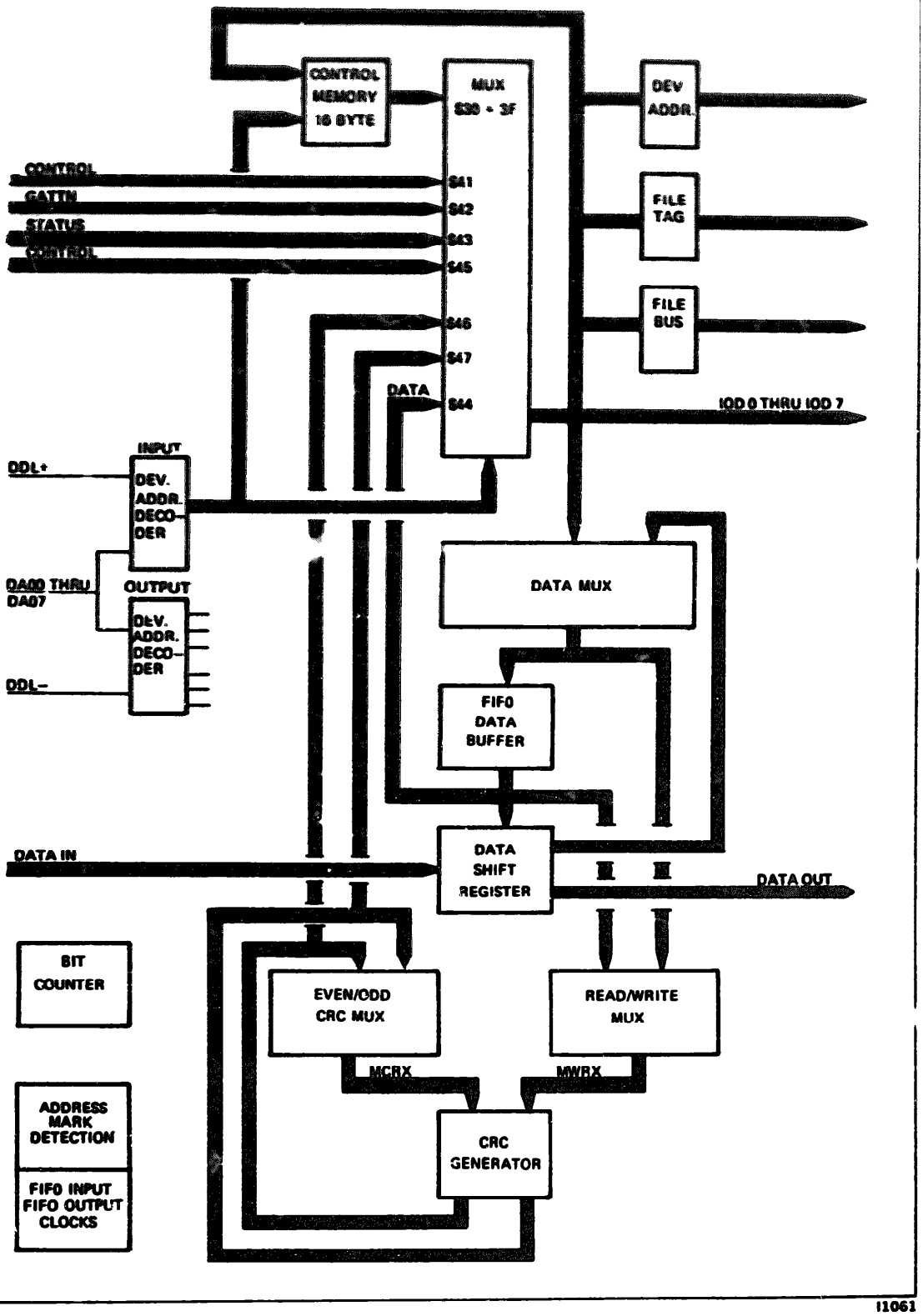


Figure 2-14. Device Interface Control Block Diagram

SHIFT REGISTER. The Data Shift Register is an 8-bit shift register used for the serializing and deserializing of write/read data, transferred between the selected disk drive and the data buffer.

CYCLIC REDUNDANCY CHECK LOGIC. The cyclic redundancy check logic comprises a 16-bit shift register which is used to generate cyclic redundancy check characters which then are used to check for data errors on comparison of congruent data. During a write operation, coding of the cyclic redundancy check character (CRCC) is derived from the data itself, after which the CRCC is appended to the particular record. During a subsequent read operation of that record, the CRCC is again generated, and the two CRC-characters are compared. The comparison of the two CRC-characters generated by the same data, enables detection of all errors involving an odd number of bits and all burst errors up to sixteen bits in length.

DRIVE STATUS AND CONTROL INTERFACE. This interface provides a communication path between the PDC and device interface for commands and status.

2.4.3.3 AC Power Sequencing Control

AC power to the drives in the disk system is provided by the power distribution panel (PDP). The supply of AC power to the drives, however, is sequenced during the power up and power down stages. The power sequencing is a combined function of the controller and the disk drive(s), and is controlled in the controller, by the power sequencing logic on the power sequencer card.

POWER UP SEQUENCE. During the power up sequence, the controller power sequence logic activates the Controlled Ground line to the drives when all voltages are in tolerance and have stabilized. This enables the drives to power up.

POWER DOWN SEQUENCE. During the power down sequence, the controller power sequence logic deactivates the Controlled Ground line to the drives. This forces the drives to power down.

After all drives have retracted their read/write heads, the AC power sequence logic will remove ground from the Heads Extended line. This signals to the controller that dc power can be removed without danger of damaging the drive or disk pack.

2.4.4 Software

The Disk Controller attaches to the IS/1000 I/O bus interface and provides control of the disk drives of the disk subsystem, (Figure 2-15). The controller services the disk drives on a time-shared basis. The controller interprets instructions received from the processor over the I/O bus, issues commands to the disk drives, assembles and disassembles data words for transfers between the drives and the processor, and sends status information to the processor.

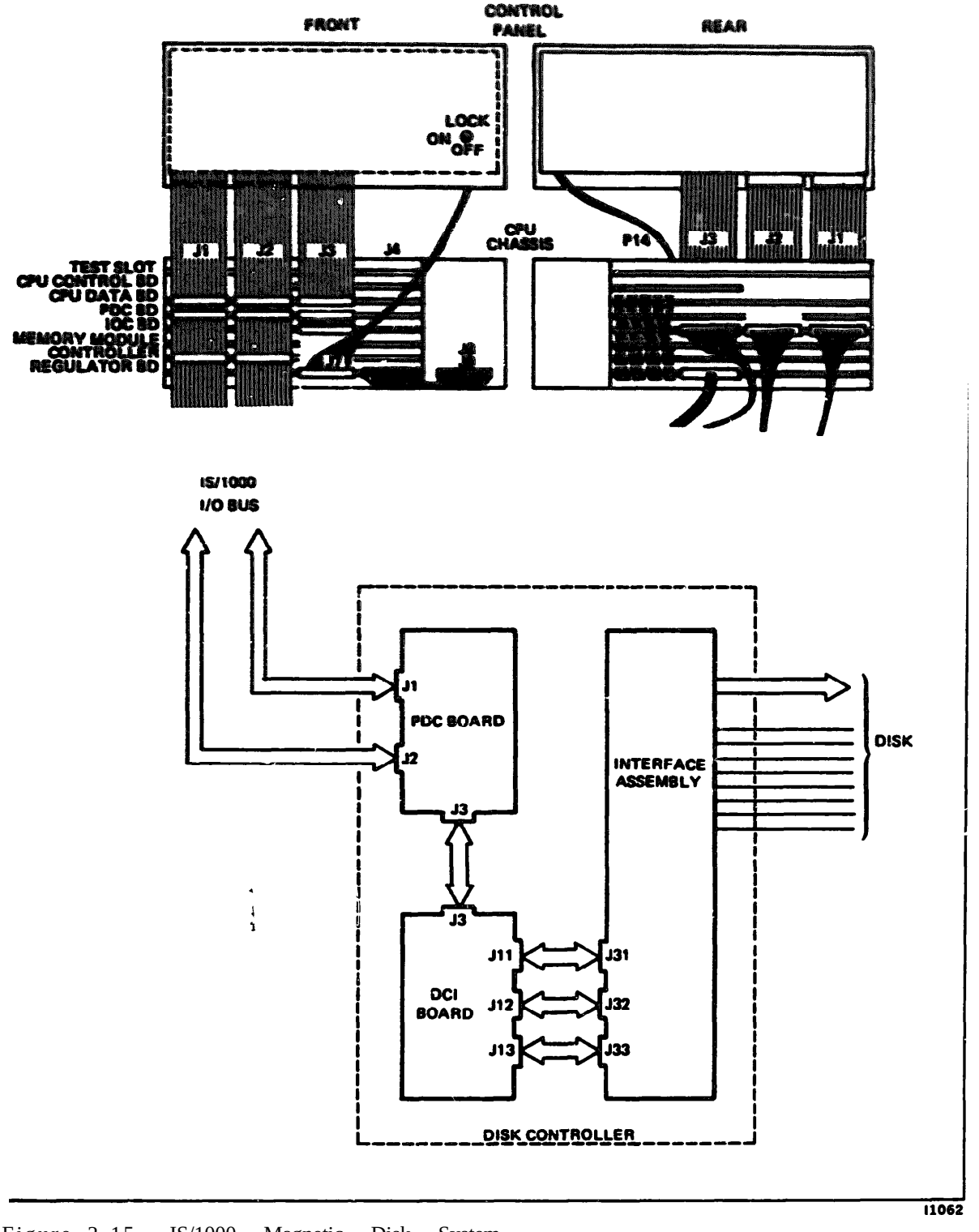


Figure 2-15. IS/1000 Magnetic Disk System

All data transfers use the DMA. The major status word is available to the CPU through the use of the RDS instruction. One external interrupt is used. Any data line can be patched for ICI operation. All interrupts are reset through the use of RDS, which, optionally, can be made to clear the status conditions that activated the reset. The controller can transfer data blocks from 1 to 65,535 words.

The following paragraphs describe the instruction concept governing the hardware and the addressing and interrupt schemes. This is preceded by a description of the data organization scheme according to which data is formatted on the disk pack.

2.4.4.1 Data Organization

The same track format is used for both, the model 114 and model 215 disk drives. Data is recorded in each track according to a fixed record length, IBM compatible format. Therefore, a disk pack recorded by an IS/1000 computer system can be read by an IBM system, and conversely, a disk pack recorded by an IBM system can be read by an IS/1000 system. However, because of the double track density recording mode of the model 215 disk drive, this IBM compatibility is limited to disk packs used in model 114 disk drives only.

The track format, as shown in Figure 2-16, consists of sixteen data records of 346 bytes each, as follows:

- Home Address.
- Track Descriptor Header.
- Track Descriptor Data Field.
- Data Record Headers.
- Data Record Data Fields.
- Gaps.

Home Address. The Home Address (HA), see figure 2-16 and 2-17a, consists of seven bytes which define the track condition and the physical location of the track within the disk pack. There is one HA area per track. This area is created by a Format command and after the gap 1 that follows the index marker, is the first area written on a track. Contained within the HA area are five information bytes and two cyclic check bytes. Following is a description of the information contained in each byte.

BYTE 0 — FLAG BYTE. The eight bits comprising this byte, have the following function designations.

Bit 0: no function, always ZERO.

Bit 1: no function, always ZERO.

Bit 2: no function, always ZERO.

Bit 3: no function, always ZERO.

Bit 4: no function, always ZERO.

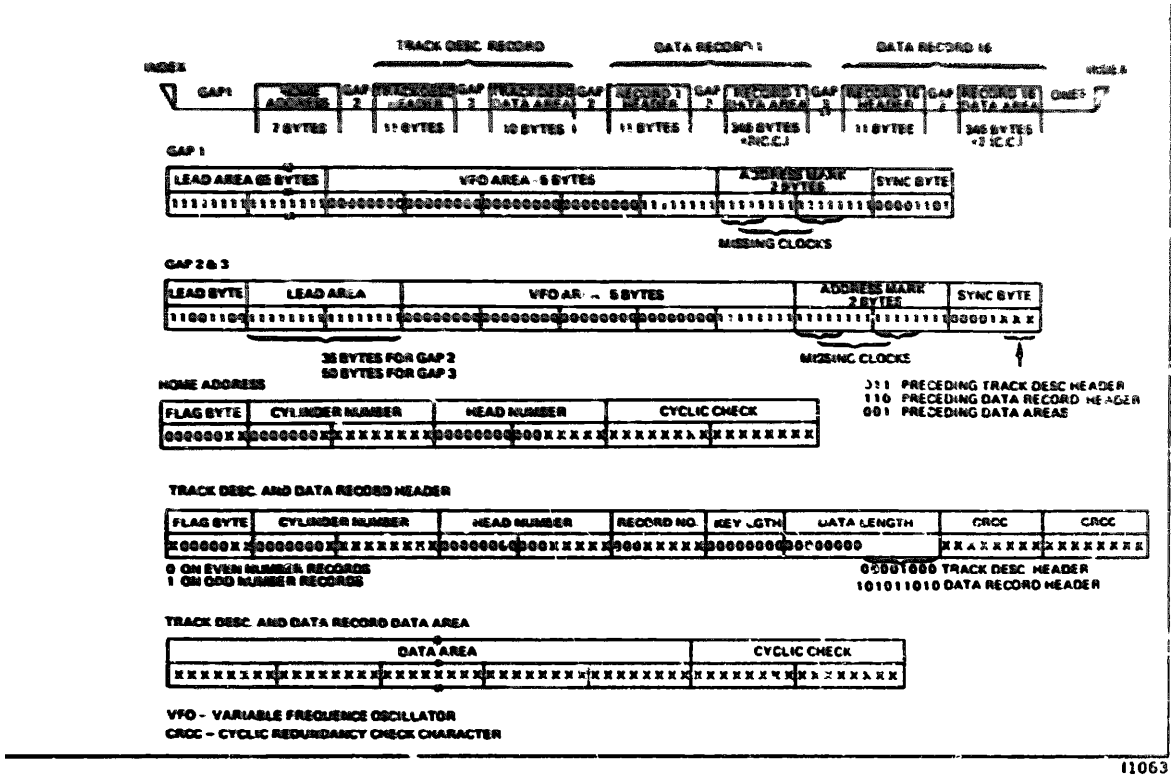


Figure 2-16. Track Format

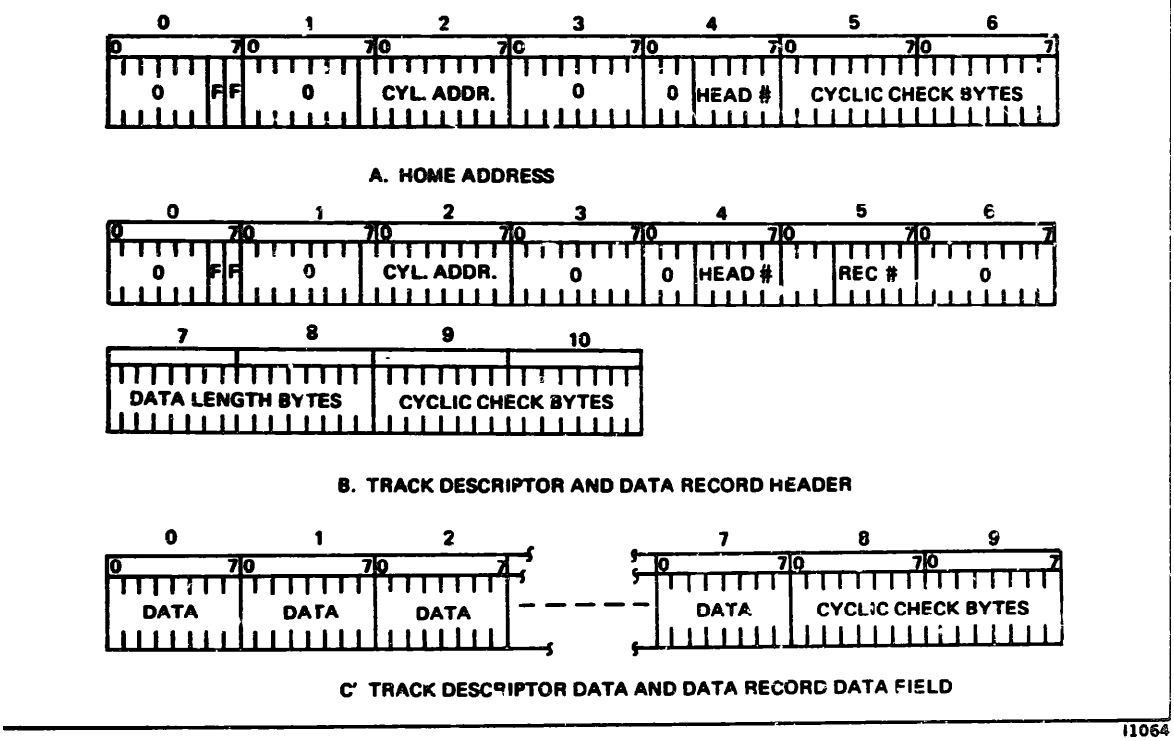


Figure 2-17. Track Format, Unit Detail

Bit 5: no function, always ZERO.

Bit 6: track function indicator

0 = good track

1 = defective track.

Bit 7: track usage indicator

0 = primary track

1 = alternate track.

Bits 6 and 7 may be used for other purposes if IBM format compatibility is not required.

BYTE 1 - CYLINDER ADDRESS BYTE 1. In model 114 applications this byte consists of all ZEROs. In model 215 applications, the LSB-bit may be 1.

BYTE 2 - CYLINDER ADDRESS BYTE 2. This byte is coded to specify the cylinder address.

BYTE 3 - HEAD ADDRESS BYTE 1. This byte contains all ZEROs.

BYTE 4 - HEAD ADDRESS BYTE 2. This byte is coded to specify the head address.

BYTE 5 - CYCLIC REDUNDANCY CHECK BYTE 1. This byte is together with byte 6, generated by hardware during the write HA phase of the Format command.

BYTE 6 - CYCLIC REDUNDANCY CHECK BYTE 2. This byte is together with byte 5, generated by hardware during the Write HA phase of the Format command.

Track Descriptor Header. The first record following the HA is the Track Descriptor Header record (see Figures 2-16 and 2-17). The Track Descriptor Header record consist of eleven bytes and is provided to enable an entire track of data to be moved to an alternate track should a portion of the recording surface become defective. The first nine bytes are information bytes, the last two bytes are cyclic check bytes. The process of switching data from a primary track to an alternate track is called flagging. Following is a description of the information contained in each byte.

BYTE 0 - FLAG BYTE. The eight bits comprising this byte, have the following function designations.

Bit 0: no function, always ZERO.

Bit 1: no function, always ZERO.

Bit 2: no function, always ZERO.

Bit 4: no function, always ZERO.

Bit 5: no function, always ZERO.

Bit 6: track function indicator

0 = good track

1 = defective track.

Bit 7: track usage indicator

0 = primary track

1 = alternate track.

Bits 6 and 7 may be used for other purposes if IBM format compatibility is not required.

BYTE 1 - CYLINDER ADDRESS BYTE 1. In model 114 applications this byte consists of all ZEROs. In model 215 applications, the LSB-bit may be 1.

BYTE 2 - CYLINDER ADDRESS BYTE 2. This byte is coded to specify the cylinder address.

BYTE 3 - HEAD ADDRESS BYTE 1. This byte contains all ZEROs.

BYTE 4 - HEAD ADDRESS BYTE 2. This byte is coded to specify the head address.

BYTE 5 - RECORD DESIGNATOR. This byte is coded to the record number. For the Track Descriptor record, this number is always ZERO.

BYTE 6 - KEY LENGTH DESIGNATOR. This byte defines the number of bytes in the key area in the IBM format. Since the GTE/IS format does not utilize key areas, this byte is all ZEROs.

BYTE 7 - DATA LENGTH INDICATOR 1. This byte together with byte 8, specifies the number of bytes in the data field of the record, excluding the Cyclic Redundancy Check bytes. For the Track Descriptor record, this number is always eight.

BYTE 8 - DATA LENGTH INDICATOR 2. This byte together with byte 7, specifies the number of bytes in the data field of the record, excluding the Cyclic Redundancy Check bytes. For the Track Descriptor record, this number is always eight.

BYTE 9 - CYCLIC REDUNDANCY CHECK BYTE 1. This byte, together with byte 10, constitutes the Cyclic Redundancy Check word. It is generated by hardware during the writing of the Track Descriptor Header phase of the Format command, and is then appended to the header.

BYTE 10 - CYCLIC REDUNDANCY CHECK BYTE 2. This byte, together with byte 9, constitutes the Cyclic Redundancy Check word. It is generated by hardware during the writing of the Track Descriptor Header phase of the Format command, and is then appended to the header.

Track Descriptor Data Field. The data field of the Track Descriptor record consists always of eight data bytes and two cyclic check bytes (see Figures 2-16 and 2-17c). The contents of this record are written by a FORMAT command. The eight data bytes constitute the four words which the controller requests from the processor. The data field contents may be used for any purpose except in IBM System 360 OS applications. In this case the data area must contain the identifier of the last record on the track and the number of bytes still available for writing on the track.

BYTES 0 THRU 7 - DATA FIELD BYTES. Bytes 0 through 7 are eight data bytes that constitute the four words requested from the processor by the controller on a Format command.

BYTE 8 AND 9 - ERROR DETECTION BYTES. Bytes 8 and 9 form the Cyclic Redundancy Check word. They are generated by hardware, then appended to the data area.

Data Record Header. The Data Record Header (Figure 2-16 and 2-17b) precedes each data record and has the same format as the Track Descriptor Header. The record area contains the number of the record and can be from 1 thru 16. The Key Length byte is always zero since the IS/1000 format does not use keys. The Data Length byte contains the number of bytes in the data area, which can be from 1 thru 346.

Data Record Data Field. The Data Record Data Field (Figures 2-16 and 2-17c) consists of 346 bytes of 173 words. The two cyclic character check bytes are generated by hardware during the writing of the data field and append to the record.

Gaps. Gaps are used to separate records and inter-record areas on the track, (see Figure 2-16). All gaps consist of a Lead Area, a VFO Area, an Address Mark and a Sync Byte. The Lead Area in gaps 2 and 3 is preceded by a so-called Lead Byte.

LEAD AREA. The Lead Area consists of bytes containing all ONEs. The main purpose of the Lead Area is to allow for spindle speed variations and for stabilization of the read and write logic during activation and deactivation of the read/write heads.

VFO AREA. The VFO Area always consists of five bytes. Four bytes contain all ZEROs, one contains all ONEs. The main purpose of the VFO Area is to enable synchronizing the VFO circuit.

ADDRESS MARK. The Address Mark consists of two bytes of all ONEs in which the clock pulses are missing for the first five bits of each byte. The Address Mark area therefore, is unique since it is the only area on the track where clock pulses are missing. The Address Mark serves as a pseudo sector mark and indicates that either a home address, a header or a data area is to follow.

LEAD BYTE. A Lead Byte is found in gaps 2 and 3 preceding the Lead Area. The Lead Byte is composed of the hexadecimal character $CC, and is written after the Cyclic Redundancy Check bytes in the preceding header.

SYNC BYTE. The Sync Byte consists of four ZEROs, and a ONE, followed by a three-bit code that describes what the area following is. The Sync Byte is used to orient the controller on byte boundaries for subsequent read operations.

2.4.4.2 Instruction Scheme

The instruction scheme employed in the magnetic disk controller, is based on the use of a packet. A packet is a set of five words stored in the IS/1000 processor memory. This 5-word packet determines the instruction to be executed and defines all criteria and parameters required for a successful execution of the instruction. In this instruction scheme, a disk system operation is initiated by the processor issuing an EDF STR instruction to the controller and placing the address of the memory location containing the first word of the packet, into the A register. Using DMA the controller then fetches the five operations from the CPU memory, goes busy, selects the specified drive, executes the indicated instruction, transfers data, sets status as needed, and finally activates the required interrupts during the termination sequence.

Packet Description. A packet consists of five consecutive words that specify the drive to be selected, the operation to be executed, the data to be operated upon, and define all criteria and parameters needed by the controller to control and successfully execute whatever operation is desired. Table 2-2 lists the five operation control words and their respective functions.

Table 2-2. Packet Structure

PACKET															
BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Operation Control Word	FUNCTION															
1	OP. CODE				INT	DR. ADR.			TR FL	SF	LB	SA	ST LOC D.S.			
2	Starting Location of next control word, if linked															
3	Starting Location of disc sector address															
4	Number of words/sectors to be operated on															
5	Memory location address of first data word															

CONTROL WORD 1. The first operation control word specifies and defines the following (see also Table 2-3).

- Operation to be executed - the operation to be executed is determined by the OP CODE, which is coded into the first four bits (bits 0, 1, 2 and 3) of the control word. Bit 0 indicates whether operations are to be linked. If command chaining is desired, bit 0 is ONE and control word 2 specifies the address of the next packet. The eight combinations of bits 1, 2 and 3, specify the type of operation to be performed.

- Interrupt to be set on termination of operation - whether or not the terminate interrupt is to be activated is determined by the INTERRUPT bit, bit 4 of the control word.

- Drive to be selected - the drive to be selected for the execution of the command specified by the OP CODE, is specified by the DRIVE ADDRESS which is coded into bits 5, 6 and 7 of the control word.

- Track status indication - to indicate whether the selected track is a primary or alternate track, good or defective, is indicated by the TRACK FLAG bits, bits 8 and 9 of the control word.

- Sector format indication - that the tracks are divided into sixteen sectors of 173 words each.

- Link Buffer designation - to designate a linked or not-linked buffer operation with the op code either 0000 or 0001, the Link Buffer bit, bit 11 is used.

- Sector Address indication - that each sector has a continuous binary address.

- Starting location of disk sector address - the starting location of the disk sector address is coded into bits 13, 14 and 15. Coding to standard format is as follows:

  000 = control word 3 contains the entire sector address.

  100 = contents of control word 3 plus 65,536 is the entire sector address. This, however, should only be used for CDS 215, i.e., for 200 TPI (tracks per inch) disk drives.

CONTROL WORD 2. The second operation control word specifies the starting location of the next packet if the link indicator bit in the op code, bit 0 of the first control word, is ONE, indicating linked operations.

Table 2-3. Operation Control Word One (Sheet 1 of 2)

Bit No.	Binary Coding	Function	Definition
0	0	Operational Code	Non-linked operation
0	1		Linked operation
1 2 3	000		Read
1 2 3	001		Write
1 2 3	010		Read Status
1 2 3	011		Seek
1 2 3	100		Format Track
1 2 3	101		Read Track Descriptor
1 2 3	110		Verify
1 2 3	111		Restore
4	0	Interrupt	Terminate Interrupt
4	1		No Terminate Interrupt
5 6 7	000	Drive Address	Disk Drive Number 0
5 6 7	001		Disk Drive Number 1
5 6 7	010		Disk Drive Number 2
5 6 7	011		Disk Drive Number 3
5 6 7	100		Disk Drive Number 4
5 6 7	101		Disk Drive Number 5
5 6 7	110		Disk Drive Number 6
5 6 7	111		Disk Drive Number 7
8 9	00	Track Flag	Good Primary Track
8 9	01		Good Alternate Track
8 9	10		Defective Primary Track
8 9	11		Defective Alternate Track

Table 2-3. Operation Control Word One (Sheet 2 of 2)

Bit No.	Binary Coding	Function	Definition
10	0	Sector Format	173 words per sector, 16 sectors per track.
10	1		Invalid command
11	0	Link Buffer	Not a linked operation, nor a linked buffer operation.
11	1		Linked buffer operation, OP. CODE is 1000 (Read) or 1001 (Write).
12	0	Sector Address	continuous binary sector address.
12	1		Invalid command
13 14 15	000	Sector, Format and Address	Word 3 is the complete sector address.
13 14 15	100	Format and Address	Word 3 plus 65,536 is the total sector address (only used for 200 tracks per inch drives).

CONTROL WORD 3. The third operation control word specifies the starting location of the sector address. This may be done in a standard format or an optional format.

In standard format the sector address is given in the form of a continuous binary address. In this format, bit 15 is the LSB and bit 0 the MSB for model 114 application. For model 215 application, bit 13 of the first control word is the MSB.

In optional format the sector address is expressed in cylinder, head and sector segments. Bits 13, 14 and 15 of the first control word together with bits 0 through five of the third control word specify the cylinder address number, with bit 5 being the LSB. Bits 6 through 10 of the third control word specify the head address number, with bit 10 being the LSB. Bits 11 through 15 of the third control word specify the sector number with bit 15 being the LSB.

CONTROL WORD 4. The fourth operation control word specifies for all operations, except Verify, the number of words to be operated on. For the Verify operation, the fourth control word specifies the number of sectors to be operated on.

CONTROL WORD 5. The fifth operation control word specifies the memory location address of the first data word to be read or written.

Basic Instructions. The four basic I/O instructions initiating all magnetic disk operations, are:

- EDF STR - Start DMA.
- EDF RST - Reset.
- ICI - Interrogate Common Interrupt.
- RDS - Read Devise Status and Reset Interrupt.

EDF STR. The EDF STR instruction has the following format.

(A indicates Device Address)

(R indicates Reject Address)

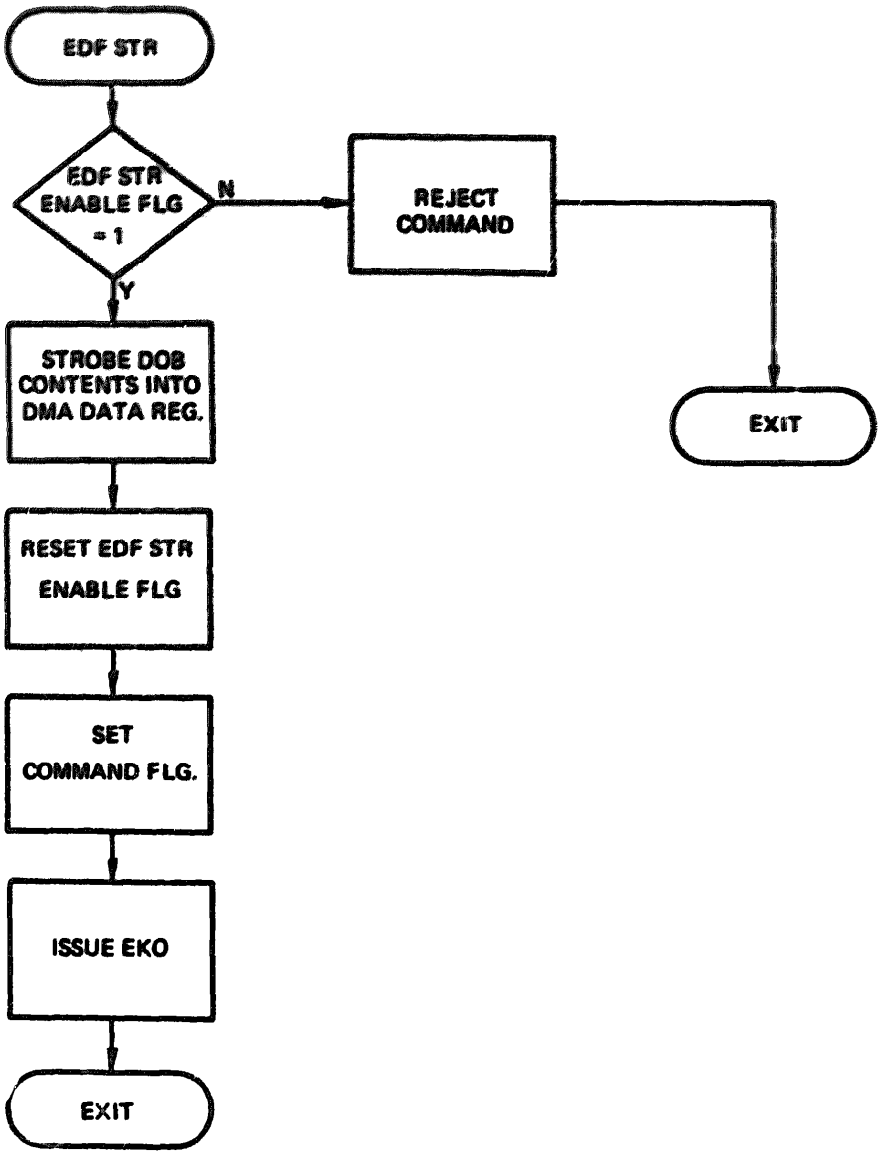
	Word 1				Word 2
		k-field	o-field	Device Address	Reject Address
Bit	0 1 2 3	4 5 6	7 8 9	10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	0 0 1 0	0 0 0	0 1 0	A A A A A A	R R R R R R R R R R R R R R R R

The EDF STR instruction causes the controller to cycle-steal the packet of five operation control words from the IS/1000 memory via DMA. The A register contains the memory location address of the first word. The reject address is the location to which a simulated BSP is performed when the instruction is rejected.

If the controller is busy, it will reject the EDF STR instruction.

If the selected drive is busy, the controller will delay execution of the EDF instruction until the drive completes its operation.

The operational flow of the executive of the EDF STR instruction, is depicted in the following flow chart.



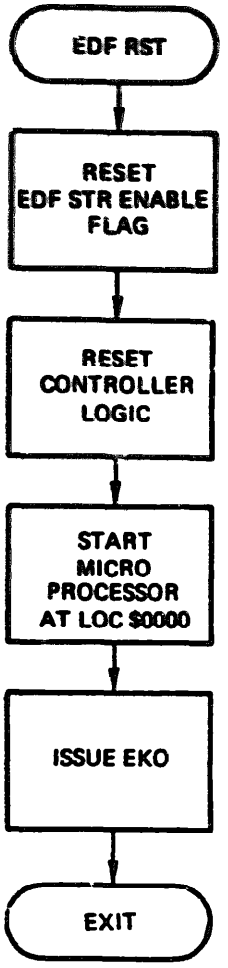
EDF RST. The EDF RST instruction has the following format:

(A indicates Device Address) - (R indicates Reject Address)

	Word 1				Word 2
		k-field	o-field	Device Address	Reject Address
Bit	0 1 2 3	4 5 6	7 8 9	10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	0 0 1 0	0 0 0	0 1 0	A A A A A A	R R R R R R R R R R R R R R R R

The EDF RST instruction resets the controller logic.

The operational flow of the EDF RST instruction execution is depicted in the following flow chart.



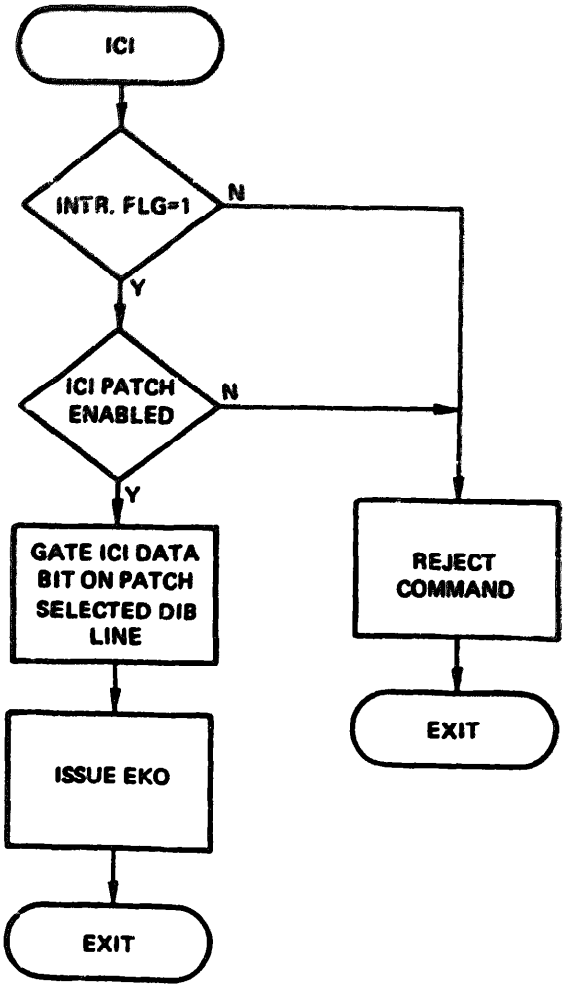
ICI. The ICI instruction has the following format

(A indicates high order address bits)

	Word 1				Word 2
		k-field	o-field	Device Address	Reject Address
Bit	0 1 2 3	4 5 6	7 8 9	1 1 1 1 1 1 0 1 2 3 4 5	1 1 1 1 1 1 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5
	0 0 1 0	1 0 0	0 0 0	A A A A A A	R R R R R R R R R R R R R R

The ICI instruction causes a plugboard selected input line to the processor to go true. When any or all interrupts are connected as common interrupts, the ICI instruction is used to determine the identification of the particular device and the interrupt pending service. The common interrupt word, selected by the patchboard in the controller, is loaded into the A register.

The operational flow of the ICI instruction execution is depicted in the following flow chart.



RDS. The RDS instruction has the following format.

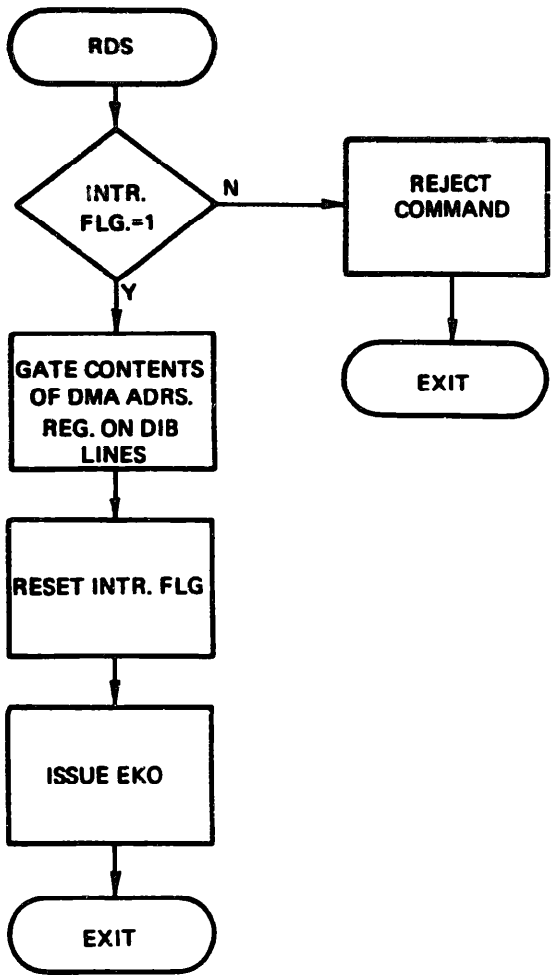
(A indicates Device Address)

(R indicates Reject Address)

	Word 1																Word 2															
					k-field			o-field			Device Address						Reject Address																
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	0	1	0	0	1	1	0	0	0	A	A	A	A	A	A	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

The RDS instruction loads the controller major status word into the A register of the IS/1000 processor. At the same time the instruction resets the interrupt flip-flop. The instruction is rejected if the interrupt is reset.

The operational flow of the execution of the RDS instruction is depicted in the following flow chart.



Packet Derived Commands. The following set of commands is derived from the op code of the first word of the packet. (Refer to Packet Description for exact coding information for each command.)

- Read Data.
- Write Data
- Read Status.
- Seek Cylinder/Track.
- Format Track.
- Read Track Descriptor.
- Verify Data.
- Restore Heads.
- Link Operation.

READ. The Read command causes data to be read from the disk pack in the addressed drive by the selected head, beginning at the specified record and cylinder, after which the data is transmitted to the IS/1000 memory. At the receipt of the read command the controller translates the continuous binary address into the desired cylinder, head and record addresses, performs a seek to the specified cylinder, activates the specified head, starts reading, and transmits the data read from the specified record(s) to the IS/1000 processor. During reading, the track header bytes of each record being read must agree with those in the controller registers, before the data can be accepted by the I/O buffer. A DMA request is generated and the data word is stored in the IS/1000 memory under DMA control. The controller compares the cyclic redundancy check word being read from the disk against the cyclic redundancy check word generated from the home address, header and data area just read. If the comparison shows data congruency and the number of words to be transferred is zero, the controller terminates. When either, the Terminate or the Gated Attention condition is set, an interrupt is generated if enabled under program control.

If the number of words to be transferred is not equal to zero, then the word-transfer counter is decremented by one for each word transfer until 173 data words have been transferred. The record address is then incremented, and as soon as record coincidence occurs, the operation is repeated from that point. If, after the last record on the track has been read, the word count is not zero, the head address is incremented and the read operation continues. When the last record of the last track in a given cylinder, has been read, the controller will:

- Set the record count to one.
- Set the head address to zero.
- Increment the cylinder address.
- Execute a seek operation.

When the disk drive completes the seek, the controller resumes the read operation. No delays are encountered during record-to-record and head-to-head transitions, but a 25 ms delay occurs during cylinder-to-cylinder transitions, due to the inherent time losses incurred through the combined factors of cylinder-to-cylinder positioning time.

WRITE. The Write command causes data to be transmitted from the IS/1000 memory to the disk drive, where it is written onto the disk pack in the addressed drive by the selected head, beginning at the specified record and cyclinder. At the receipt of the Write command the controller translates the continuous binary address into the desired cylinder, head and record addresses, performs a seek to the specified cylinder, activates the specified head, and starts reading to locate the correct sector. When the desired sector has been located the data received from the IS/1000 processor memory is written. The controller generates a cyclic redundancy check character (CRC) from the home address, header and data being written, and at the end of the record writes the CRC behind the last data bit. When the number of words to be written is reduced to zero, the controller terminates. When either, the Terminate or the Gated Attention conditions are met, an interrupt is generated.

If the number of words to be written is not equal to zero, the word-transfer counter is decremented by one for each word transfer until 173 data words have been transferred. The record address is then incremented and as soon as record coincidence occurs, the operation is repeated from that point. If, after the last record has been written onto the track, the word count is not zero, the head address is incremented and the write operation continues. When data has been written into the last record of the last track in a given cylinder, the controller will:

- Set the record count to one.
- Set the head address to zero.
- Increment the cylinder address.
- Execute a seek operation.

When the disk drive completes the seek, the controller resumes the write operation. No delays are encountered during record-to-record and head-to-head transitions, but a 25 ms delay occurs during cylinder-to-cylinder transitions, due to the inherent time losses incurred through the combined factors of radial head displacement and disk rotation.

READ STATUS. The Read Status command transmits the controller status to the IS/1000 memory in the form of seven status words, as follows:

- Status Word 1 - Major Status.
- Status Word 2 - Minor Status.
- Status Word 3 - Number of words or sectors that have not been transferred.

- Status Word 4 - DMA address of last word transferred at termination of operation before Read Status.
- Status Word 5 - Link address of the last packet control word of the previous operation.
- Status Word 6 - Bits 7 through 15: cylinder address.
- Status Word 7 - Bits 3 through 7: head address. Bits 11 through 15: sector address.

An interpretation of the sixteen bits of the major status word is given in Table 2-4. An interpretation of the sixteen bits of the minor status word is given in Table 2-5.

SEEK. Through the Seek command the controller directs the drive to position the heads at the cylinder specified by the record address in the operation control word. The controller normally goes busy long enough to fetch the operation control words from memory and then issues the Seek command to the selected drive, after which the controller initiates a termination sequence. If the drive is busy, the controller delays issuance of the Seek command until the drive becomes ready.

Simultaneous Seek Operations - The controller provides the facility for performing multiple seek operations simultaneously. The controller is busy for less than one ms during a Seek command, while the selected drive may be busy for up to 135 ms during execution of the Seek command. Therefore, after a Seek command has been issued to one drive, another drive can be selected and caused to seek. This process can be continued until all drives are seeking. The first drive to become ready then sets the Gated Attention common interrupt.

FORMAT TRACK. The Format Track command is used to prepare a track of the disk pack to enable standardized data operations within a GTE/IS, or compatible, magnetic disk system, by directing the drive to write the track format on the specified track. For a description of the track format, see under Data Organization in this section.

The Format Track OP CODE is terminated with a Controller Alert, or Invalid Command, when the Format Protect switch on the drive interface card cage is in the PROTECT position. (The Format Protect switch can be accessed by opening the cabinet door).

During the Format Track command, the controller converts the specified binary record address to the appropriate cylinder and head addresses, performs a seek operation to the desired cylinder, activates the correct head, then writes the track format with data sent from the IS/1000 memory, as follows:

- Sync byte and bytes 0 through 4 of the Home Address (Figure 2-17, a).
- Sync byte and bytes 0 through 8 of the Track Descriptor Record Header (Figure 2-17, b).
- Sync byte and bytes 0 through 7 of the Track Descriptor Data Area (Figure 2-17, c).

Table 2-4. Major Status Word

Bit	Status	Description
0	Controller Alert	An abnormal condition occurred during the execution of the last command. This bit is the inclusive OR output of Minor Status bits 0, 1, 2, 3, 4, 5 and 10.
1	Controller Busy	The controller is busy executing a command and cannot accept another.
2	Format Protect	All format commands are rejected because the Format Protect switch is in the Protect position.
3	Selected Drive Busy	The selected drive is busy executing a seek or a restore/recalibrate operation.
4	Drive 7 Attention	Bits 4 through 11 specify that the specified disk has an attention condition. An attention condition results from either of the following: a. The drive has completed a Seek operation. b. The drive has failed to complete a Seek operation (Seek Incomplete). c. The drive has completed a Restore operation. d. The drive has been powered up and is ready. Attention conditions a, c and d can be reset by any drive command. Attention condition 6 (Seek Incomplete) can only be reset by a Restore Command.
5	Drive 6 Attention	
6	Drive 5 Attention	
7	Drive 4 Attention	
8	Drive 3 Attention	
9	Drive 2 Attention	
10	Drive 1 Attention	
11	Drive 0 Attention	
12	Selected Drive Alert	An abnormal condition exists in the selected disk drive. This bit is the inclusive OR output of Minor Status bits 12, 13, 14 and 15.
13	Double Track	This bit indicates that the disk system is configured for processing disk packs of 406 cylinders.
14	Gated Attention	An attention condition exists in one or more of the disk drives. This bit is set when one or more of the disk drive's attention become active. This bit is reset when the Major Status is interrogated by an RDS Command.
15	Terminate	The controller has completed an operation. This bit is set when the controller goes Not Busy. This bit is reset when the Major Status is interrogated by an RDS command.

Table 2-5. Minor Status Word (Sheet 1 of 2)

Bit	Status	Description
0	Data Error	This bit indicates that the regenerated Cyclic Redundancy Check byte does not compare with those read from the disk pack. Multiple record read operations are terminated upon detection of the error. When bit 11, Header Verify Error, is also set, this bit indicates that the Cyclic Redundancy Check was on the header. *) See note for reset information.
1	Invalid Address	The instruction contained a non-existent track address. *) See note for reset information.
2	Rate Error	Indicates that the processor either did not provide a data word in time to maintain continuity during a write operation, or did not accept a data word in time to prevent overflow during a read operation. If this condition occurs during a write operation, the controller writes the remainder of the record, writes the Cyclic Redundancy Check bytes, then terminates the operation. If the condition occurs during a read operation, the controller continues to read the remainder of the record, checks the Cyclic Redundancy Check bytes, then terminates the operation. *) See note for reset information.
3	Flag Verify Error	During the execution of a read or write operation the Track Flag bits read do not match those in the Flag Register. The operation is terminated. *) See note for reset information.
4	Header Verify Error	This bit indicates that during the execution of a read or write command a valid header for the specified record could not be found within two revolutions of the disk, or that the header had a cyclic check error. The operation is terminated upon detection of the error. Reasons for this condition could be a dirty or damaged disk surface or a positioning failure of the read/write heads. *) See note for reset information.
5	End of Pack	During multiple record read or write operations, an attempt has been made to read or write beyond the last cylinder of the disk pack. *) See note for reset information.

Table 2-5. Minor Status Word (Sheet 2 of 2)

Bit	Status	Description
6	Last Flag Bit	The last track flag bits read from a track header during a read or write operation. If the Flag Verify Error bit is set (Bit 3), then these bits may be examined to see how the track is actually flagged.
7	Last Flag Bit	
8	Write Current Sense	The selected disk drive is drawing write current.
9	Selected Pack Change	A disk pack change or drive address change has occurred in the selected drive.
10	Invalid Command	In a linked buffer operation when: a. A read command is followed by a write command. b. A write command is followed by a read command c. A format command is issued while the Format Protect switch is up. d. When non-implemented options are called for. e. No restore status follows a seek in complete condition. f. No read status follows a seek incomplete condition. The Invalid Command Status bit sets the Controller Alert status. *) See note for reset information.
11	None	Unused.
12	Drive Selection Error	Either the specified drive is not selected or more than one drive is selected.
13	Selected Seek Incomplete	The selected drive has a Seek Incomplete condition. This condition can be cleared either by a Restore command or by consecutively powering the drive up then down manually.
14	Selected Drive Unsafe	The selected disk drive is unsafe and will not perform any operation. This condition requires operator or maintenance intervention.
15	Select Drive Off Line	The selected disk drive has its Enable/Disable switch in the Disable position.

*) Note: This indicator bit is reset by the following commands: Format Track, Read, Read Track Descriptor, Restore, Seek, Verify and Write.

- Sync byte and bytes 0 through 8 of each Data Record Header (Figure 2-17, b).

- The data areas of all data records are written with an all-ZEROES pattern.

To format the track, the controller requires 93 words from the IS/1000 memory. The first three words specify the Sync byte and the Home Address bytes 0 through 4.

The next five words specify the Sync byte and the Track Descriptor Record Header bytes 0 through 8.

The next five words contain the Ring Sync byte and the Track Descriptor Data Area bytes 0 through 7.

Sixteen sets of five words each specify the Ring Sync bytes and the Data Record Header bytes 0 through 8 for each of the sixteen records on the track.

If the track is to be formatted for IBM compatibility, the core image illustrated in Figure 2-18 is required, and the following parameters must be adhered to:

- If the track is to be formatted as defective, the Track Descriptor Header must contain the cylinder and head number of the alternate track.

- If the track is to be formatted as an alternate track, the Track Descriptor header must contain the cylinder and head number of the defective track which it replaces.

- The flag bits must have the following connotation:

  bit 6 (left bit) - 0 = good track.
  1 = defective track.

  bit 7 (right bit) - 0 = primary track.
  1 = alternate track.

If no IBM compatibility is required, anything may be written in the Track Descriptor Header and Data Area, except for the first byte, which must be written as indicated.

Use of Flag Bits - The track flag bits are used by IBM software systems for the identification of defective and alternate tracks. However, if IBM compatibility is not required, the use and meaning of these bits may be defined by the user and utilized for other purposes, such as read or write protection of the track. Since the track flag bits are compared with the controller flag register before data transfers between the disk and the memory can take place, only tracks with matching flag bits can be accessed. If an attempt is made, the Flag Verify Error status bit is set without data transfers. To access the data, the last flag bits may be extracted from

	0 ——— 15		ADDRESS
HOME ADDRESS	0 0 0 0 1 1 0 1	0 0 0 0 0 ^ F F	n
	0 0 0 0 0 0 0	CYLINDER No.	n+1
	0 0 0 0 0 0 0 0	0 0 0 HEAD No.	n+2
TRACK DESC. HEADER	0 0 0 0 1 0 1 1	0 0 0 0 0 0 F F	n+3
	0 0 0 0 0 0 0	CYLINDER No.	n+4
	0 0 0 0 0 0 0 0	0 0 0 HEAD No.	n+5
	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	n+6
	0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0	n+7
TRACK DESC. DATA FIELD	0 0 0 0 1 0 0 1	0 0 0 0 0 0 F F	n+8
	0 0 0 0 0 0 0	CYLINDER No.	n+9
	0 0 0 0 0 0 0 0	0 0 0 HEAD No.	n+10
	0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0	n+11
	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	n+12
DATA RECORD HEADER	0 0 0 0 1 1 1 0	* 0 0 0 0 0 F F	n+13
	0 0 0 0 0 0 0	CYLINDER No.	n+14
	0 0 0 0 0 0 0 0	0 0 0 HEAD No.	n+15
	0 0 0 SECTOR No.	0 0 0 0 0 0 0 0	n+16
	0 0 0 0 0 0 0 1	0 1 0 1 1 0 1 0	n+17

The 5 data record header words are accepted 15 more times with the record number being advanced one count each time.

*This bit is ONE on odd numbered records, ZERO on even numbered records.

F = Flag bit.

Cylinder = 0-202 (model 114 disk drive).
0-405 (model 215 disk drive).

Head No. = 0-19

Sector No. = 1-16

Figure 2-18. Format Core Image for IBM Compatibility

the Minor Status word and then loaded into the controller flag register using the Select command.

READ TRACK DESCRIPTOR. The Read Track Descriptor Command causes the five words (nine bytes) of the header, and the four data words of the specified track descriptor record to be read. The controller converts the binary record address to cylinder address, head address, and record zero, performs a seek operation, then proceeds to read. The track flag bits of the record must agree with the controller's Flag register contents before data is read. Upon completion the Termination interrupt is activated.

VERIFY. The Verify operation is intended to check sectors after a write operation. The third operation control word of the packet specifying the Verify command, specifies the number of sectors instead of number of words to be operated on. The controller converts the binary address to the desired cylinder address, head address and record number, performs a seek, then reads. The Track Flag bits of each record must agree with those in the controller Flag register. The controller compares the cyclic redundancy check word being read from the disk against the cyclic redundancy check word it generates from the home address, header and data area read.

RESTORE. The Restore command causes the selected drive to position the heads at cylinder 0. The controller remains busy until the drive has positioned the heads at cylinder 0, then terminates and sets the interrupt.

LINK OPERATION. The Link Operation command is used for command chaining. Linked operations are indicated when bit 0 of the first operation control word of a packet is ONE. Bit 11 of the same control word further defines the linked operation as to whether or not linking of similar read or write operations are indicated, where the sector address is ignored on all but the initial packet. The fifth operation control word specifies the next packet in the chain.

Linked Operations - During linked operations, when the word count is zero, the next packet of five control words is read from memory and the specific operation continues. These linked conditions continue as determined by the software, until a non-linked operation is completed at which time operations cease when the word count becomes zero. The controller continues to end of record, verifies check bytes, updates status and sets terminate interrupt. The recommended method of operation sequences is to terminate all sequences with a linked read status operation so that status has been sent when the interrupt is detected.

Command Rejection. The controller acknowledges acceptance of an instruction by sending an EKO pulse to the processor. If the command is rejected, no EKO pulse is returned. In the latter case, the processor executes a simulated BSP (branch and store contents of P register) instruction to the memory location specified by the second word of the rejected instruction. Under the following conditions a command will be rejected and no EKO acknowledgement signal issued:

- The controller is busy. When the controller is busy it will reject all commands except EDF RST.
- An EDF STR command has been given but the EDF STR enable flag is not set.
- An ICI or RDS command has been given but no interrupt flag is set.

Timing Considerations. The data word transfer rate required by the controller is approximately 156 kHz. The controller has a 40-byte buffer register and must be serviced within approximately 40 us after a DMA service request. All data transfers will be terminated when a rate error occurs. If data transfers are terminated using the EDF RST instruction, it will clear any pending DMA request and inhibit any further requests. During linked buffer operations (indicated by bit 11 of control word 1 being ONE), rate errors can occur if more than three buffers are linked within one sector.

2.4.5 Firmware

The firmware is the microcoded implementation of the logic controlling the sequencing, timing and monitoring of all disk drive functions in response to IS/1000 commands.

Physically, the firmware consists of four PROM modules of 512 x 8 bits each. This provides 1,024 x 16 bits of memory capacity required to store the micro program. The micro program itself consists of fifteen subroutines which are used on a shared basis for the implementation of the eight disk operation directing commands. For the sequences of usage of these subroutines by each of the eight commands refer to the flow diagrams in Appendix A.

2.4.5.1 Subroutines

RESET. Upon issuance of an EDF RST command by the IS/1000 processor, the EDC sets its program counter to zero. The program counter contents set to zero, calls in the Reset subroutine. The Reset subroutine:

1. Clears memory location $30 through $3F, setting them to zero.
2. Resets the device interface
3. Resets the CMD flag.
4. Sets the Start Enable flag.

IDLE. In the idle state, the controller looks for the CMD flag or for an interrupt (Gated Attention). When either is found, the controller terminates the idle subroutine loop and calls in the Start subroutine. The Idle subroutine sends an interrupt to the IS/1000 after updating the last Selected-Drive status.

START. The Start subroutine causes five control words to be read out of the processor memory and to be transferred to the PDC via the DMA. The five control words specify and define the disk operations to be performed. During the Start subroutine, the disk drive is selected and its status checked.

ADDRESS CONVERT. The Address Convert (ADCONV) subroutine converts the continuous binary address into cylinder, head and sector addresses, which are then stored in the File register. The ADCONV subroutine also checks for invalid commands and/or invalid option callouts.

SEEK. The Seek subroutine controls the seek operation in the disk drive. The Seek subroutine furnishes Seek-start, cylinder and head information. The Seek subroutine also checks for invalid addresses.

READ, WRITE, VERIFY. The Read/Write/Verify (RWV) subroutine searches for the selected data record header for read, write or verify commands. The RWV subroutine is called in after a head count or sector count increment.

If this header can not be found in two revolutions, i.e., within two index marks a header verify error is reported as minor status, a controller alert as major status and the invalid command status is set for a zero-word count.

READ. The read subroutine which is a part of the read instruction, searches for the data record header for a maximum time of 358 us. If it is not found within that time a data error status is reported and the command is terminated. After the header is found the data is transferred from the FIFO to the DMA data register. If the word count is less than 173, the controller continues to read the sector and checks the CRC, but suppresses any write operation when the word count equals zero. If the word count is greater than a sector, the sector, head, or cylinder count will be incremented. The next subroutine sequence will be either RWV, Increment HD-RWV, or Seek-RWV, before returning to the Read Subroutine.

WRITE. This subroutine writes part of the gaps, starting at about half way the lead area, before writing the data. If the word count is less than a full sector, and no linked buffers are specified, the sector will be filled with ZEROS until the CRC is written. If the word count is greater than a sector, the sector count is either incremented and the RWV subroutine executed, or the head count is incremented and the RWV executed. If the last sector of the cylinder is selected, then the write data will cause the cylinder count to be incremented by interspersing a Seek subroutine, after which the Write subroutine finishes the word count. When the word count is zero the command is checked to see if it is a linked buffer operation, in which case the program branches to the NCP part of the Start subroutine.

VERIFY. The Verify subroutine uses parts of the read subroutine since they are functionally similar. The search for the data record header is shared with the read subroutine, after which data is taken from the FIFO and the CRC character is generated, but no data is stored into memory. If the sector count is more than one, and the CRC is correct, either the sector count, the head count, or the cylinder count is incremented. The Verify subroutine is repeated for the next sector.

FORMAT. The format subroutine operates on one complete track only. The subroutine writes Gap 1 immediately after the index mark, and follows it with the home address, gap 2, the track descriptor header, another gap 2, and a track descriptor data record. The subroutine then writes a gap 2, a data record header, a gap 2, data record with all ZEROs and a gap 3, repeating this until 16 data records are formatted. The remainder of the track is filled with ONEs until the next index marker is encountered.

READ TRACK DESCRIPTOR. The Read Track Descriptor (RTD) subroutine is executed after a seek subroutine, as part of the RTD command. After detection of an index mark, the home address is read and verified. The track descriptor header, which consists of 5 words, is then read and transferred into the IS/1000 memory via DMA. The track descriptor data area is next read into the IS/1000 memory. If the header information does not compare, a minor status header verify error is reported. If a CRC error occurs, then both data error and header VFY error flags are reported as minor status.

READ STATUS. The Read status (RDSTAT) subroutine updates the gated attention part of the first major status word. The RDSTAT subroutine then updates the selected drive, assembles major and minor status, word count from previous instruction, DMA address from the previous instruction, link address from the previous instruction, last cylinder address, last head and sector information, and sends this to the IS/1000 processor via the DMA. The major and minor status are then reset.

RESTORE. The Restore subroutine activates Data Bus 6 and the control line to the selected drive with the proper timing.

TERMINATE. The Terminate (TERM) subroutine:

1. checks for drive interrupts (gated attention)
2. updates selected drive status
3. updates Memory Control Words
4. checks for Link Command
5. Sets Major Status into Address Register
6. Sets Interrupt and Terminate Status
7. Resets Disk Interface
8. Set Start Enable
9. Calls in the Idle subroutine.

DIAGNOSTIC. The Diagnostic (DIAG) subroutine is called in upon detection of the DMA address being zero after an EOF start. This subroutine checks the FIFO, the CRC register and whether the DMA address register can be incremented. The Error status or Ending status is found in the DMA address register after the interrupt is raised.

2.4.5.2 Command Implementation

The controller executes the following six basic operations, and any combination thereof, upon command of the processor:

- **Standby (idle state)**
- **Select a disk drive.**
- **Position the heads at a specific location of the disk pack, select a head and locate the portion of the track specified by the processor.**
- **Write a particular record as directed by the processor.**
- **Read a particular record as desired by theprocessor.**
- **Transfer data or status information to the processor.**

On the device side, the controller directs the selected disk drive to perform any of the above operations via the device interface by activating the Bus and Tag lines. Each instruction is implemented when a Tag line is active simultaneiously with a Bus line. The command coding for the three Tag lines, terms CNTRL-, STCYL- and STHED-, and the nine Bus lines, terms DBUS0- thru DBUS8-, is given in Table 2-6. Note that term DBUS0- is only used in system configurations using the model 215.

On the processor side, this is accomplished through decoding of the control words obtained from the processor memory via the DMA. The decoded function then activates the proper subroutines of the micro program. To facilitate the exchanges of data between the PDC and the DCI logic units, dedicated memory locations and special registers are provided.

On the DCI side, these are locations $30 through $4F. Locations $30 through $3F are 8-bit memory registers used for storage of ***control and status words by the micro program (refer to Tables*** 2-7, 2-8, and 2-9, for address and content interpretation). Refer to Table 2-10 for a description of functions $40 through 4F.

On the processor side, these are locations $00 through $0F. Refer to tables 2-11 and 2-12 for address and content interpretations.

Table 2-6. Drive Command Implementation

BUS Lines		TAG Lines		
Model 114	Models 213/215	CNTRL-	STCYL-	STHED-
		RESULTANT FUNCTION		
	DBUS0-		Cylinder 256	
DBUS0-	DBUS1-	Write Gate	Cylinder 128	
DBUS1-	DBUS2-	Read Gate	Cylinder 64	
DBUS2-	DBUS3-	Seek Status	Cylinder 32	
DBUS3-	DBUS4-	Reset Head Register	Cylinder 16	Head Address 16
DBUS4-	DBUS5-	Erase Gate	Cylinder 8	Head Address 8
DBUS5-	DBUS6-	Select Head	Cylinder 4	Head Address 4
DBUS6-	DBUS7-	Return to 000	Cylinder 2	Head Address 2
DBUS7-	DBUS8-	Head Advance	Cylinder 1	Head Address 1

Table 2-7. Dedicated Memory Locations $30 - $3F in Controller

Location	Function
$30-$31	CTL Word 1 Upper - CTL Word 1 Lower
$33-$34	LK ADR U1 - LK ADR L1
$35-$36	LK ADR U2 - LK ADR L2
$37	Relative Addr. for Instruction Decode
$38	Flag
$39	Gated Attn
$3A	Major Status Upper
$3B	Major Status Lower
$3C	Minor Status Upper
$3D	Minor Status Lower
$3E-$3F	CTL Word 2 Upper - CTL Word 2 Lower

Table 2-8. Input Function $30 - $4F

IOD Bit	Function							
	$30-3F	$41	$42	$43	$44	$45	$46	$47
0	MEM 0	OR	ATTEN 7	WCSEN	FIFO 0	$\overline{\text{SYNC}}$	CR00	CR08
1	MEM 1	IR	ATTEN 6	PRCHG	FIFO 1	AMDET	CR01	CR09
2	MEM 2	INDEX	ATTEN 5	SWFMTP	FIFO 2		CR02	CR10
3	MEM 3	RATER	ATTEN 4	BUSY	FIFO 3		CR03	CR11
4	MEM 4	FIFO8	ATTEN 3	DSERR	FIFO 4		CR04	CR12
5	MEM 5	DDRV	ATTEN 2	SKINC	FIFO 5		CR05	CR13
6	MEM 6	SIXST	ATTEN 1	UNSAF	FIFO 6	SIXST	CR06	CR14
7	MEM 7	ENDCYL	ATTEN 0	$\overline{\text{ONLIN}}$	FIFO 7		CR07	CR15

IOD Bit	$48	$49	$4A	$4B	$4C	$4D	$4E	$4F
0								
1								
2	u	u	u	u	u	u	u	u
3	n	n	n	n	n	n	n	n
4	d	d	d	d	d	d	d	d
5	e	e	e	e	e	e	e	e
6	f	f	f	f	f	f	f	f
7	i	i	i	i	i	i	i	i
	n	n	n	n	n	n	n	n
	e	e	e	e	e	e	e	e
	d	d	d	d	d	d	d	d

Table 2-9. Location $30 - $4F Output Function $30 - $4F

IOD Bit	Function							
	$30-3F	$41	$42	$43	$44	$45	$46	$47
0	MEM 0		DBUS 1		FIFO 0	FIFO 0,8		AMDET
1	MEM 1		DBUS 2		FIFO 1	FIFO 1,8		ENIDX
2	MEM 2		DBUS 3		FIFO 2	FIFO 2,8		
3	MEM 3		DBUS 4		FIFO 3	FIFO 3,8		
4	MEM 4		DBUS 5	CNTRL	FIFO 4	FIFO 4,8		RDHA
5	MEM 5	FDEVA4	DBUS 6	STHED	FIFO 5	FIFO 5,8		RDTD
6	MEM 6	FDEVA2	DBUS 7	STCYL	FIFO 6	FIFO 6,8		RDDA
7	MEM 7	FEDVA1	DBUS 8		FIFO 7	FIFO 7,8	DBUS 0	RDRH
IOD Bit	$48	$49	$4A	$4B	$4C	$4D	$4E	$4F
0		RESET FIFO	RESET STATUS		RESET EFIFO F/F			SET CRC
1								
2								
3								
4								
5								
6								
7	WRITE							

Table 2-10. Location $40 - $4F Function Description (Sheet 1 of 2)

Location	Function
DA 40	Not used
DA 41	Output is the selected drive binary address.
DA 41	Input is controller status (CTLS) as follows: OR - FIFO Output Ready. IR - FIFO Input Ready. INDEX - Index Pulse. RATER - Rate Error. DDRV - Single or Double Density Drive (Patch). SIXST - Second Index has occurred FIFO8 - FIFO Output Bit 8.
DA 42	Output is drive bus signal.
DA 42	Input is gated attentions from drives.
DA 43	Output is for selecting drive tag line CNTRL, STCYL or STHED.
DA 43	Input is drive status and is defined below. WCSEN - Write Current Sensed. PKCHG - Pack Change. SWFMTP - Format Protect Selected. BUSY - Drive Busy. DSERR - Disk Select Error. SKINC - Seek Incomplete. UNSAF - Drive Unsafe. ONLIN - Drive Not Online.
* DA 44	Input reads FIFO output bits zero thru seven.

* DA 44 and DA 45 outputs are used for loading FIFO bits zero thru seven and in addition DA 45 causes bit 8 to be loaded with a ONE which is used to cause an address mark to be written on the disk pack.

Table 2-10. Location $40 - $4F Function Description (Sheet 2 of 2)

Location	Function
* DA 45	Inputs are assigned as follows: SYNC - used for VFO Phase SYNC. AMDET - True when looking for address mark. SIXST - 2 index, the second index has occurred.
DA 46	Output at B7 is double density drive MSB signal bus line.
DA 46	Input is the upper CRC register.
DA 47	Output consists of the following disk interface controls: AMDET - Enable address mark detect. ENIDX - Enable index. RDDA - Read data. RDHA - Read home address. RDRH - Read data record header. RDTD - Read track descriptor.
DA 47	Input is the lower CRC register.
DA 48	Output at B7 = "1" is the control write mode. B7 = "0" is read mode.
DA 49	Output resets the FIFO.
DA 4A	Output resets status.
DA 4B	Not used
DA 4C	Output resets enable FIFO F/F.
DA 4D	Not used
DA 4E	Not used
DA 4F	Output sets CRC register.

* DA 44 and DA 45 outputs are used for loading FIFO bits zero thru seven and in addition DA 45 causes bit 8 to be loaded with a ONE which is used to cause an address mark to be written on the disk pack.

Table 2-11. Dedicated Memory Locations $00 - $0F in Controller

Location	Function	Location	Function
F0	} Word 1	F8	
F1		F9	
F2	Flag	F10	
F3	Cyl. Adr. Upper	F11	
F4	Cyl. Adr. Lower	F12	Word Cnt..- Sector
F5	Head Addr.	F13	
F6	Sector Adr.	F14	Word Cnt. } Word 4
F7		F15	Word Cnt. }

Table 2-12. Input/Output Function $00 - $0F

Location	Output Function	Input Function
00	Load ARu	Read ARu DMA
01	Load ARl & Reset ARu	Read ARl MAJ
02	Load DRu	Read DRu
03	Load DRl	Read DRl
04	Incr. AR	
05	Load "CMD FLG" @ IOD0	
06	Load "STRENB" @ IOD1	
07	Set IS/1000 Interrupt	Read Status Register
09	DMA Start, Write Upper Byte	
0A	DMA Start, Write Lower Byte	
0B	DMA Start, Write Both Bytes	
0F	DMA Start, Read	

2.4.6 Interfaces

The following paragraphs describe the subsystem interface that interconnects the controller in the magnetic disk subsystem, to the disk drives under its control. The system interface is only described where it is essential to the overall understanding of the controller's functions, i.e., primarily the signal line designations between controller and processor. For more complete and exacting information on the system interface linking the subsystem to the processor, refer to the GTE/IS publication H0011, titled IS/1000 I/O Interface Reference Manual

Both interfaces are shown in Figure 2-19. Note that the IS/1000 I/O cabling is actually internal to the chassis in which the controller is housed. The signal mnemonics of the system interface as applicable for the disk subsystem, are shown in Figure 2-20.

As can be seen from Figure 2-19, the controller-to-device(s) cabling consists of three types of cables, a Signal cable, as many DC cables as there are drives in the system, and an AC cable.

2.4.6.1 Signal Cable

The signal cable connects the disk drives serially in daisy-chain fashion to the controller and must be terminated in the last disk drive. The maximum combined length in a disk subsystem of all Signal Cable segments, must not exceed 100 feet. The last drive in the subsystem is terminated with a terminator.

Signal mnemonics are shown in Figure 2-20, while the connector pin assignments are given in Table 4-9 in section 4. Following is a brief description of each of the signal lines.

DBUSX-. The DBUS0- through DBUS7- lines (and DBUS6- line in the model 215) are time shared bus lines that serve to identify certain functions depending upon which of three tag lines is active at the time. Only one tag line can be active at any one time. Table 2-6 lists the various functions the bus lines can identify.

CNTRL-. Term CNTRL- is a tag line that, when active, identifies the DBUSX- lines as control signals (see Table 2-6). Simultaneously activating one or more of the DBUSX- signals determines which operation(s) is or are to be performed.

STCYL-. Term STCYL- is a tag line that, when active, identifies the DBUSX- lines as the cylinder address to be accessed (see Table 2-6). Simultaneously activating one or more of the DBUSX- signals determines to which cylinder the heads are moved during the ensuing seek operation.

STHED-. Term STHED- is a tag line that, when active, identifies the DBUSX- lines as the head to be selected, i.e., the track number to be accessed (see Table 2-6). Simultaneously activating one or more of the DBUSX- signals determines which track in a certain cylinder is read from or written upon.

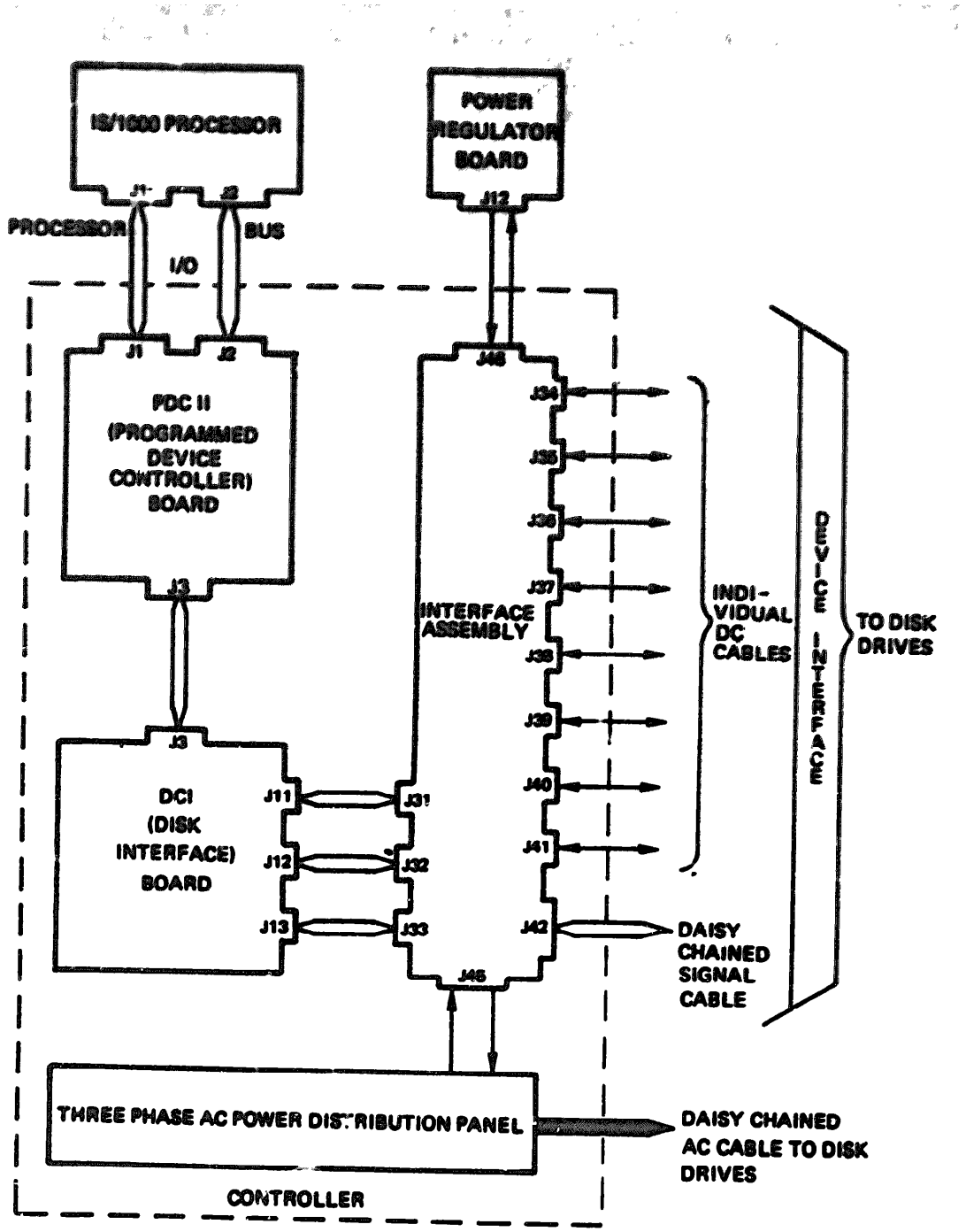


Figure 2-19. IS/1000 Magnetic Disk System Interface

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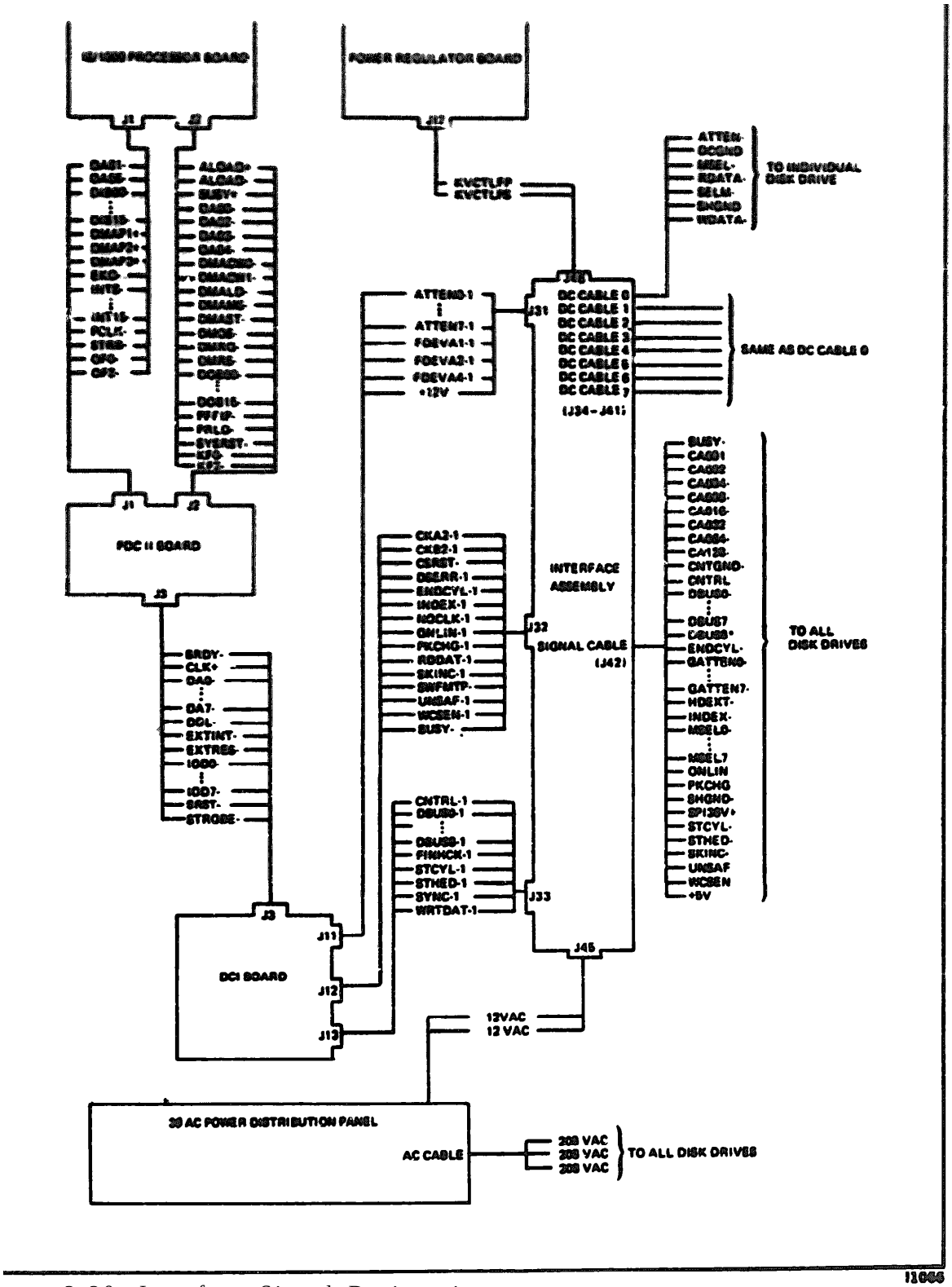

Figure 2-20. Interface Signal Designations

BUSY-. The BUSY- signal when active, indicates that the selected drive is in the process of executing a seek or restore operation.

EXDCYL-. The EXDCYL- signal when active, indicates that during a read or write operation the head address has progressed from 19 to 20, i.e., a non-existing track is being specified.

HDEXT-. The HDEXT- signal when active, indicates that the heads are extended into the disk pack. The HDEXT- line is used for monitoring purposes during power-down sequences. During a power-down sequence, the dc voltages and control signals to the drive can not be removed until the last Heads-Extended switch has opened, thus deactivating the HDEXT- line. This signifies that the heads are unloaded, i.e., out of the disk pack.

INDEX-. The INDEX- pulse indicates the beginning and subsequant ending of all the tracks in the disk pack. The INDEX- pulse is generated at every complete revolution of the disk pack by the index gap in the protective bottom disk of the disk pack passing the index transducer. At the operating rotational speed of 2400 rpm, the pulse frequency is 40 Hz. Pulse length is 70 $\pm$ 30 us while time duration between pulses is 25 ms.

ONLIN-. Term ONLIN- indicates that in the selected drive the disk pack is rotating at full operating speed, the heads are extended and seek, read or write operations can commence.

PKCHG-. Term PKCHG- indicates that the disk pack has been changed or that the address of the disk drive has been altered.

UNSAF-. The UNSAF- line is activated when any of the DC operating voltages falls below the tolerance specified level. Term UNSAF- active causes the immediate extraction of the heads from the disk pack.

SKINC-. The SKINC- line indicates that the seek operation was not completed within one second from the time the seek command was issued. A restore command must be executed following a SKINC- condition.

WCSEN-. Term WCSEN- active indicates the sensing of write current and thus signifies that the disk drive is performing a write operation. The write current sense line becomes active within 10 us from the leading edge of write gate.

+5V. The +5V line is used by the terminator for the termination of the signal lines.

SPI36V+. The SPI36V+ line is used for power on sequencing purposes. The +36 Vdc sequence pick in signal is generated by the first drive with ac power on.

CNTGD-. The CNTGD- line is used during power down sequencing. The controlled ground line is normally grounded and holds the disk drive power sequencing relays energized. Opening this line deenergizes the relays, causing immediate head retraction and initiating a power down sequence.

2.4.6.2 DC Cable

The dc cable connects the disk drives parallel in radial fashion to the controller. The maximum length of each cable must not exceed 50 feet.

Signal mnemonics are shown in Figure 2-20, while the connector pin assignments are given in Table 4-10 in section 4. Following is a brief description of the signal lines.

ATTNX-. The gated attention line indicates that either a power on sequence, a seek operation, or a restore (head return to cylinder 000) operation has been completed.

MSELX-. The module select line is used to gate signal lines to the proper (selected) drive.

RDATA-. The read data line is used to transfer serial data read from the disk pack, from the selected disk drive to the disk controller.

SELMX-. The selected module line indicates that the drive has been selected, and provides the gating for the selected read data line.

WDATA-. The write data line is used to transfer serial data to be written on the disk pack, from the controller to the selected disk drive.

2.4.6.3 AC Cable

To enable the sequencing of power turn-on and turn-off, the disk drives derive their ac power from the controller in serial/ consecutive fashion. The maximum combined length in a subsystem, of all ac cable segments must not exceed 50 feet. The ac power provided is three phase 208/230 Vac. The phases are rotated from drive to drive to balance the power loading. For connector pin assignments, refer to Table 4-11.

2.4.7 Theory of Operation

The sole purpose of the magnetic disk subsystem is to store information on a disk pack so that information can be recovered and utilized at a later time. To accomplish this function, the subsystem needs electrical power. The controller derives this power directly from a suitable power source; the drives in the subsystem obtain their electrical power from the power distribution panel (PDP). In the case of a single disk drive, this may simply consist of applying the ac power to the multiple drive subsystem; however, the powering up process of the drives must be controlled and sequenced to avoid sudden excessive power surges. Power sequencing logic is therefore incorporated into the power circuits, establishing definite power-on and power-off sequences.

As part of the power up process, the disk drive is initialized through a first seek operation, which places the heads at cylinder 000. A programmed seek operation can then direct the heads to any desired cylinder of the disk pack.

In a particular cylinder, a desired track can be written upon or read from, by selecting the corresponding head and specifying a write or a read operation, respectively.

Each track is not only segmented for a fixed format recording mode, but is also made unique, hence identifiable, amongst all other tracks in the disk pack, during the write format operation.

Format and data can be verified, i.e., no data transfers to the processor take place, during a read verify operation, while status can be checked during a read status operation.

In the event of a logic or program function error, a means to reestablish initial conditions is provided through the restore operation, which is initiated with the EDF RST instruction. In the event of a failure or malfunction, in which data stored on the disk pack is in danger of being destroyed or physical damage to disk pack and heads may result, the heads are automatically removed from the disk pack and retracted.

The functional modes of operation in a magnetic disk subsystem therefore are:

1. Power sequencing. Power sequencing is a combined function of the controller and the disk drive(s). The two power sequencing modes are:

   - Power-up sequence.
   - Power-down sequence.

2. Seek operation. There are three types of seek operations, as follows:

   - first seek
   - programmed seek
   - restore

   The first seek operation in an automatic, self-initiated function of the disk drive, while the programmed seek is a processor initiated, controller directed operation.

   Recalibration of the heads to home position, i.e., at cylinder 000, is part of the restore operation; it is *controller* initiated but uses the drive's own recalibration logic.

3. **Write. There are two types of write operations, both are processor initiated and controller directed. They are:**
   - **Format (write format)**
   - **Write (write data)**
4. **Read. There are three types of read operations, which are all processor initiated and controller directed. They are:**
   - **Read. (read data).**
   - **Read track descriptor.**
   - **Verify (read without data transfer).**
5. **Restore. The restore operation is a controller initiated operation, which uses some of the disk drive auto-logic. The restore operation resets all logic and positions the heads in the disk drive at cylinder 000.**
6. **Emergency Retract. This is a fully automatic, self-initiated function of the disk drive. In an emergency retract operation, the heads are retracted, i.e., completely withdrawn from the disk pack.**

The eight controller operational modes, aside from the power-up and power-down sequencing, are:

1. **Seek.**
2. **Restore.**
3. **Write.**
4. **Format track.**
5. **Read.**
6. **Read track descriptor.**
7. **Verify.**
8. **Read Status.**

2.4.7.1 Power Sequencing

Power sequencing is the combined function of the controller and the disk drive(s). During the power-on sequence with the Heads Extended line from the drives open (no ground), the controller provides the drives with a ground level by activating the Controlled Ground line, after all voltages have stabilized within tolerance range. This starts the power-up sequence to the first disk drive. The next disk **drive in** line starts up when the disk pack in the previous disk drive has attained 70 percent of its rotational speed. During the Power-off sequence, the controller deactivates the Controlled Ground line to the drives. This starts the power-down sequence in the disk drives. After all drives have retracted their heads, ground is removed from the Heads Extended line of the disk drives. This indicates to the controller that it can turn the dc power off without damage to the drive or the disk pack. Figure 2-21 depicts a timing diagram of the power-up and power-down sequences.

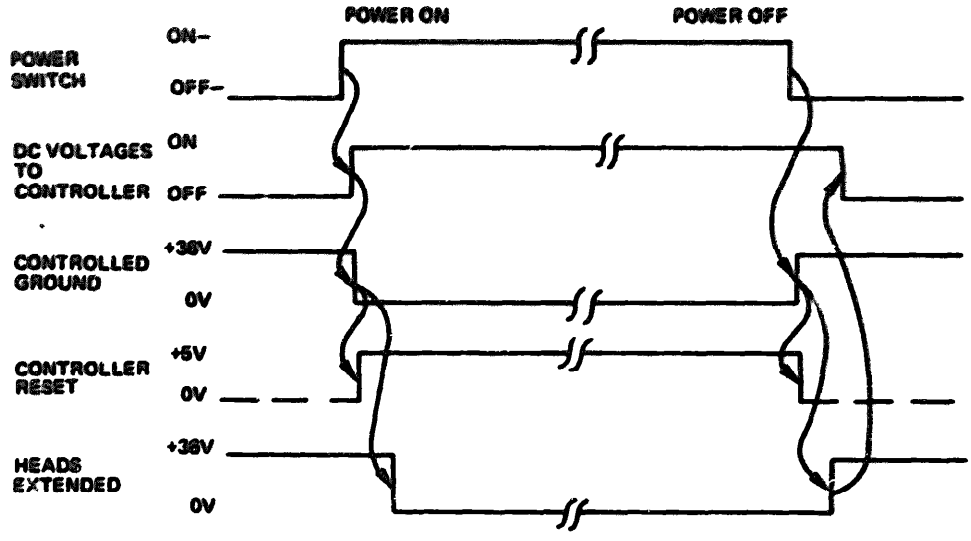

Figure 2-21. Power Up/Power Down Sequences

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Power Sequencing Logic Implementation. The Power sequence card contains the time delay and interlock circuits needed to effect the power-up and power-down sequences. The PSQ card also has its own power supply. A circuit diagram of the circuitry implementing the power sequencing logic, is shown in Eng. Dwg. 300112 of Appendix C. The Power Sequence card is located in slot J3 of the card cage and receives 12 Vac input power from the 30 Vac power panel. A full wave rectifier converts the 12 Vac to the pulsating 15 dc voltage, +15 Vdc (R), used to energize the relays. The +15 Vdc (R) is then filtered to obtain the low ripple dc circuit supply voltage, +15 Vdc (C). Both dc voltages are available whenever the circuit breakers on the AC powr panel are in the ON position. This makes the Power Sequence card independent from the rest of the card cage, which, although containing a +5 Vdc power supply for its circuits, must receive its +15 Vdc from the controller via J44.

Power-on Sequence. To power up a IS/1000 computer system with a magnetic disk subsystem attached, the power switch on the front panel of the IS/1000 must be placed in the ON position. This applies ground to the KVCTL- line which in turn energizes relay K1. This applies ground to the KVCTL+ line, which then turns on the IS/1000 power supplies. This applies power to the controller while the controller reset line, term CSRST-, is held to ground by relay K2.

The energizing of relay K1 through the power switch on the IS/1000 control panel removes ground from the input to the time delay circuit. The 15 second delay time ensures that the power is up and

that the controller and drive interface circuits have stabilized before power is applied to a disk drive. When the delay circuit has timed out, ground is applied to relay K2. The energizing of K2 removes ground from the Controller Reset (CSRST-) and applies ground to the Controlled Ground (WCNTGD-) lines going to all drives.

The +36 Vdc supplied by the first disk drive in the subsystem, is sent to the controller on the signal cable connector pin CM; the +36 Vdc is then jumpered to pin CL to provide the sequence pick voltage for the power sequence circuit of the first disk drive. The +36 Vdc in combination with the controlled ground level, energizes relay KA in the first disk drive, causing the disk drive motor to be started. When the disk pack in the drive reaches 70 percent of its rotational speed, relay KB is energized, which propagates the +36 Vdc to the next disk drive in the subsystem. This process is then repeated for every following drive in the magnetic disk subsystem. This sequential powering up of the disk drives, prevents excessive current surges. As soon as the disk pack in a disk drive has attained operating speed, the drive's head assembly is allowed to move out of its fully retracted position, causing the Heads Extended line, term WHDEXT-, to go true. This in turn causes the Power Interlock circuit to apply ground to the KVCTL+ line, thus locking in the IS/1000 regulator assembly as long as term WHDEXT- is true. This completes the power-up sequence.

Power-off Sequence. A power-off sequence is initiated by placing the power switch on the front panel of the IS/1000 processor, in the OFF position. This removes ground from the KVCTL- line thereby de-energizing relay K1. The de-energizing of K1 interrupts the ground path to line KWCTL+ while simultaneously applying ground to the Time Delay *circuit.* Term KVCTL+ remains low due to the Power Interlock circuit, but when the Time Delay times out, ground is removed from relay K2, de-energizing K2. This deactivates term WCNTGD- going to all disk drives, **thereby** initiating their power down sequences. The de-energizing of K2 also applies ground to line CSRST-, which resets the controller and readies the drive interface circuits for power-off. When all disk drives have fully retracted their heads, they remove ground from the WHDEXT- line. The Power Interlock circuit now removes ground from line KCVCTL+, which then turns off IS/1000 power supplies and subsequently removes power from the controller.

2.4.7.2 Seek Operation

There are two types of seek operations; an initiating or first seek which has as purpose to home the heads in on the first cylinder, and a programmed seek which directs the heads to any cylinder required for access of any desired area on the disk pack. A programmed seek operation is initiated by a seek command. When seeking from one location on the disk pack to another, an address conversion must take place. In the event of a seek error, a restore operation is initiated which positions the heads at home position, i.e., cylinder 000. Also, before any seek operation can be successfully executed, all disk packs used in a magnetic disk subsystem must be formatted strictly according to one format. A disk pack used in the GTE/IS magnetic disk system must be formatted according to the format

given in Figures 2-16 and 2-17. A disk pack is initially formatted during a format operation which is effected through a format command.

First Seek. The first seek operation is an automatic, self-initiated function of the disk drive, consisting of a complete forward motion at low speed from the retracted position of the heads all the way into the disk pack (beyond the last cylinder), until the carriage is stopped by the forward mechanical stop (Crash Stop), immediately followed by a reverse motion to the home position at cylinder 000.

The first seek operation commences when the disk pack in the drive reaches 70 percent of its operating rotational speed. The first seek concludes the power up sequence when it causes the HEAD EXT/RET switches to transfer by moving the heads out of their retracted position. The first seek is completed when the heads are positioned at cylinder 000. At the successful completion of the first seek operation, the disk drive is ready for on-line operations.

Programmed Seek. The programmed seek is a processor initiated, controller directed operation. A programmed seek operation to any desired cylinder is possible when the cylinder address at which the heads in the selected drive are currently positioned, is known. Initially this is the first cylinder (cylinder address 000), later it is the cylinder address where the heads were positioned at after cessation of the last accessing operation. A programmed seek is initiated by a seek command from the processor. The controller then selects the specified disk drive and determines the cylinder and head addresses. The cylinder difference is the difference count between the cylinder to be accessed and the cylinder the heads are at. The Seek Logic is microprogram implemented. The logic flow of the Seek operation is shown in the Seek flow diagram in appendix A. The seek command is coded on the Bus and Tag lines as shown in Table 2-6, and together with the address information, sent to the selected disk drive.

Seek Timing Considerations. The timing inter-relationships, although related through signal interaction, can be classified as follows:

- Those pertaining to disk pack motion, its control and measurement.
- Those pertaining to head movement, its control and measurement.

The operating rotational speed of the disk pack is maintained at 2400 **rpm** ±2 percent. To enable the measurement of this speed at all times, the disk pack's rotation is monitored by electromagnetic means through the use of an index-transducer (see Figure 2-22). **At 2400** rpm, the frequency of ***recurrence*** of the index pulse will be 40 Hz; time duration between index pulses then is 25 ms, while the duration of the index pulse itself is 80 us. The relative positioning of one index pulse with respect to all other index pulses is 18 us.

The time necessary to position the heads in the model 114 from cylinder 000 to cylinder 202 (maximum positioning time), is 65 ms. The time needed to position the heads in the model 215 from cylinder

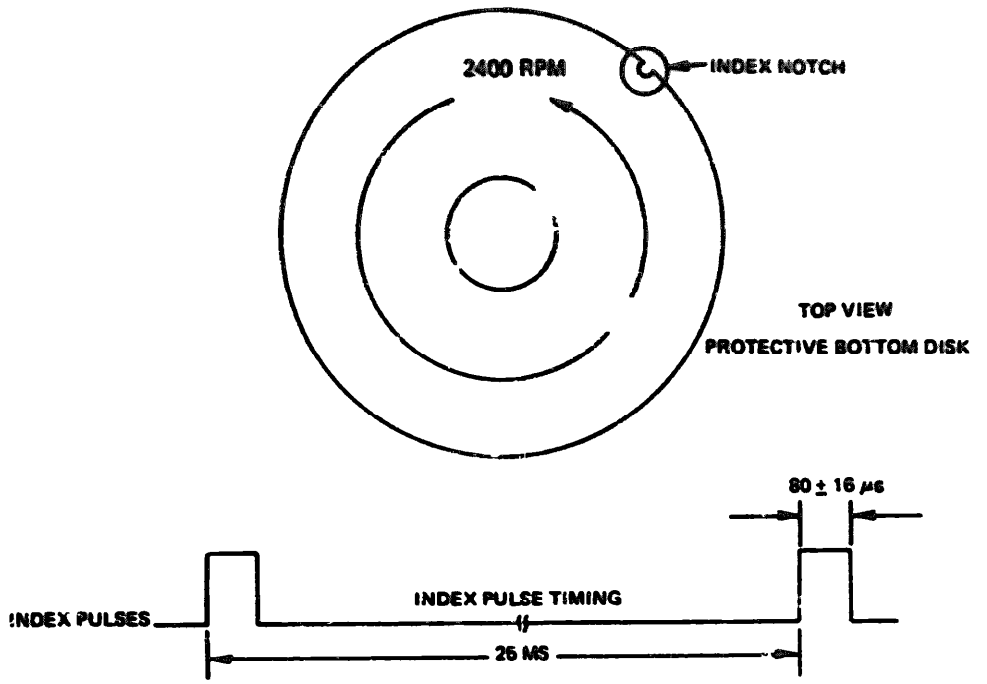

Figure 2-22. Index and Speed Detection

000 to cylinder 405 is 55 ms. The time required to position the heads from one cylinder to the next cylinder in both models disk drive, is 12 ms (minimum positioning time). The average head positioning time is based upon 50 percent of the maximum positioning time, i.e.; 32.5 ms for the model 114, and 27.5 ms for the model 215. **Average** rotational latency in both models disk drive is 12.5 ms.

2.4.7.3 Restore Operation

The restore operation is essentially a seek operation, in the sense that it causes the heads in the selected drive, from whatever cylinder they are at, to be positioned at cylinder 000. Thus, in effect, it is a seek operation to cylinder 000. The Restore logic is microprogram implemented. The logic flow is shown in the Restore flow diagram in appendix A. The Restore command is coded on the Bus and **Tag** interface lines as shown in Table 2-6, and **sent** to the selected disk drive.

2.4.7.4 Write Operation

Data is recorded on the disk pack using a double frequency bit-serial NRZ recording scheme. In this method of data recording a clock pulse is injected at the beginning of each bit cell time (Figure 2-23). A ONE bit, in the form of a data pulse, doubles the pulse frequency while a ZERO bit, represented by the absence of a data pulse, does not influence the clock pulse frequency.

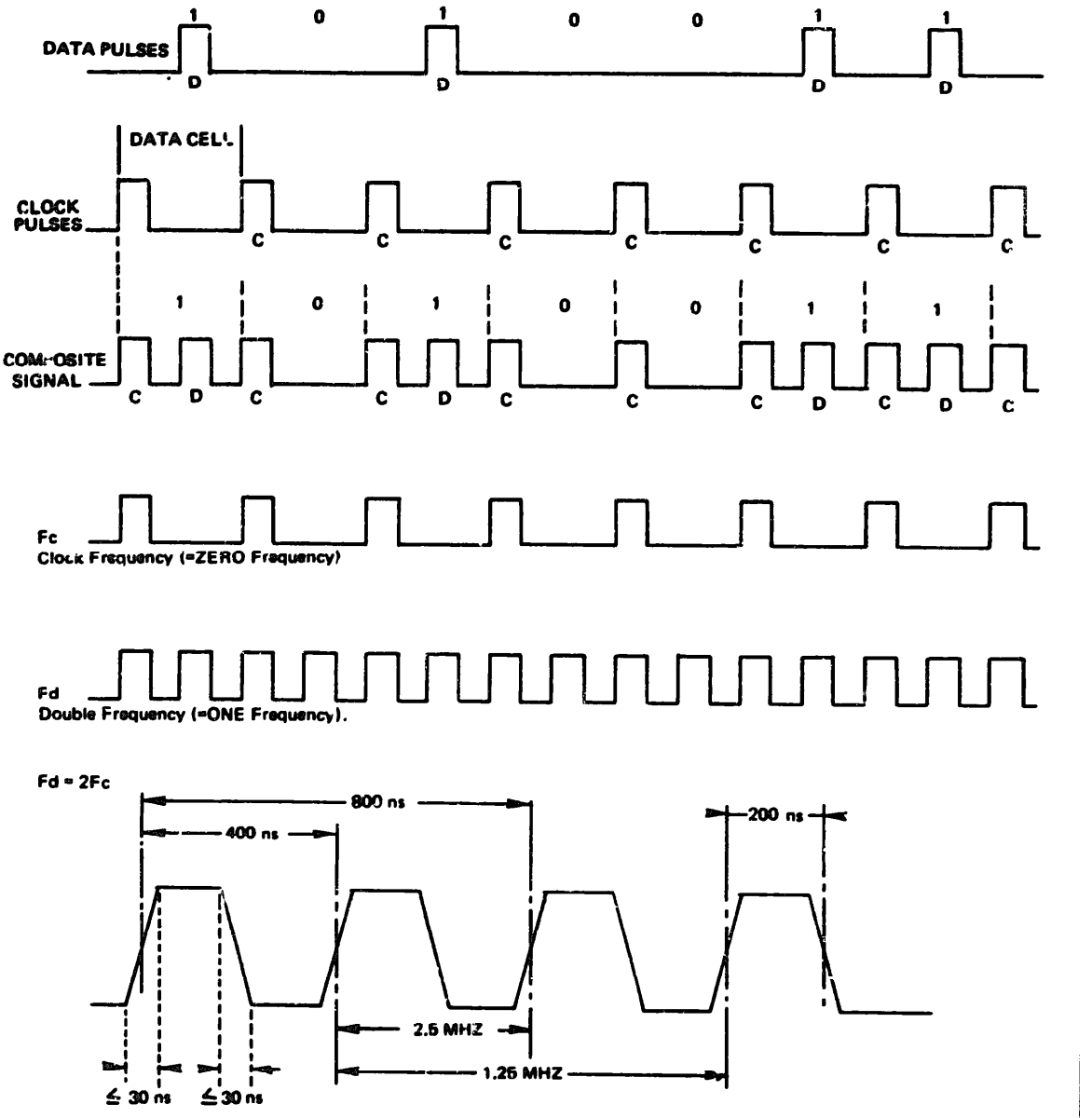

Figure 2-23. Double Frequency Data Recording

The write head works in conjunction with a tunnel erase head which is located in the head pad, slightly behind the write head. The combination write head/erase head enables the model 114 disk drive to write a 0.010 inch wide data track, then immediately erase it to a 0.007 inch wide, sharply defined track; in model 215 disk drives, data is recorded in an 0.007 inch wide track which is narrowed to a sharply defined 0.004 inch wide track by the erase head.

The purpose of the write and erase operations is to convert incoming digital data into a signal that will cause controlled magnetization of specific areas on the disks, in such a manner that when these magnetic patterns are read back, they will generate an electrical pulse train which translates into data that is identical to the original information. **A** typical write sequence data bit pattern is shown in Figure 2-24.

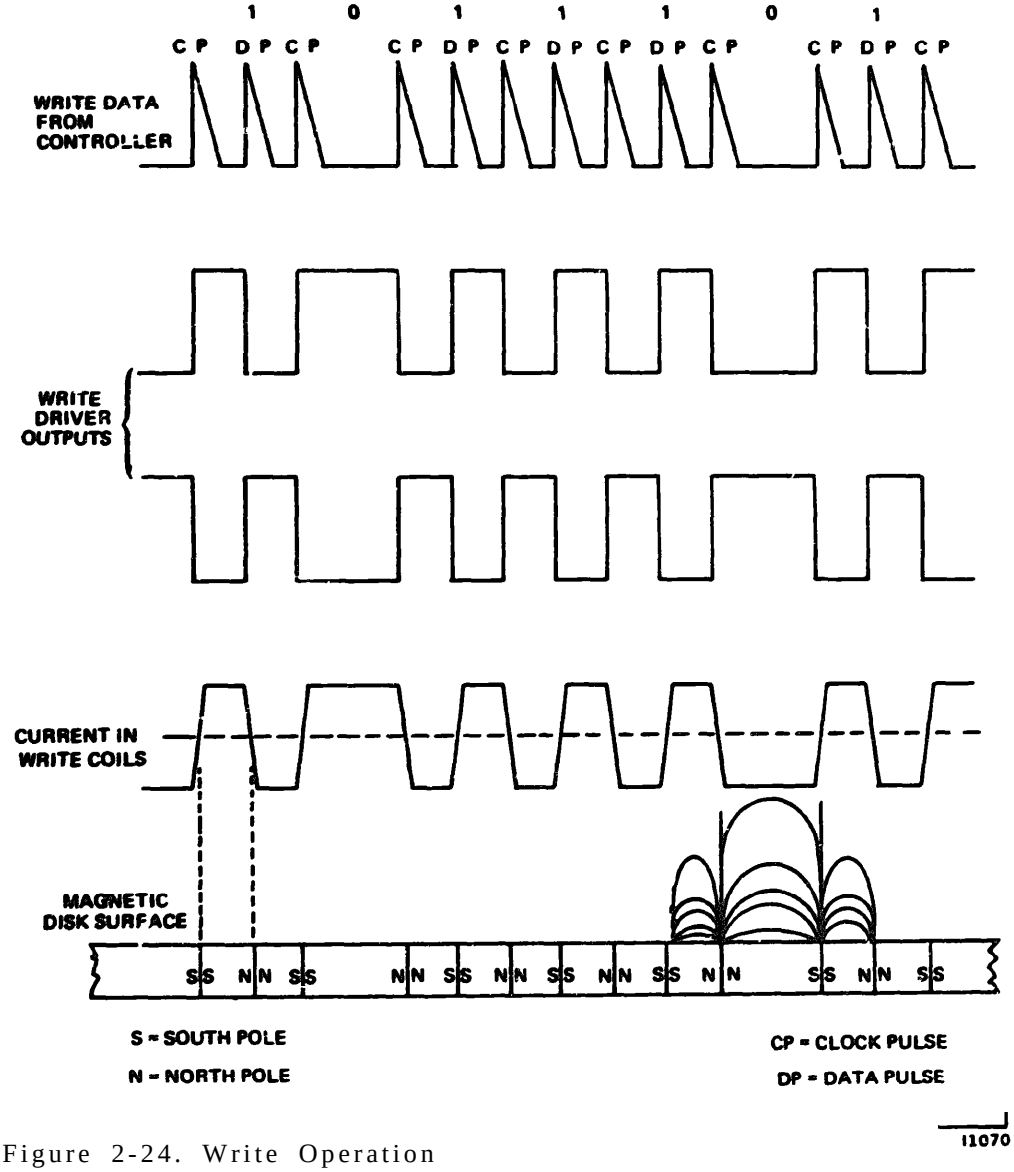

Figure 2-24. Write Operation

2.4.7.5 Write Command

The write operation is actually a combined write and erase operation. The tunnel-erase head located directly behind the write head in the same head pad, is used to tunnel erase the track after writing. This causes the tracks to be sharply defined while it simultaneously creates buffering inter-tracks that minimize crosstalk **(Figure 2-25). A** write operation is initiated **by** a write command from the processor. The controller then initiates a seek operation to direct the heads to the desired cylinder, selects the head associated with the specified track, and verifies that the correct track is accessed. Writing can commence after successful execution of the aforementioned operations. During the writing of data, data transfers are made from the IS/1000 memory to the controller, where the data is checked, serialized, and then sent to the disk drive. In the drive this electrically coded data is recorded onto the selected track in the form of magnetic flux reversal patterns.

The write logic is micro program implemented. The logic flow of the write operation is shown in the write flow diagram in appendix A. The Write command is coded on the Bus and Tag lines as shown in Table 2-6, and sent to the selected disk drive.

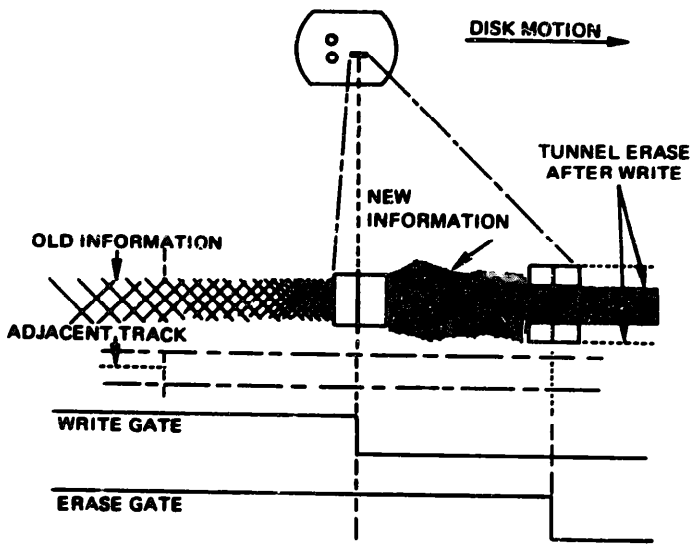

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Figure **2-25.** Head/Disk, Physical/Electrical Relationships

2.4.7.6 Write Timing Considerations

Frequency of the clock oscillator is 1.25 MHz, i.e., a 200 ns pulse is written every 800 ns (Figure 2-23). This 800 ns time interval between two clock pulses is called the data cell or bit cell time. **A** ONE is represented by a 200 ns pulse entered into **the data cell** time slot, i.e., between two clock pulses. Pulses are now 400 ns apart, thus effectively doubling the pulse frequency to 2.5 MHz. **A** ZERO is represented by two consecutive clock pulses without an interspersed data pulse. Maximum, i.e., worst case, rise and fall times of the squared clock and data pulses must not be more than 30 ns.

Commencement of the ***write*** and erase functions coincides and the controller therefore activates the write and erase gating signals simultaneously. However, since the erase head is physically located behind the write head with respect to the recording track, a point on the track passes under the write head approximately 50 us before it passes under the erase head. (Figure 2-25). The controller counteracts the time displacement between the recording and the tunnel erasure of the same point on the track, by dropping the write gate 50 us before the erase gate.

2.4.7.7 Write Data Transfer Rate

The data transfer rate during a write operation is 1.25 M bits per second between the processor and the subsystem. Within the subsystem the bit rate varies between 1.25 M bits per second *for* ZERO signifying data units, and 2.5 M bits per second for ONE signifying data units. To ensure that the read data bit rate will be within specified limits, the data bit rate during write operations must not vary more than 0.3 percent from nominal.

2.4.7.8 Format Track Operation

The format track operation is basically a write operation. Everything that has been said for the write operation applies equally to the format track operation. However, instead of random data which **may be scattered throughout the processor memory,** only very specific data, permanently assigned to specific locations in memory, is repetitively accessed and transferred from memory during the formatting of a track. The format used to store data on a disk pack in a GTE/IS magnetic disk subsystem, is an IBM compatible fixed format, as shown in Figure 2-16 and 2-17. The format track operation is used to establish this format on a track, As can be seen from Figure 2-16, the. track format consists basically of three major parts:

1. Home Address.
2. Track Descriptor Record.
3. Data Records, of which there are sixteen to a track.

Each track is started and subsequently ended by an index marker. The data areas of all records are filled with ZEROES.

The track fomatting logic is micro program implemented. The logic flow of the format track operation is shown in the **format** track flow diagram in appendix **A.**

The format command is coded on the Bus and Tag lines as shown in Table 2-6.

2.4.7.9 Read Operation

The read operation is for all practical purposes the inverse of the write operation. During a write operation, data represented by a bi-directional electrical current flowing through the write coil, is transformed into magnetic flux reversals **in the** write core, and stored as magnetic flux reversals in the magnetic surface of the recording medium passing across the write gap. During a read operation, the magnetic polarity reversing flux patterns on the recording medium passing across the read gap, induce electrical voltage pulses in the read coil, which then translate back into data.

The induced electrical voltages across the read coil approximate a sine wave with each peak representing a pulse. The sine wave frequency therefore is half the pulse rate. When reading clock pulses only, i.e., ZERO representing flux patterns in the recording track, the signal frequency is 625 kHz. The pulse rate, however, being twice the signal freguency is 1.25 M bits/sec. When reading clock and data pulses, i.e., ONE representing magnetic patterns on the recording **track,** the signal frequency is 1.25 MHz, the pulse rate 2.5 M bits/sec, and the data bit rate 1.25 MHz.

A typical read sequence bit pattern is shown in Figure 2-26.

2.4.7.10 Read Command

The purpose of the read operation is to convert data that is magnetically coded on the disk pack for off-line storage, into equivalent, electrically coded data for on-line processing.

A read operation is initiated by a read command from the processor. The controller then initiates a seek operation to direct the heads to the desired cylinder, selects the head associated with the specified **track,** and verifies that the correct track is accessed. Reading can commence after successful execution of the aforementioned operations.

During a read operation, the disk drive translates magnetic flux reversals on the disk pack into electrical pulses, which, after signal qualification and conditioning are sent to the controller.

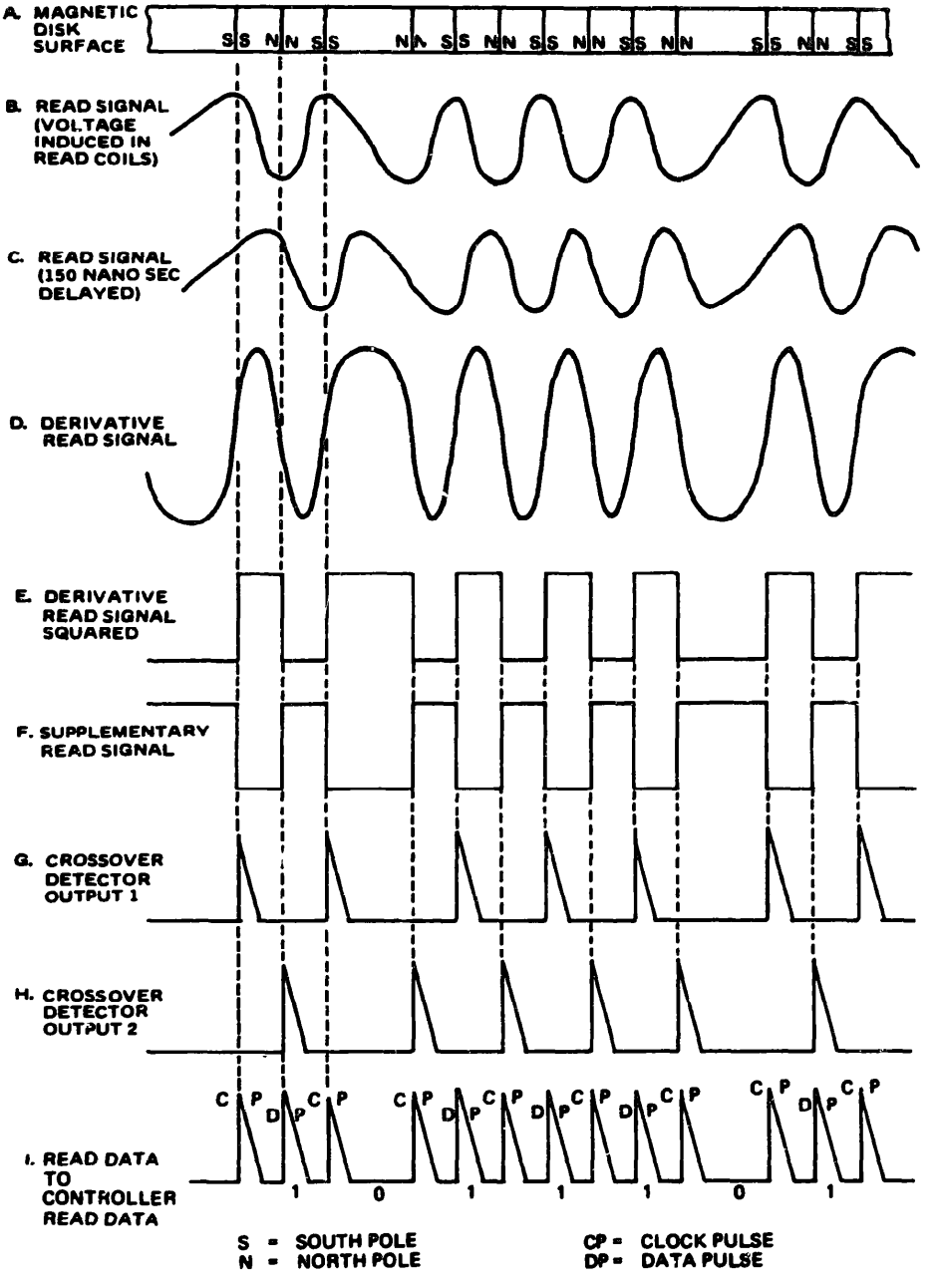

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Figure 2-26. Read Operation

In the **controller this serial** data from the disk drive is interpreted, checked and reformatted ***for*** parallel transmission to the ***processor.***

The read logic is micro program implemented. The ***logic*** flow **of** the read operation is shown **in** the read flow diagram, in appendix **A.** The read command is coded on the Bus and Tag lines as shown in Table 2-6, and sent to the selected disk drive.

2.4.7.11 Read Timing Considerations

The Read function is enabled when the Control Tag and the Bus lines are active simultaneously (Table 2-6). To ensure definite function interpretation, the Bus line must become active at least 200 ns prior to the Tag line and remain active for at least 200 ns after the Tag line has been deactivated. Minimal signal duration is 800 ns for the Tag pulse and 1200 ns for the Bus line pulse. Once deactivated, the bus line must remain inactive for at least 400 ns before it can become active again. Read Gate and Read Data become active at the same time, but Read Data is considered reliable only when read at least 10 us after Select Head or Advance Head.

2.4.7.12 Read Data Transfer Rate

The data transfer rate during a read operation is determined by the *recording* density and the rotational speed of the disk pack being read. The nominal bit rate is 1.25 million bits per second. Due to the inherent differences in head access and spindle speed variations among individual drives in the same subsystem, or even from one **subsystem to** the other, this nominal. bit rate may vary as much as ±15 percent.

2.4.7.13 Read Track Descriptor Operation

The read **track** descriptor operation is basically a read operation. Everything that has been said for the read operation applies egually to the read track descriptor operation. However, instead of reading the contents of an entire track, only the information comprising the five words of the header and the four data words of the specified track descriptor record, are sampled. This information can then be used for flagging or other identification purposes.

The read track descriptor logic is **micro** program implemented. The logic flow of the read track descriptor operation is shown in the corresponding flow **diagram in appendix** A. **The** read track descriptor command is coded on the Bus and Tag lines as shown in **Table** 2-6, and sent to the selected disk drive.

2.4.7.14 **Verify Operation**

The verify **operation is basically a read operation. Everything that** has been said for the read operation applies equally to the verify

operation. However, the operation is limited to reading for verification purposes only, and no data transfers to the IS/1000 processor take place. The verify operation is especially intended for the checking of header and cyclic check words after a write operation.

The verify logic is micro program implemented. The logic flow of the verify operation is shown in the verify flow diagram in appendix **A.** The *verify* command is coded on the Bus and Tag lines as shown in Table 2-6, and sent to the selected disk drive.

2.4.7.15 Read Status Operation

The read status operation has nothing in common with the regular read operation, which gathers data from the disk **pack.** A read status operation is initiated by a read status command from the processor. During the read status operation controller status information is sent to the processor by transferring the status words to the IS/1000 memory, in the following order:

1. *Major* status.
2. Minor status.
3. Number of **words** or sectors that have not been transferred.
4. DMA address location of last word transferred at termination of last operation preceding the read status operation.
5. Link address of the last packet control word pertaining to the previous operation.

Optionally, the following two additional status words may be sent to the IS/1000 memory:

1. Cylinder and head address.
2. Sector address.

These optional two status words will only be sent to the processor if so specified and when a word count greater than 5 is encountered.

The read status logic is micro-program implemented. The logic flow of the read status operation is shown in the read status flow diagram in appendix A. The read status command is coded on the Bus and Tag lines as shown in Table 2-6, and sent to the selected disk drive.

SECTION 3
OPERATING PROCEDURES

3.1 GENERAL

This section describes the operation and interpretation of the controls and indicators on the processor and disk drive control panels. Proper operation and correct interpretation of these controls and indicators, enables controlled initiation, modification, monitoring and suspension of all disk operations.

3.2 CONTROL *PANELS*

The operator control panels provide the switches and indicators required for operator communication between the processor and the disk subsystem.

3.2.1 Processor Operator Panel

The model 4821-01 IS/1000 control panel enables the operator to control processor operation for programming and maintenance purposes.

The control panel is shown in Figure 3-1. The functions of the control panel switches and indicators are described in Table 3-1.

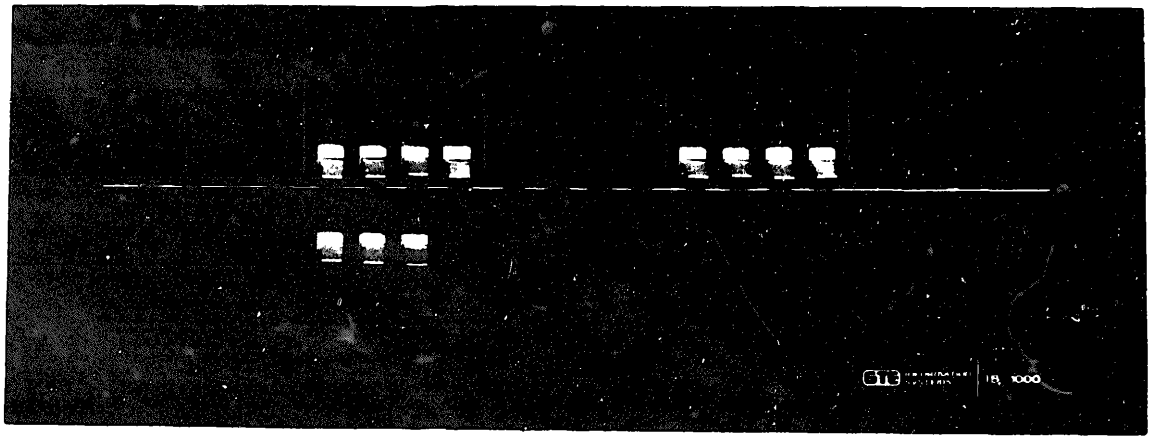

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Figure 3-1. IS/1000 Control Panel

Table 3-1. Control Panel Functions (Sheet 1 of 5)

Switch or Indicator	Type	Function
LOCK/ON/OFF	Key Switch	Insertion of the key is required to turn this switch to any position. In the LOCK position, power is applied, but no switches are operative. The SENSE switches are considered to be in the down position when the key switch is in this position. In the ON position, power is applied and all panel switches and indicators are operative. In the OFF position, no power is available to the processor.
POWER	Indicator	Comes on when power is applied to the processor.
LOAD	Momentary	When raised and released, initiates automatic loading of a bootstrap program from the ROM into memory and puts the CPU in the run mode, executing the program loaded from the ROM Actuating this switch with the power panel connected resets the system prior to automatic loading of the bootstrap program.
RUN	Indicator	Comes on when the CPU is in the run mode.
LT	Indicator	Displays the contents of S-Register bit 8, which indicates a less-than arithmetic condition.
GT	Indicator	Displays the contents of S-Register bit 9, which indicates a greater-than arithmetic condition.
EQ	Indicator	Displays the contents of A-Register bit 10, which indicates an equal-to arithmetic condition.
OVF	Indicator	Displays the contents of S-Register bit 11, which indicates an overflow arithmetic condition.
0 thru 15 Data Entry	Toggle switches*	In the up position, these switches insert a ONF into the corresponding bit positions of the selected register when the MODE switch is in the WRITE position and the INITIATE switch is pressed.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

Table 3-1. Control Panel Functions (Sheet 2 of 5)

Switch or Indicator	Type	Function
0 thru 15 Data Display	Indicators	When the MODE switch is in the READ position, these indicators display the contents of the register specified by the REGISTER SELECT switches. When the M Register is selected (M up, P and I down), the INITIATE switch must be pressed before the contents of the memory location specified by the address in the P Register are displayed. When the MODE switch is in the WRITE position, these indicators display the contents of the data switches. An indicator that is lit (on) displays a ONE bit.
GP REGISTER/ SENSE 8, 4, 2, 1	Toggle switches*	Used to select one of the general-purpose X Registers when REGISTER SELECT switches P, I and M are all in the down position. The 8, 4, 2 and 1 switches represent different binary values (weights). A switch set to the up position represents a ONE in that bit position. The combination of all four GP REGISTER switches is used to select the desired general-purpose register. For example, when all four switches are down, the A Register (X-Register 0) is selected. When only the right-most switch is up, the B Register (X-Register 1) is selected. All four switches up selects X-Register 15 (binary 1111). When the CPU is executing instructions, the switches act as program sense switches to allow external control over specified program operations. The up position specifies a logical ONE. The program can determine the state of the switches using BST and BSF instructions.
REGISTER SELECT P, I, M	Toggle switches*	The P and I switches, respectively, select the P or I Register when in the up position. In the up position, the M switch selects the M Register. When P, I and M are in the down position, the X Register specified by the GP REGISTER/SENSE switches is selected.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

Table 3-1. Control Panel Functions (Sheet 3 of 5)

Switch or Indicator	Type	Function
		When more than one switch is up, the left-most switch has priority. Thus, to select the I Register, the P switch must be down. To use the M switch, the P and I switches must be down. The direction of transfer must be selected by setting the MODE READ/WRITE switch and, if an X Register is selected, the GP REGISTER/SENSE switches must be properly set.
MODE READ/WRITE	Toggle switch*	In the READ position, when the INITIATE switch is pressed and the M switch is selected (M switch up, P and I switches down), the contents of the memory location specified by the contents of the P Register are shown on the data display indicators. The contents of the P, I or a general-purpose register may be displayed simply by selecting the appropriate register. The INITIATE switch need not be pressed. In the WRITE position, when the INITIATE switch is pressed, information from the data switches is transferred to either the register selected by the P, I or GP REGISTER switches, or, if the M switch is selected, the memory location specified by the contents of the P Register.
INITIATE	Momentary switch*	When the MODE switch is set to the WRITE position the INITIATE switch is pressed to enter information from the data switches into the selected register or memory: • The P Register when the P switch is up. • The memory location specified by the contents of the P Register when the M switch is up and the P and I switches are down.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

Table 3-1. Control Panel Functions (Sheet 4 of 5)

Switch or Indicator	Type	Function
		• The general-purpose register selected by the GP REGISTER switches when the P, I and M switches are down. *NOTE: Data is not written into the I Register.* When the MODE switch is set to the READ position, the M switch is selected and the INITIATE switch is pressed, the contents of the memory location specified by the contents of the P Register are shown on the data display indicators. When the MODE switch is set to the READ position, the contents of the following is displayed on the data display indicators: • The P Register when the P switch is up. • The I Register when the I switch is up and P is down. • The general-purpose register selected by the GP REGISTER switches when the P, I and M switches are down.
HALT	Momentary switch	When the CPU is in the run mode, pressing the HALT switch stops program execution at the completion of the instruction in process. When the CPU is in the halt mode: • If the M switch is selected, pressing the HALT switch increments the P Register and initiates a read/restore memory cycle. This has the effect of stepping through the memory and displaying the contents of each successive location on the data display indicators. Stepping through memory in this way displays the contents of successive locations but does not enable writing of data into memory, even if the MODE switch is set to WRITE.

Table 3-1. Control Panel Functions (Sheet 5 of 5)

Switch or Indicator	Type	Function
		• If the M switch is not selected, pressing the HALT switch causes one instruction to be executed. This instruction is in the memory location specified by the contents of the P Register. After execution of the instruction, the P Register specifies the location of the next instruction to be executed.
RESET	Momentary switch*	Pressing this switch when the CPU is in the halt mode effects the CPU logic as follows: • Resets the arithmetic overflow flip-flop. • Resets the memory control flip-flops. • Resets the automatic program-load flip-flop and indicator. • Sets all N-Register flip-flops (unmasks all interrupts). • Resets all interrupt flip-flops. • Resets the interrupt control sequencer. • Readies the instruction-trap interrupt for service. • Readies the power-fail/restart interrupt for service. • Resets all device controllers on the I/O bus.
RUN	Momentary switch*	When pressed, starts automatic program execution with the instruction at the memory location specified by the contents of the P Register.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

3.2.2 Format Protect Switch

The read/write protect switch is located on the power sequence card in the card file chassis of the interface assembly. The switch is shown in Figure 3-2. The functions of the Switch are described in Table 3-2.

3.2.3 Disk Drive Control Panel

The operator control panels differ for the models 114, 213 and 215 disk drives. They are described separately in the following paragraphs.

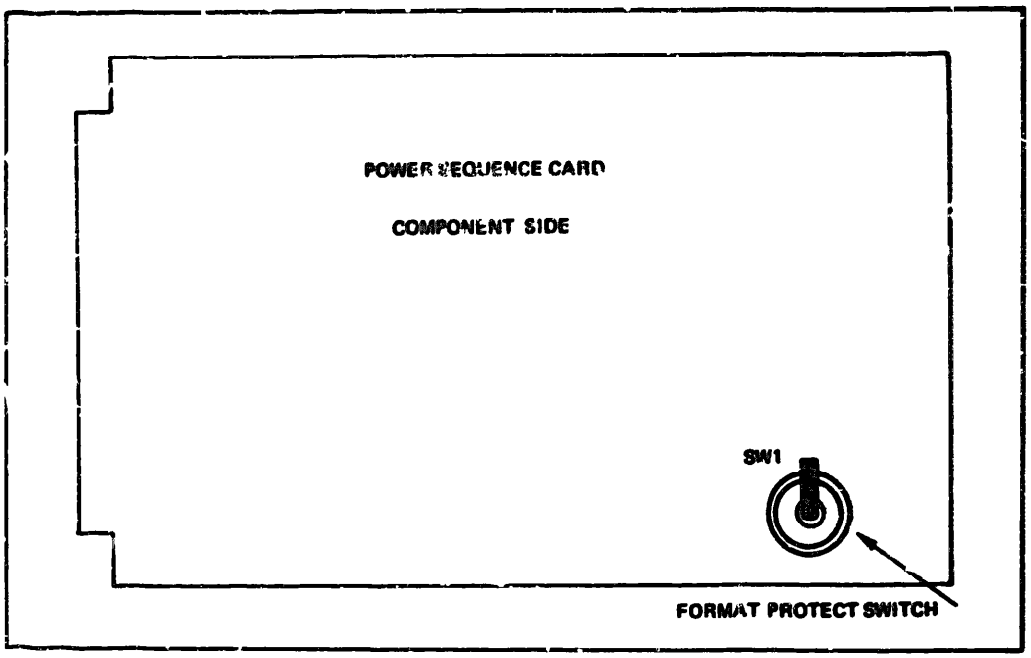


Figure 3-2. Format Protect Switch

Table 3-2. Format Protect Switch

Switch Setting	Function
Up	The track format of the disk pack in the selected disk drive can not be altered.
Down	The accessed track of the disk pack in the selected drive can be formatted.

3.2.3.1 Model 114 Disk Drive

The model 114 operator control panel is shown in Figure 3-3. The functions of the switches and indicators are described in Table 3-3.

3.2.3.2 Model 213 Disk Drive

The model 213 operator panel is shown in Figure 3-4a. The functions of the switches and indicators are described in Table 3-4.

3.2.3.3 Model 215 Disk Drive

The model 215 operator panel is shown in Figure 3-4b. The function of the switches and indicators is the same as for the model 213. Refer to Table 3-4 for a description of switch and indicator functions.

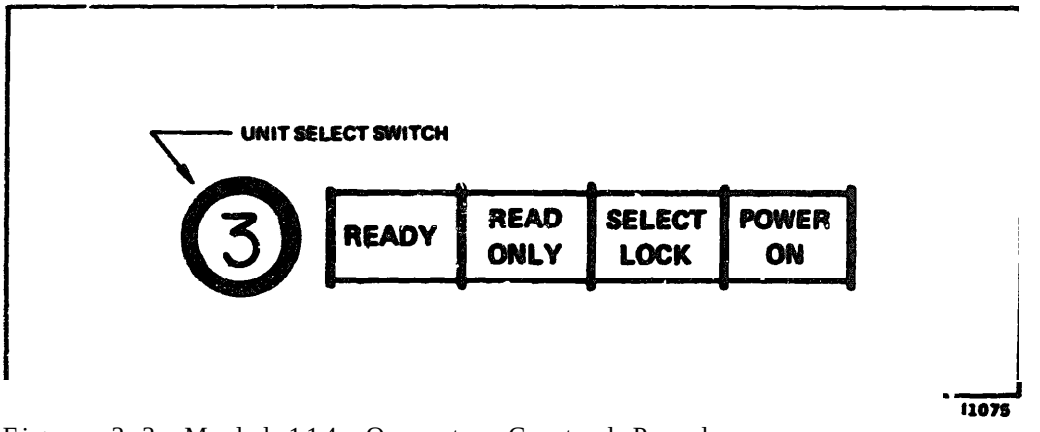
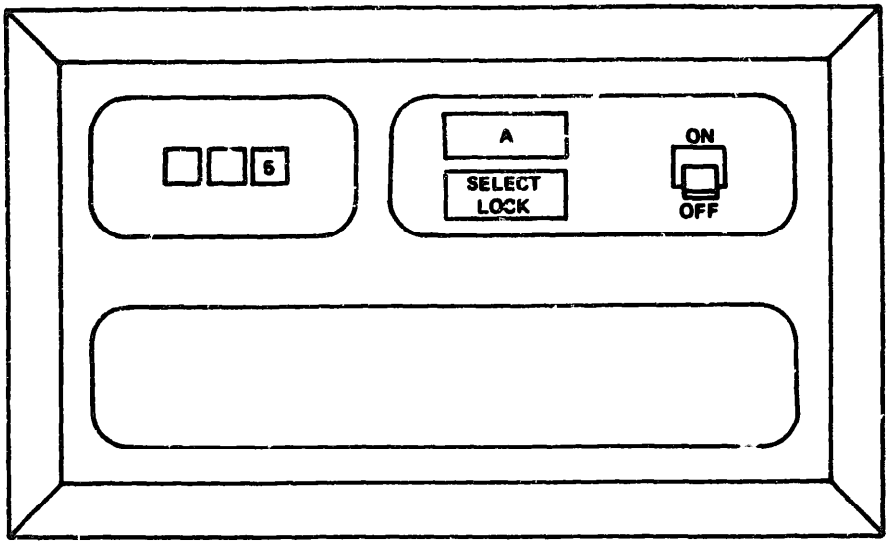


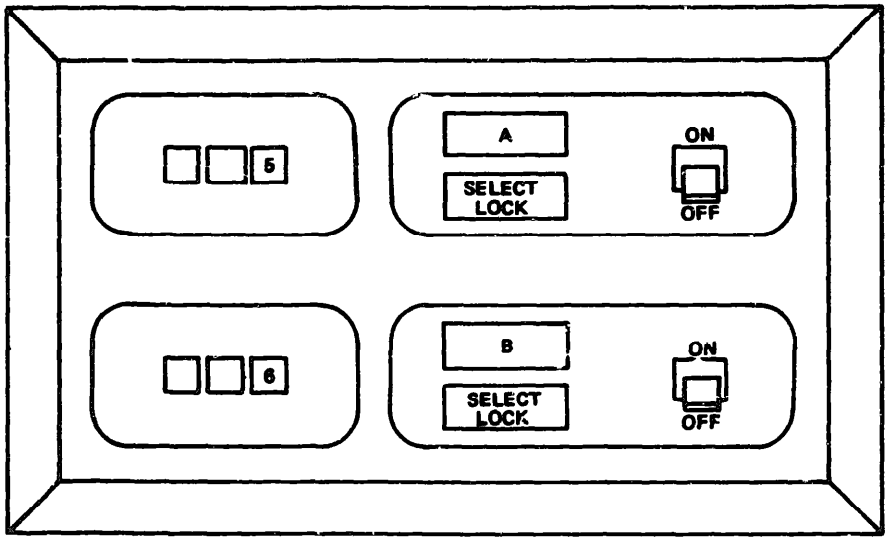
Figure 3-3. Model 114, Operator Control Panel

Table 3-3 Model 114, Controls and Indicators

Control/Indicator	Function
POWER ON Pushbutton/ Indicator, white	Initiates and indicates power-up or power-down sequence when pressed.
READ ONLY Pushbutton/ Indicator, yellow	Indicates that any write operation is inhibited when pressed to light.
SELECT LOCK Indicator, red	Indicates that an unsafe drive condition exists.
READY Indicator, green	Indicates that the drive is ready for operation
Unit Select Switch	Provides On-line Signal and Unit select number to controller when turned to slot position and pushed down.



A. MODEL 213 OCP



B. M. ODEL 215 OCP

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Figure 3-4. Model 213/215 Operator Control Panels

Table 3-4. Model 213/215, Controls and Indicators

Control/Indicator	Function
ON/OFF Switch	Toggle switch used to initiate a power-up, or power-down sequence.
File Number *Indicator (Green)	Indicates that initial seek is complete and the drive is ready.
SELECT LOCK *Indicator (Red)	Indicates an unsafe condition exists and corrective action is required.
Unit Select Block	Provides On-Line Signal and Unit Select number to controller when inserted into Unit Select Switch Selector Socket.

*Push-to-test

3.3 PROGRAM LOADING

Program loading can be accomplished automatically, or through a peripheral device. The next paragraphs describes the method of automatic program loading and through the TTY, since this is by far the common peripheral used for program loading.

For program loading from other devices refer to the User's Manual, GTE/IS publication E0006.

3.3.1 **Automatic Program Load**

Automatic program Load (APL) enables loading of the Bootstrap program into memory from the ROM.

3.3.1.1 Control Panel APL

With the control panel connected and the CPU in the halt mode, the APL function can be activated in one of two ways:

- With the LOCK/ON/OFF switch at the ON position, raise and release the LOAD switch.
- With the LOCK/ON/OFF switch at the LOCK position, APL may be activated via the ALOAD+ and ALOAD- signals over the I/O bus. ALOAD+ (normally low) goes high for about 10 us, then low again. ALOAD- (normally high) goes low and then high in sync with ALOAD+.

If APL is to be activated both via the I/O bus and the control panel, the switch on the I/O controller that activates the APL must have an additional control corresponding to the key on the control panel.

This control disables the I/O bus switch controls from ALOAD+ and ALOAD-. When enabled via a key on the control panel, APL cannot be

activated from the I/O bus. When APL is enabled by a switch similar to a key and is activated over the I/O bus, the APL function cannot be activated from the control panel.

3.3.1.2 Power Panel APL

The power panel APL function has the same interlock as the control panel. In addition, APL causes the CPU and controller (via I/O signal SYRST-) to be reset when activated.

3.3.1.3 Blank Panel APL

Since the CPU does not require either the control panel or the power panel for operation, a blank panel may be used. Under these conditions, the APL function is controlled exclusively from the I/O bus. This eliminates the interlocking function only, but still allows the CPU and controllers to be reset during APL.

3.3.1.4 APL Cautions

Activation of the APL feature via the I/O bus or from the power panel is not synchronized with CPU timing. Therefore, if the CPU is executing programs when the APL is activated, the resetting of the CPU will probably alter the contents of the registers in the CPU.

The memory interface is designed so that resetting the CPU does not affect reading data from memory. If, however, the CPU is writing into memory when it is reset, the data that is written cannot be assumed to be correct.

3.3.2 **Program** Loading

The following describes program loading via the TTY paper tape reader.

Perform program loading as follows:

1. Determine the type of ROM in the system: single-segment, four-segment, or two-segment. The TTY program is resident in the following ROM segments:
   - Single-segment ROM: segment I.
   - Four-segment ROM: segment I.
   - Two-segment ROM: segment II.
2. Perform program loading procedures for a specific ROM as follows:
   - Single-segment ROM - perform step 3.
   - Four-segment ROM - perform step 4.
   - Two-segment ROM - perform step 5.

k. If the operator desires to verify a tape after loading, proceed to step l.

l. Load the tape as described previously with SENSE switch 2 up.

m. Rewind the tape and load it a second time with SENSE switch 1 up.

If an error is detected during either load operation, the processor halts with the I-Register set to one of the values listed in Table 3-6. If loading is successful, the I-Register value is $1.

4. Perform automatic loading of an absolute program using four-segment ROM as follows:

a. Ready the program on the input device (steps 3a thru 3d).

b. At the processor control panel, press HALT then RESET.

c. Set the SENSE switches as follows:

- 8 down.
- 4 down.
- 2 up if it is desired to halt the program just loaded before control is transferred to it.
- 1 up if it is desired to halt the program to inspect and/or enter configuration data into the processor A and B Registers.

d. Set P, I, and M down.

e. Lift and release LOAD. If SENSE switch 1 is down, the program loads into the processor core memory.

A halt occurs with any of the I-Register values shown in Table 3-7.

Table 3-6. Tape Load Halts, Single-Segment ROM

I-Register Value	Meaning
$1	Successful load.
$F	Checksum error.
$1F	Verify error.
$2F	I/O instruction rejected.
$3F	Load error.

Table 3-7. Tape Load Halts, Four-Segment ROM

I-Register Value	Meaning	Recovery
$22	Enter configuration data in A Register.	Enter data and press RUN.
$3B	Halt prior to branching to program.	Press RUN.
$F	Bad checksum on last record.	Restart ROM.
$F	Check checksum on record last read.	Restart ROM by pressing RUN.
$0	I/O instruction reject.	Restart ROM at P=$55.

f. Enter or inspect configuration data in the A and B Registers as follows:

- A Register:

Bits	Use
0 thru 3	Unused.
4 thru 7	Interrupt line.
8 thru 9	Unused.
10 thru 15	Device address.

- B Register - Not used.

g. Press RUN. The program loads into the processor core memory.

5. Perform automatic loading of an absolute program using two-segment ROM as follows:

a. Ready the program on the input device (steps 3a thru 3d).

b. Press HALT and then RESET.

c. Set the SENSE switches as follows:

- 8 up.
- 4 up.
- 2 up if it is desired to halt the program just loaded before control is transferred to it.
- 1 down.

d. Set P, I, and M down.

e. Lift and release LOAD. The program loads into the processor core memory.

SECTION 4
INSTALLATION

4.1 GENERAL

This section outlines the basic procedures to install and prepare the hardware for operation. Correct installation is a prerequisite to proper operation and should only be *performed* by qualified service personnel.

WARNING

Before performing any of *the installation or removal procedures in this section, ensure that all electrical power is removed from the units and the chassis to prevent possible injury or equipment damage.*

Due care should be exercised and proper tools used at all times, to prevent damage to the boards and/or the equipment.

4.2 SITE REQUIREMENTS

The PDC and DCI logic boards are both to be installed in a regular IS/1000 powered chassis (assembly 101787), *or* in an extended powered chassis (assembly 103039). They must preferably be installed one directly above the *other*. The chassis is mounted in a regular 19-inch electronic component rack or cabinet.

The IOL, MUX, PLO, *PSQ* and SMX logic cards are all installed in the card file of the disk interface chassis (assembly 103982). They must be inserted in the order given in Figure 4-1. The interface chassis is mounted in the same 19 inch electronic component rack or cabinet.

The ac power panel is mounted in the same cabinet as the powered chassis and the disk interface assembly.

4.2.1 Power Requirements

The power requirements for the controller are given in Table 4-1.

Power requirement for the PDC board is +5.0 Vdc at 7.0 A. This power is supplied by the chassis power supplies.

Power requirement for the DCI board is +5.0 Vdc at 2.0 A. This power is supplied by the chassis power supplies.

The power required by the card complement of the disk interface card file is supplied by a self contained power supply. This *power* supply also provides the *+5.0* Vdc at 1.0 ***A,*** needed for the terminator terminating the signal lines of the multiplex cable in the last disk drive of the disk system.

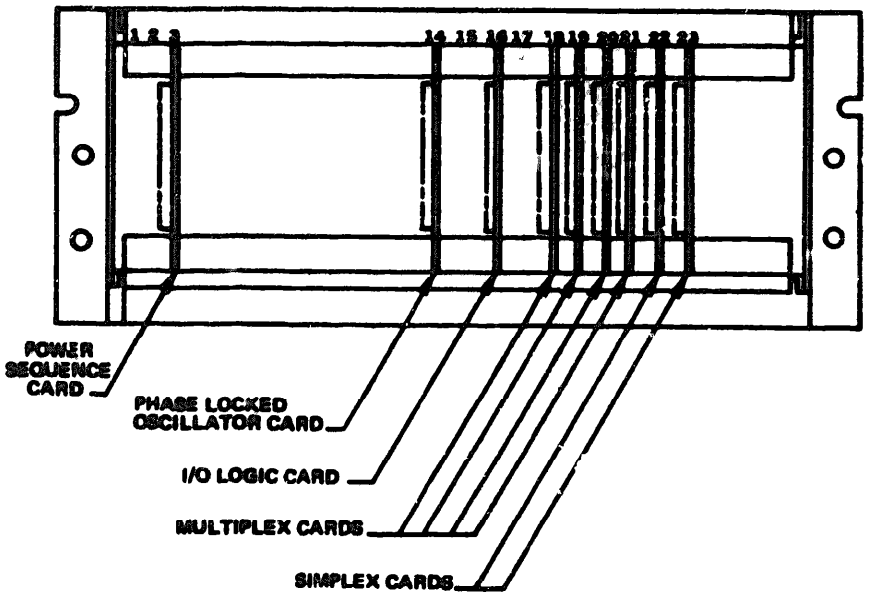

Figure 4-1. **Card File, Card Locations.**

AC power required by the entire disk subsystem is determined by the size of the disk system. The controller requires a 110 Vac, single phase, power source. Model 114 disk drives require single phase or three phase 208 or 230 Vac, Model 215 disk drives require three phase 208 or 230 Vac. The drives receive their ac power via the power distribution panel in the controller, which enables the controller powering up and down sequences in case of multi-spindle disk subsystems. Additionally, the three phase 208/230 Vac, is rotated from drive to drive. Power consumption of the 110 Vac depends upon the complement of logic boards and cards used in addition to the PDC and IOC boards. Power consumption of the 208 or 230 Vac depends upon how many disk drives the subsystem consists of and can be computed from the data given in Table 4-1.

4.2.2 Environmental Requirements

The controller is designed to operate in a normal data processing environment.

4.2.2.1 Temperature

Under operating conditions the temperature range must be between 60°F and 90°F, with a maximum allowable temperature variation of 15°F per hour. Under non-operating conditions, the temperature

Table 4-1. Disk System Power Consumption

Equipment	Power Consumption			
	Voltage	Current		Heat Dissipation
PDC Board	+5 Vdc	7A		
DCI Board	+5 Vdc	2A		
I/O Assembly	+5 Vdc	4A		
Terminator	+5 Vdc	1A		
		Starting	Operating	
Disk Drive Model 114	208/230 ± 10% Vac single phase 60 ± 0.5 Hz 50 ± 0.5 Hz (Optional)	20 A for 7 seconds	3.5 A	2050 BTU/hr
Disk Drive Model 213	208/230 ± 10% Vac three phase 60 ± 0.5 Hz 50 ± 0.5 Hz (Optional)	20 A for 7 seconds	4.3 A	2900 BTU/hr
Disk Drive Model 215	208/230 ± 10% Vac three phase 60 ± 0.5 Hz 50 ± 0.5 Hz (Optional)	20 A for 7 seconds per spindle	4.3 A per spindle	5800 BTU/hr

range can be between -30°F and 150°F. Cooling for the PDC and IOC boards is provided by the chassis power supply cooling fans which provide a positive pressure airflow across the horizontal PC boards. The interface assembly is cooled by a selfcontained fan.

4.2.2.2 Relative Humidity

Under operating conditions the relative humidity must be between 10 percent and 80 percent. Under non-operating conditions, the relative humidity can be between 5 percent and 98 percent. In either case, condensation must be prevented at all times.

4.3 CABLING AND PATCHING

The system cabling, as shown in Figures 4-2, 4-9 and 4-24, consists **of four types of** cabling:

1. Processor to controller interface cabling.
2. Intra-controller cabling.
3. Controller to device interface cabling.
4. Power cabling.

Five types of patching are possible:

1. Address patching.
2. Interrupt and ICI patching.
3. DMA-priority patching.
4. Drive type recognition patching.
5. Number of SMX cards patching.

4.3.1 Processor to Controller Interface Cabling

The processor to controller interface is constituted by the regular internal interface, i.e., two 50-line flat ribbon cables connecting the J1 and J2 edge connectors of the CPU board to the J1 and J2 edge connectors of the PDC board. The internal interface cable is illustrated in Figure 4-3. Figure 4-3 also gives the physical pin designations of the edge connectors. For electrical signal line/ connector pin designations, alphabetically by ***mnemonic, refer to*** Tables 4-2 and 4-3. For a numerical by pin number listing, *refer* to engineering drawing 300337, page 4, of Appendix C.

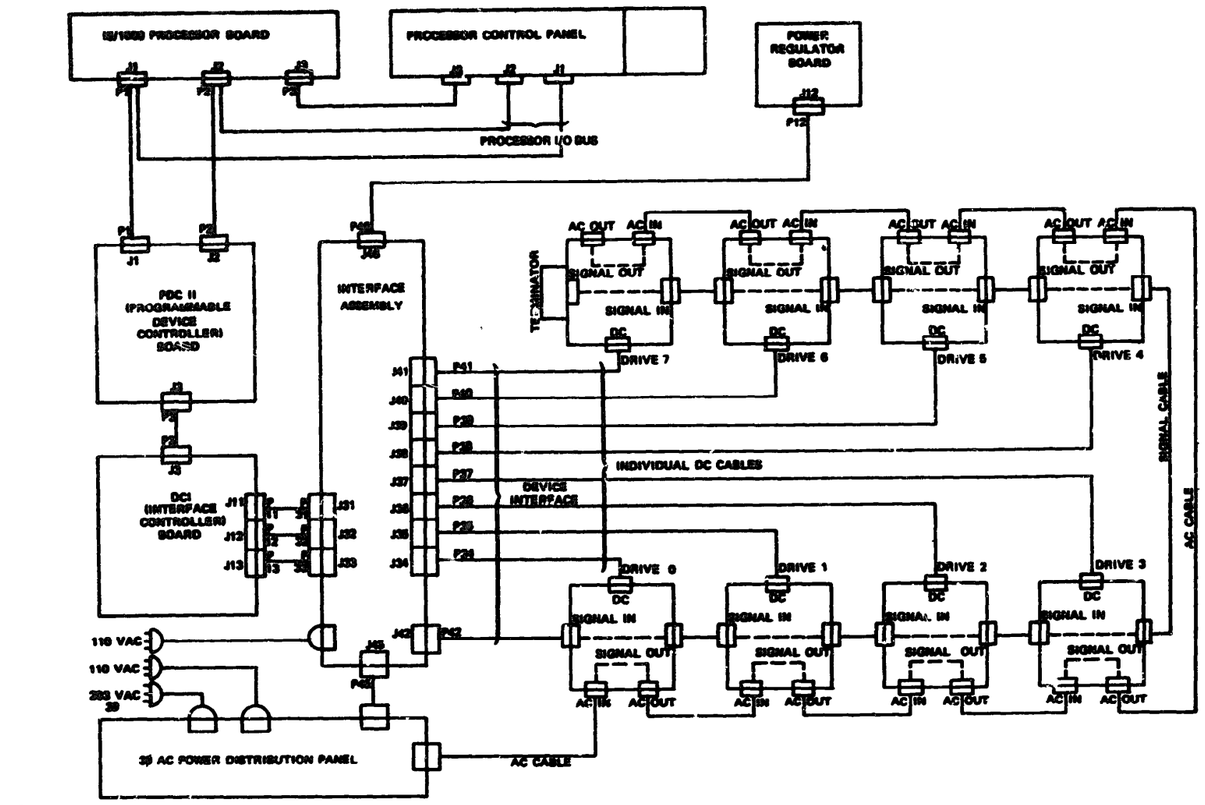

Figure 4-2. IS/1000 Magnetic Disk System Cabling Diagram

Table 4-2. PDC Board, Edge Connector J1

Signal Name	Pin	Ground	Signal Name	Pin	Ground
DA01-	49		DMAP1+	22	
DA05-	46	17 GND	DMAP2+	26	
DIB00-	5	19 GND	DMAP3+	42	
DIB01-	4	21 GND	EKO-	10	
DIB02-	12	23 GND	INTO8-	32	
DIB03-	13	25 GND	INTO9-	28	
DIB04-	3	27 GND	INT10-	34	
DIB05-	14	29 GND	INT11-	36	
DIB06-	1	31 GND	INT12-	30	
DIB07-	11	33 GND	INT13-	26	
DIB08-	15	35 GND	INT14-	40	
DIB09-	16	37 GND	INT15-	24	
DIB10-	9	39 GND	OFO-	48	
DIB11-	10	41 GND	OF1-	50	
DIB12-	7	43 GND	OF2-	47	
DIB13-	8	45 GND	PCLK-	44	
DIB14-	2		STR8-	20	
DIB15-	6				

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Table 4-3. PDC Board, Edge Connector J2

Signal Name	Pin		Ground	Signal Name	Pin		Ground
ALOAD+	40	2	GND	DOB04-	14		
ALOAD-	42	4	GND	DOB05-	15		
BUSY+	27	6	GND	DOB06-	16		
DAC0-	44	8	GND	DOB07-	13		
DA02-	45	26	GND	DOBC8-	24		
DA03-	46	28	GND	DOB09-	20		
DA04-	47	31	GND	DOB10-	22		
DMACW0-	34	33	GND	DOB11-	10		
DMACW1-	32			DOB12-	12		
DMALD-	7	35	GND	DOB13-	11		
DMAMS-	36	37	GND	DOB14-	23		
DMAST-	38	39	GND	DOB15-	25		
DMOS-	29	43	GND	KF0-	48		
DMRQ-	1			KF1-	49		
DMRS-	3			KF2-	50		
DOB00-	19			PFFIP-	41		
DOB01-	17			PRLD-	30		
DOB02-	18			SYRST-	5		
DOB03-	21						

4.3.2 Intra Controller Cabling

The intra-controller cabling consists of the following cables:

- **One 50-line flat ribbon cable connecting the J3 edge connector of the PDC board to the J3 edge connector of the DCI board. The cable is illustrated in Figure 4-3, and shows the physical pin designations. For electrical signal line/connector pin designations, alphabetically by mnemonic, refer to Table 4-4 and 4-5. For a numerical by pin number listing, refer to sheet 4 of engineering drawings 300337 and 300352, of Appendix C.**
- Three identical 30-line cables connect the J11, J12 and J13 edge connectors of the DCI board to the J31, J32 and J33 connectors of the interface assembly, respectively. The cable is illustrated in Figure 4-4. For physical pin designations, see Figure 4-8. For electrical signal line/connector pin designations, alphabetically by mnemonic, ***refer*** to Tables 4-6, 4-7, and 4-8. For a numerical by pin ***number*** listing, refer to engineering drawing 300352, sheet 4, *of* Appendix C.

4.3.3 Controller to Device Interface Cabling

The controller to device interface comprises the following cables:

- One 100-line signal cable connecting the J42 connector of the interface assembly to the SIGNAL IN connector of the ***first*** disk drive in the disk subsystem. In a multiple spindle system, the signals input to the first drive, must be

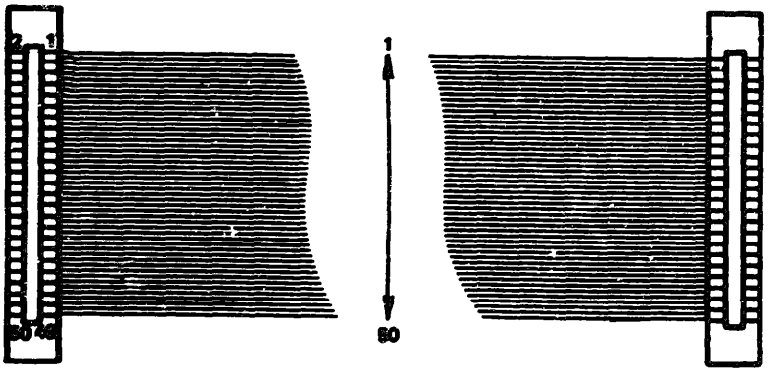

Figure 4-3. Internal Interface Cable/Connector Assembly

Table 4-4. PDC Board, Edge Connector J3

Signal Name	Pir No.		Ground	Signal Name	Pin No.		Ground
BRDY-	47	1	GND	IOD0-	21	28	GND
CLK+	43	4	GND	IOD1-	23	30	GND
DA0-	5	6	GND	IOD2-	25	32	GND
DA1-	7	8	GND	IOD3-	27	34	GND
DA2-	9	10	GND	IOD4-	29	36	GND
DA3-	11	12	GND	IOD5-	31	38	GND
DA4-	13	14	GND	IOD6-	33	40	GND
DA5-	15	16	GND	IOD7-	35	42	GND
DA6-	17	18	GND	SRST-	3	44	GND
DA7-	19	20	GND	STRB-	49	45	GND
DDL-	41	22	GND			46	GND
EXTINT-	39	24	GND			48	GND
EXTRES-	2	26	GND			50	GND

Table 4-5. DCI Board, Edge Connector J3

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
BRDY-	47	1	GND	IOD2-	25	28	GND
CLK+	43	4	GND	IOD3-	27	30	GND
DA00-	5	6	GND	IOD4-	29	32	GND
DA01-	7	8	GND	IOD5-	31	34	GND
DA02-	9	10	GND	IOD6-	33	36	GND
DA03-	11	12	GND	IOD7-	35	38	GND
DA04-	13	14	GND	SRST-	3	40	GND
DA05-	15	16	GND	STRB-	49	42	GND
DA06-	17	18	GND			44	GND
DA07-	19	20	GND			46	GND
DDL-	41	22	GND			48	GND
IOD0-	21	24	GND			50	GND
IOD1-	23	26	GND				

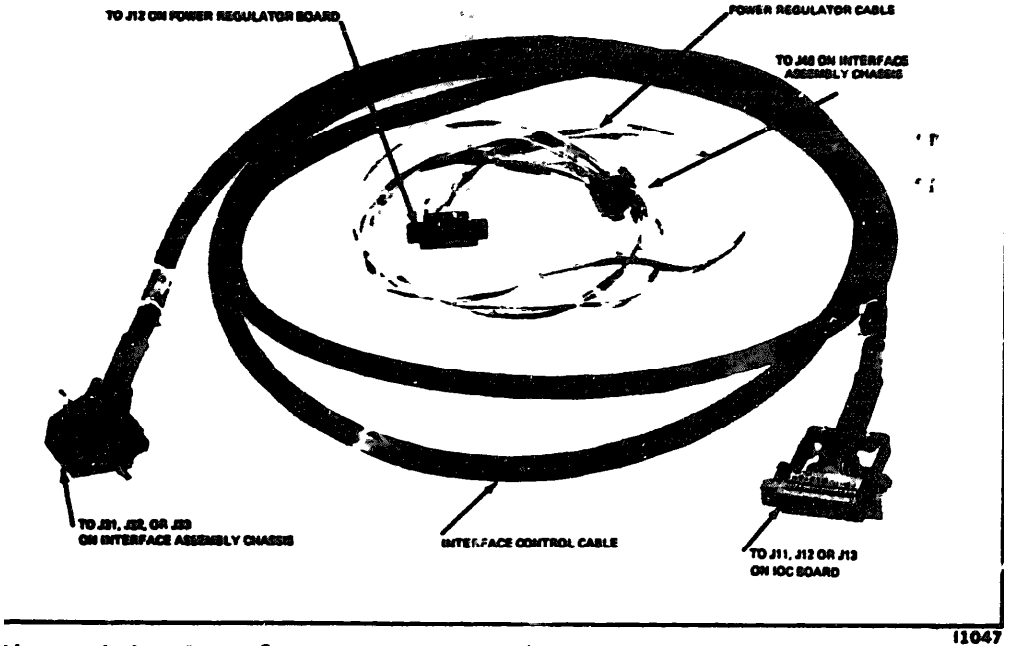

Figure 4-4. Interface Control Cable/Connector Assembly, and Power Regulator Cable

propagated to the next drive(s) by shorter cable segments in daisy chain fashion. The cable must be terminated in the last drive by a terminator. The cable is illustrated in -***Figure*** 4-5. For physical pin designations, see Figure 4-8. For electrical signal line/connector pin designations, refer to Table 4-9. For terminator and cable assembly numbers, refer to Table 4-22.

- From one to eight identical dc cables, depending upon the number of disk drives in the subsystem. Each cable connects one of the J34 thru J41 designated connectors on the interface assembly, to the DC connector of a disk drive. Hence, each disk drive in the subsystem is separately connected to the controller by one such DC cable. The cable is illustrated in -Figure 4-6. ***For*** physical pin designations, see Figure 4-8. For electrical signal line/connector pin designations, refer to Table 4-10. For cable assembly number refer to Table 4-22.

4.3.4 Power Cabling

The PDC and DCI boards receive electrical power in Standard IS/1000 fashion, through edge connector P14, which on each-board is plugged into receptacle J14 of the common power bus in back of the card cage chassis.

Table 4-6. DCI Board, Edge Connector J11

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
ATTEN0-1	4	3	GND	ATTEN7-1	18	23	GND
ATTEN1-1	6	5	GND	FDEVA1-1	24	27	GND
ATTEN2-1	8	9	GND	FDEVA2-1	22		
ATTEN3-1	10	11	GND	FDEVA4-1	20		
ATTEN4-1	12	15	GND	+12V(output)	28		
ATTEN5-1	14	17	GND	+12V(output)	29		
ATTEN6-1	16	21	GND	+12V(output)	30		

Table 4-7. DCI Board, Edge Connector J12

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
BUSY-1	13	3	GND	ONLIN-1	4	27	GND
CKA2-1	22	5	GND	PKCHG-1	14		
CKB2-1	24	9	GND	RDDAT-1	18		
CSRST-	26	11	GND	SKINC-1	10		
DSERR-1	16	15	GND	SWFMTP-	25		
ENDCYL-1	7	17	GND	UNSAF-1	8		
INDEX-1	6	21	GND	WCSEN-1	12		
NOCLK-1	20	23	GND				

Table 4-8. DCI Board, Edge Connector J13

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
CNTRL-1	24	3	GND	DBUS7-1	14	27	GND
DBUS0-1	4	5	GND	DBUS3-1	16		
DBUS1-1	6	9	GND	FINHCK-1	25		
DBUS2-1	7	11	GND	STCYL-1	20		
DBUS3-1	8	15	GND	STHED-1	22		
DBUS4-1	10	17	GND	SYNC-1	26		
DBUS5-1	12	21	GND	WRTDAT-1	18		
DBUS6-1	13	23	GND				

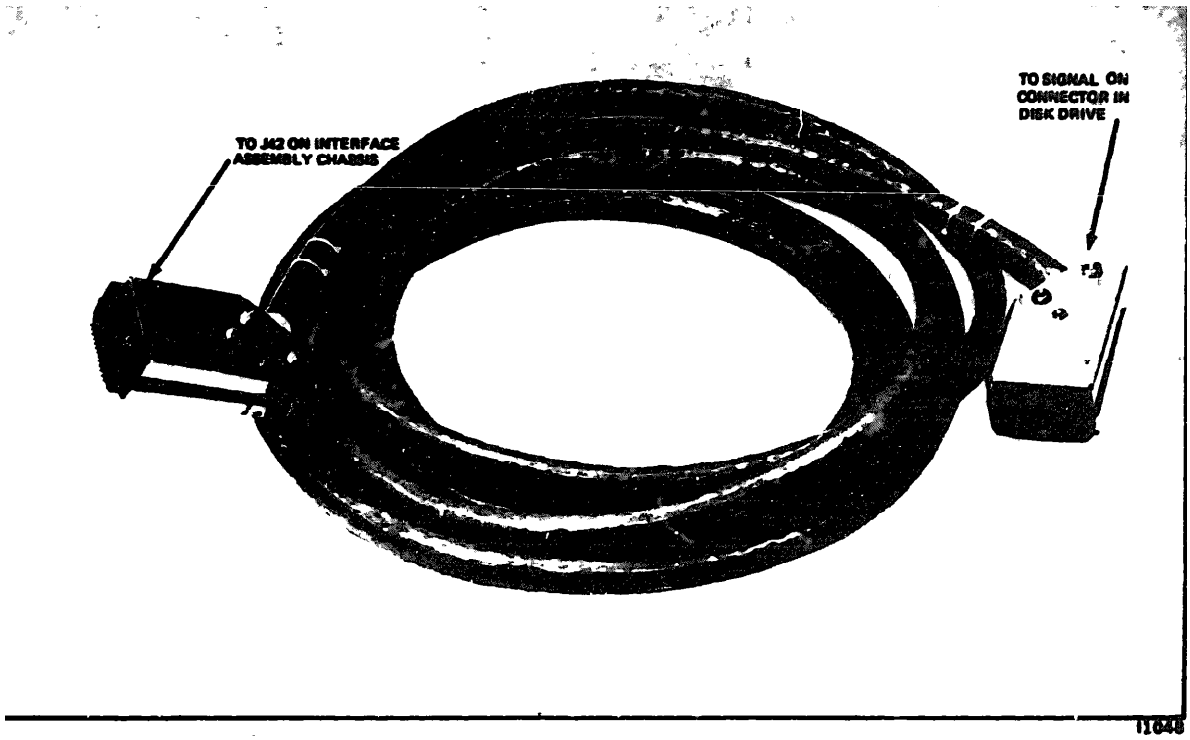

Figure 4-5. Signal Cable

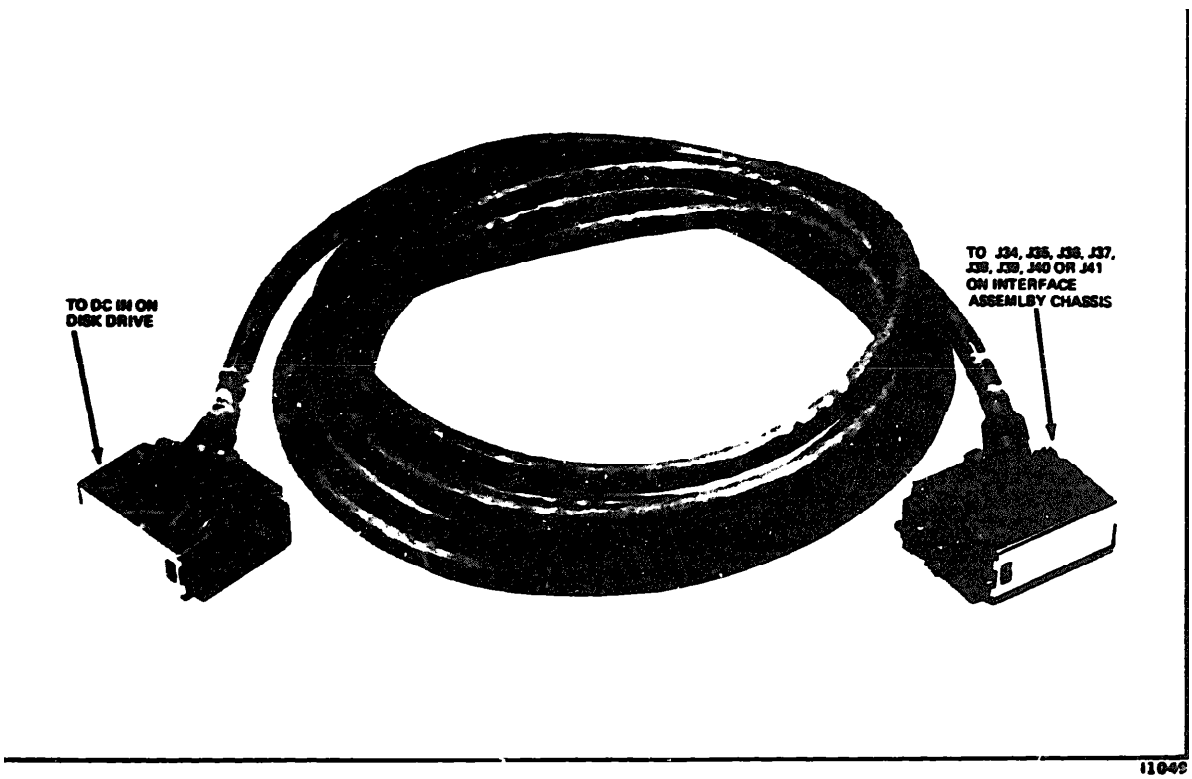

Figure 4-6. DC Cable

Table 4-9. Signal Cable

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
DBUS0-	A	B	GNDA	GATTEN5-	AJ	AK	GNDAJ
DBUS1-	C	D	GNDC	GATTEN6-	AL	AM	GNDAL
DBUS2-	E	F	GNDE	GATTEN7-	AN	AP	GNDAN
DUBS3-	H	J	GNDH	GATTEN-(Spare)	AR	AS	GNDAR
DBUS4-	K	L	GNDK	+5V	AT	AU	GNDAT
DBUS5-	M	N	GNDM	NOT USED	AV	AW	GNDAV*
DBUS6-	P	R	GNDP	CA001	AX	AY	GNDAX
DBUS7-	S	T	GNDS	CA002	AZ	BA	GNDAZ
NOT USED	U	V	GNDU*	CA004	BB	BC	GNDBB
STCYL-	W	X	GNDW	CA008	BD	BE	GNDBD
STHED-	Y	Z	GNDY	CA016	BF	BH	GNDBF
CNTRL-	a	b	GNDa	CA032	BJ	BK	GNDBJ
MSEL0-	c	d	GNDc	CA064	BL	BM	GNDBL
MSEL1-	f	g	GNDf	CA128	BN	BP	GNDN
MSEL2-	h	i	GNDh	BUSY-	BR	BS	GNDBR
MSEL3-	j	k	GNDj	ONLIN-	BT	BU	GNDBT
MSEL4-	m	n	GNDm	INDEX-	BV	BW	GNDBV
MSEL5-	p	q	GNDp	UNSAF-	BX	BY	GNDBX
MSEL6-	r	s	GNDr	SKINC-	BZ	CA	GNDBZ
MSEL7-	t	u	GNDt	ENDCYL-	CB	CC	GNDCB
MSEL- (Spare)	v	w	GNDv	PKCHG-	CD	CE	GNDCD
GATTEN0-	x	y	GNDx	WCSEN-	CF	CH	GNDCF
GATTEN1-	z	A	GNDz	HDEXT-	CJ	CR	SHGND
GATTEN2-	AB	AC	GNDAB	CNTGND-	CK	CS	SHGND
GATTEN3-	AD	AE	GNDAD	SPI36V+	CM		
GATTEN4-	AF	AH	GNDAF	36VOUT+	CL		

Table 4-10. DC Cable

Signal Name	Pin No.		Ground
WDATA-	5	3	DCGND
RDATA-	12	25	SHGND
ATTEN-	21	26	GND21
SELM-	22	27	GND22
MSEL-	23	28	GND23

The interface assembly derives its ac *power* through a cable which plugs into an appropriate 110 Vac power source. The interface assembly obtains ***power*** regulation via a two-wire cable connecting the J46 connector on the interface assembly chassis, to edge connector J12 of the nearest power regulator board.

The ac power distribution panel (PDP) has two power cables; one connects to a 110 Vac single phase, the other to a 208 Vac three phase power source.

The first disk drive in the disk subsystem is connected to the PDP via the AC cable. The ac cable is a 7-conductor cable which connects to the female bulkhead connector J1 on the PDP, and to the recessed male bulkhead connector AC IN on the disk drive. In a multiple spindle system, the voltages, input to the first drive must be propagated to the next drive(s) by shorter cable segments. In a multiple spindle system, the phase is also rotated from drive to drive. This phase rotation is accomplished within each drive by cross wiring the pins of the AC IN connector to those of the AC OUT ***connector*** within the disk drive.

Control of the ac distribution by the Power Sequence logic board is enabled by the dual conductor cable from the PDP to the J45 connector on the back panel of the interface assembly chassis. The ac cable is illustrated in Figure 4-7, the **power** regulator cable in Figure 4-4, and the power control cable in Figure 4-24. For physical pin designations, see Figure 4-8. For electrical signal/connector pin designations, refer to Tables 4-11, 4-12 and 4-13. The complete physical cable routing is given in Figure 4-9; for an illustration of the actual cabling see photograph in Figure 4-24. For cable assembly numbers, refer to Table 4-23.

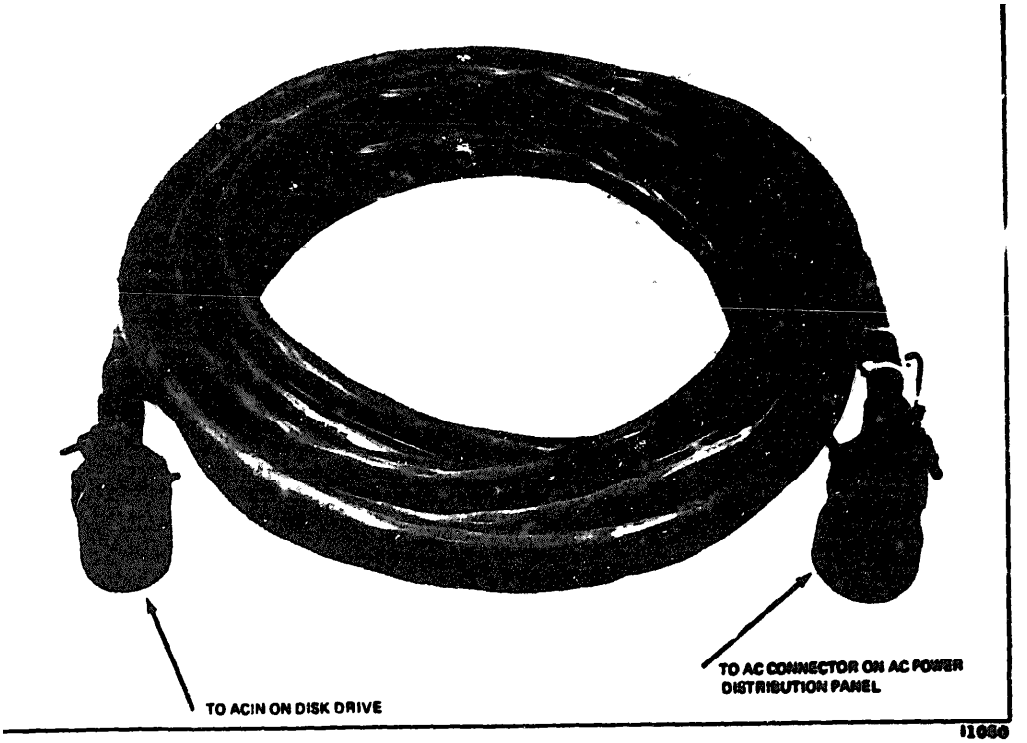

Figure 4-7. AC Cable

4.3.5 Address Patching

The device address is coded by jumpering the patch modules in locations D7 and E8 on the PDC board, as shown in Figure 4-10a. (See also Appendix C, engineering drawing 300337, sheet 21). *For* a ONE bit code jumper the odd numbered input pin (DA00+ thru DA05+) to the corresponding output pin (ADA00+ thru ADA05+). For a ZER0 bit code, jumper the even numbered input pin (DA00-1 thru DA05-1) to the corresponding output pin (DA00+ thru DA05+).

4.3.6 Interrupt and ICI Patching

The interrupt level is coded by jumpering the patch module in location A10 of the PDC board, as shown in Figure 4-10b. (See also Appendix C, engineering drawing 300337, sheet 21). The level is determined by jumpering input term INTR-1 on pin 1 to any one of the output pins 5 thru 13. According to which output pin is selected, term INTR-1 will become term INT08- thru INT15-.

The ICI is coded by jumpering the patch modules in locations A11 and A12 of the PDC board, as shown in Figure 4-10c (see also Appendix C, engineering drawing 300337, sheet 21). The ICI must be enabled by wiring pin 3 to pin 4 on either module. The interrupt level is selected by input term ICIDAT- on pin 1 of both modules,

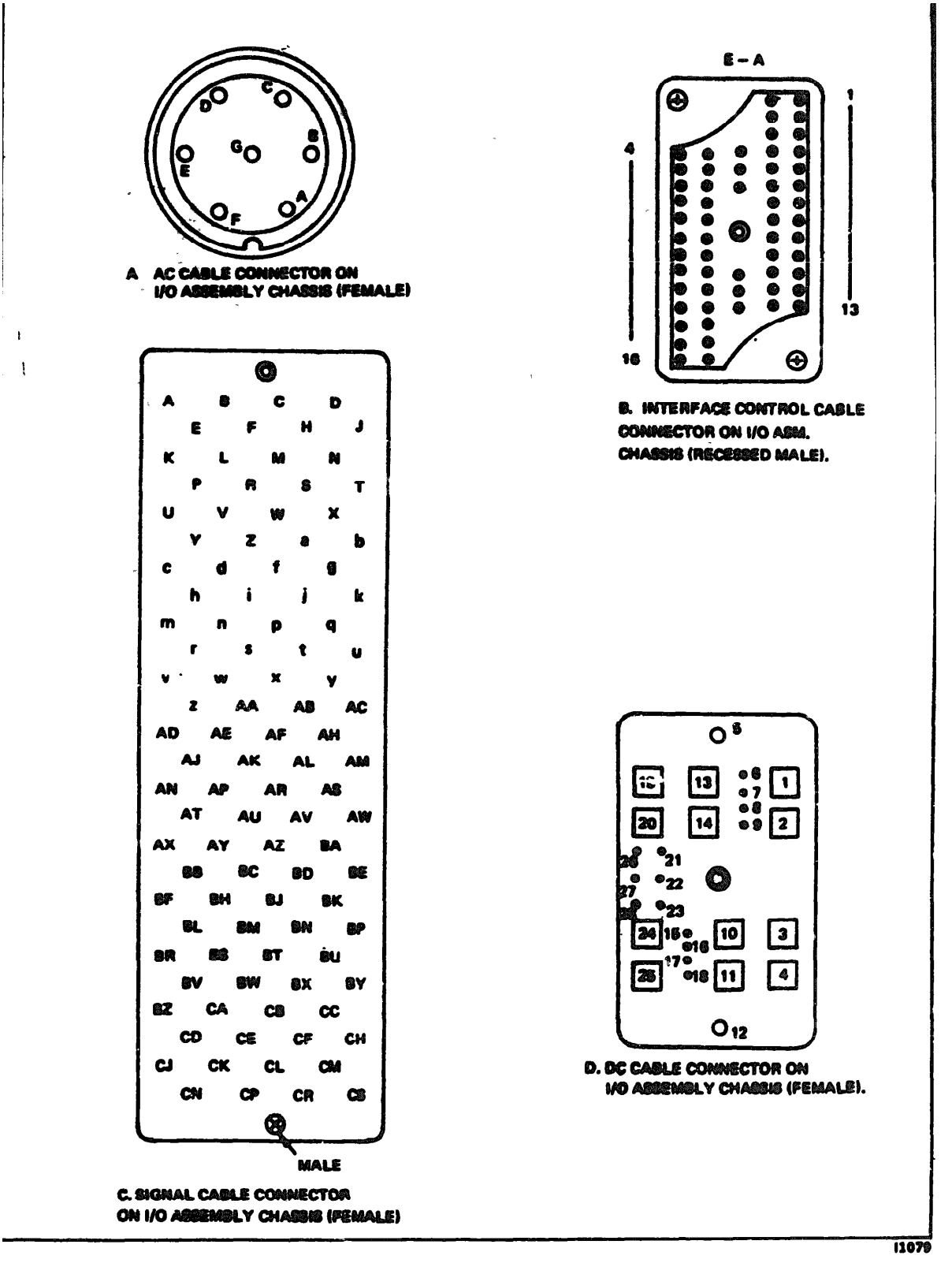

Figure 4-8. Connector Pin Numbering

Table 4-11. AC Cable

Signal Name	Pin No.		Ground
208 VAC	A		
208 VAC	B		
208 VAC	C	G	Ground

Table 4-12. Power Regulator Cable

Signal Name	Pin No.		Ground
KVCTLFP	13		
KVCTLPS	14		

Table 4-13. Power Control Cable

Signal Name	Pin No.		Ground
12 VAC	12		
12 VAC	14		

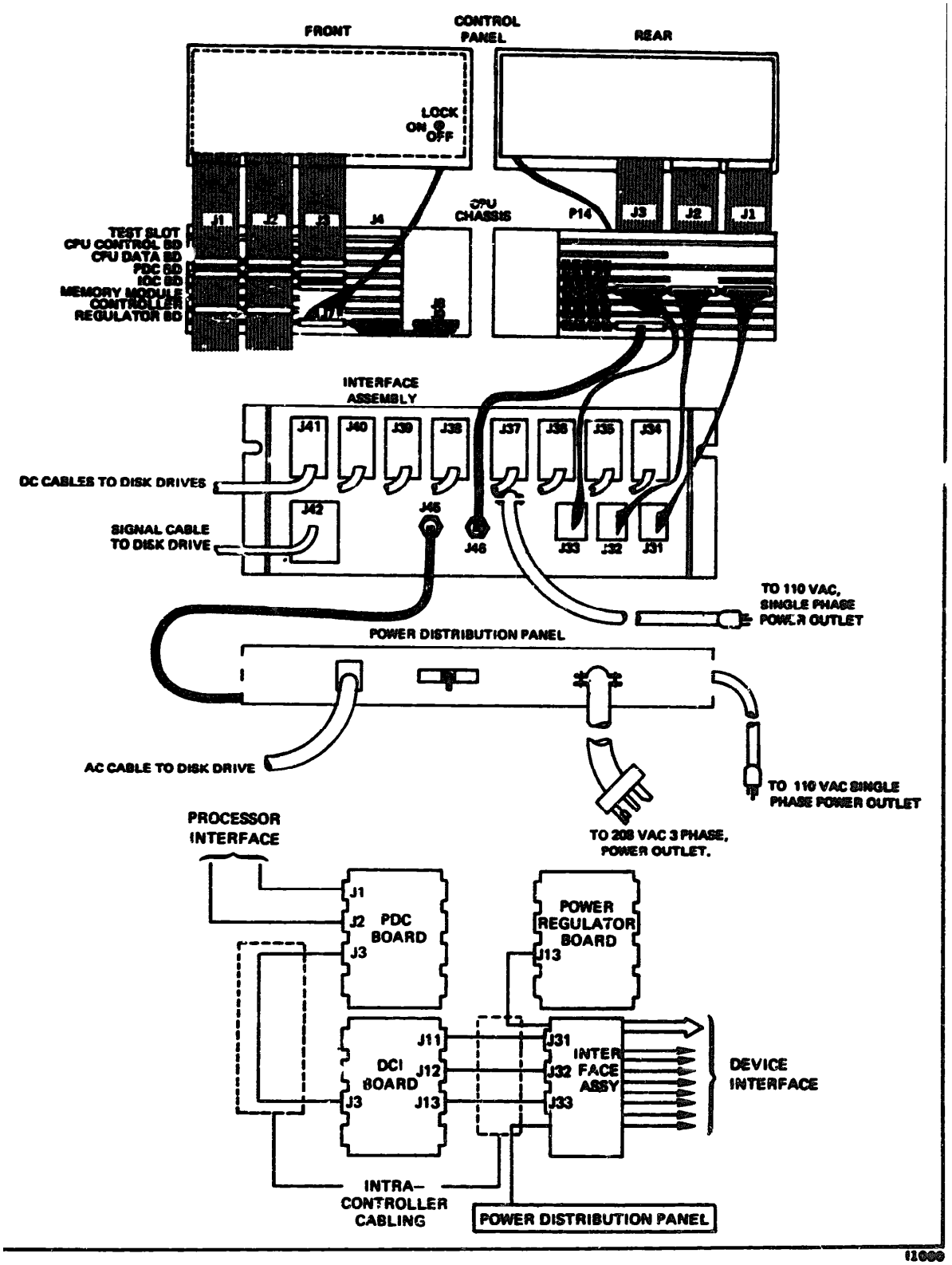

Figure 4-9. IS/1000 Magnetic Disk System, Cabling Layout

to either pin 5 thru 13 of the patch module in location A12 to bring up interrupt term DIB00- thru DIB07-, or to pin 4 thru 13 of the patch module in location A11, to bring up term DIB08- thru DIB15-.

4.3.7 DMA Priority

The DMA priority is coded by jumpering the patch module in location B8, as shown in Figure 4-10d (see also Appendix C, engineering drawing 300337, sheet 28). The DMA priority must be wired in whenever the disk controller shares the DMA channel with **another** DMA using controller.

DMA priority level 1 is coded by jumpering pin 13 to pin 1 and pin 12 to pin 2.

DMA priority level 2 is coded by jumpering pin 13 to pin 2 and pin 12 to pin 3.

DMA priority level 3 is coded by jumpering pin 13 to pin 3.

4.3.8 Patching For Number-of-Drives Indication

If the Magnetic-Disk Subsystem comprises less than five disk drives, a single Simplex card (inserted in slot 22 of the Interface Assembly Card File) suffices, and the patch module in location B6 of the IOL card (slot 16 in the Card File), must be jumpered accordingly, (see Figure 4-10e). If the Magnetic Disk Subsystem comprises *more* than four disk drives, a second Simplex card must be added (inserted in slot 23 of the Interface Assembly Card File).

If the subsystem contains from five to eight disk drives, no patching is necessary. If the subsystem comprises from one to four disk drives, *jumper* the following pins:

- Pin 3 to pin 12.
- Pin 4 to pin 11.
- Pin 5 to pin 10.
- Pin 6 to pin 9.

4.3.9 Drive Type Recognition Patching

Whether the magnetic disk subsystem comprises model 114 or model 213/215 disk drives, must be indicated by jumpering the patch module in location B10 of the DCI board accordingly, as shown in Figure 4-10f.

For model 114 disk drives, jumper pin 3 to pin 11.

For models 213 and 215 disk drives, jumper pin 5 to pin 11.

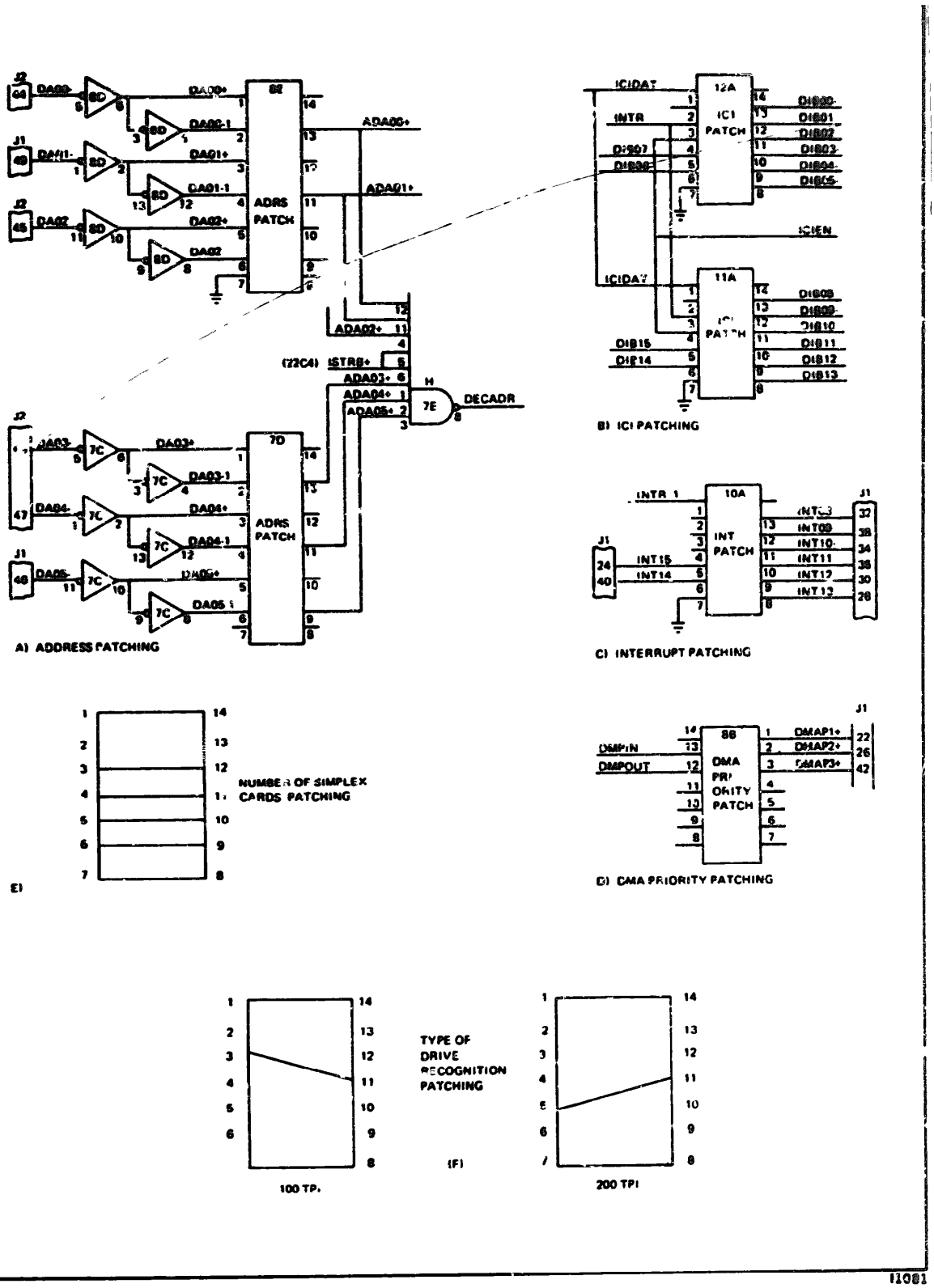

Figure 4-10. Patching

4.4. SERVICING

The design of the IS/1000 system provides for easy access to the logic boards and cards, and facilitates dynamic, in-system testing. The following paragraphs describe replacement and testing procedures of the various controller assemblies.

WARNING

Before attempting removal or installation of any assembly or component, ensure that all electrical power is removed from the* units and** the **chassis to *prevent possible personal injury or equipment damage.

Due care should be exercised at all times when handling the various units during removal, installation and testing of same.

4.4.1 Board Removal

The PDC and DCI boards can be removed as follows: (See Figure 4-11):

a. Turn off electrical power by setting the OFF/ON/LOCK key-operated switch on the processor control panel to OFF.

b. If removal of the ***processor*** control panel is required, first unscrew one of the knurled thumbscrews holding the panel to the ***chassis.*** Then, with one hand holding the panel assembly for support, unscrew the other thumbscrew.

c. While holding the processor control panel assembly with one hand, carefully disconnect the three flat ribbon cables from the J1, J2 and J3 edge connectors, and the *power* regulator cable from J7.

d. Place the processor control panel on a suitable, soft, preferably cushioned surface.

e. In front, remove the flat ribbon cable from edge connector J3 of PDC. and DCI boards alike. *For the* PDC board, additionally remove the internal interface cables from edge connectors J1 and J2.

f. In back, loosen with a screwdriver the six screws securing the device interface control cables to edge connectors J11, J12, and J13 **of** the DCI board and disconnect the cables.

g. In front, loosen and remove screws holding the logic board retaining strip to the left inside wall of the card cage. Remove the retaining strip.

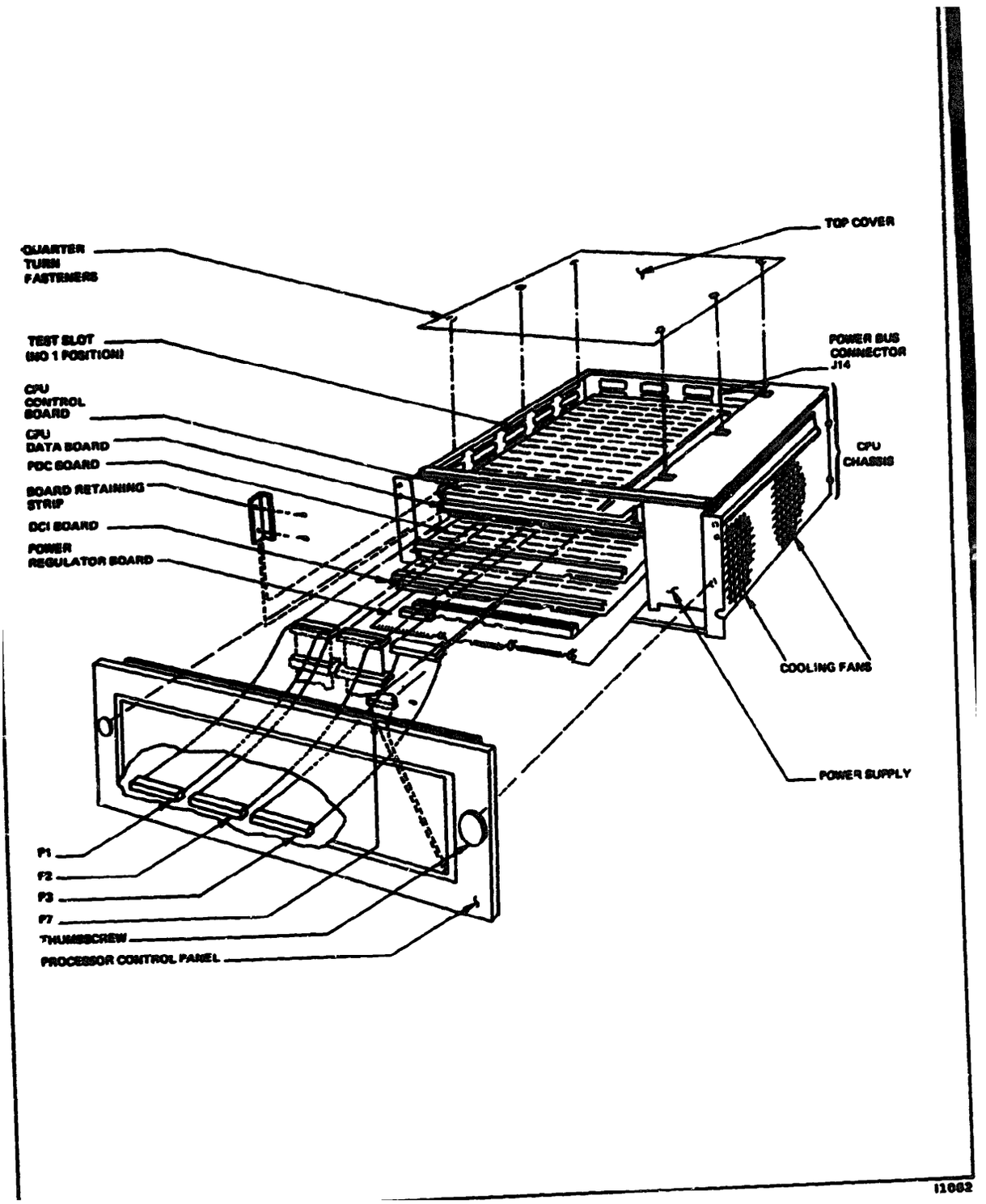

Figure 4-11. Card Cage and PCP Assembly.

h. **From the front of the chassis, pull the board to be removed forward with evenly applied controlled force, until the power edge connector P14 disengages from the backplane power supply bus. Gently slide the board out of the chassis.**

i. Place the board ***on*** a suitable, soft, preferably cushioned surface, or ***put*** in an appropriate container.

j. If applicable, re-install the board retaining strip.

k. If applicable, re-install the processor control panel, per procedural steps k and l of Board Installation paragraph 4.4.2.

4.4.2 Board Installation

The PDC and IOC boards can be installed as follows:

a. Turn off electrical power by setting the OFF/ON/Lock key-operated switch on the processor control panel, to OFF.

b. If applicable, remove processor control panel following procedural steps b, c and d of Board Removal paragraph 4.4.1.

c. If applicable, remove the logic board retaining *strip* according to step g of the Board Removal paragraph 4.4.1.

d. From the front, guide the board into the appropriate chassis slot, ensuring that the board properly engages the guide rails on both sides of the chassis.

e. Gently slide the board into the chassis until the power edge connector P14 contacts the power supply bus J14. Sliding action should be smooth. If an ***obstruction is*** encountered, do *NOT* force board insertion; instead, remove board and investigate problem.

f. With controlled ***force*** push the board back into the chassis, until J14 fully engages P14 and the board is completely contained within the chassis.

g. Replace the board retaining strip against the left inside wall of the chassis, and fasten with screws.

h. Clean all connectors that have been handled with a cotton swab dipped in Freon TP or denatured alcohol.

i. In front, connect the flat ribbon cable to edge connector J3 of PDC and DCI boards alike. For the PDC board, also connect the two internal interface cables to edge connectors J1 and J2.

j. In back, connect the device interface control cables from the device interface assembly connectors J31, J32 and J33, to edge connectors J11, J12 and J13 of the IOC board, respectively. Secure the cable connectors to the IOC board, by fastening the connecter side screws.

k. If required, support the processor control panel with one hand, carefully connect the three flat ribbon cables to the J1, J2 and J3 edge ***connectors.*** Connect the power regulator cable from the power regulator board to J7.

l. Place the processor control panel in position against the card cage chassis, and secure by fastening the two thumbscrews on both sides of the panel.

4.4.3 Board Test

The PDC or DCI board, when suspect of intermittent failure, can be dynamically tested within the system by placing the board in the test slot, location 1 of the card cage ***chassis.*** The signal cabling can be temporarily modified if necessary, through the use of test cables (refer to Table 4-23 for assembly number), as shown in Figure 4-12. The chassis slides out and the top cover plate is removed for complete access to the logic board.

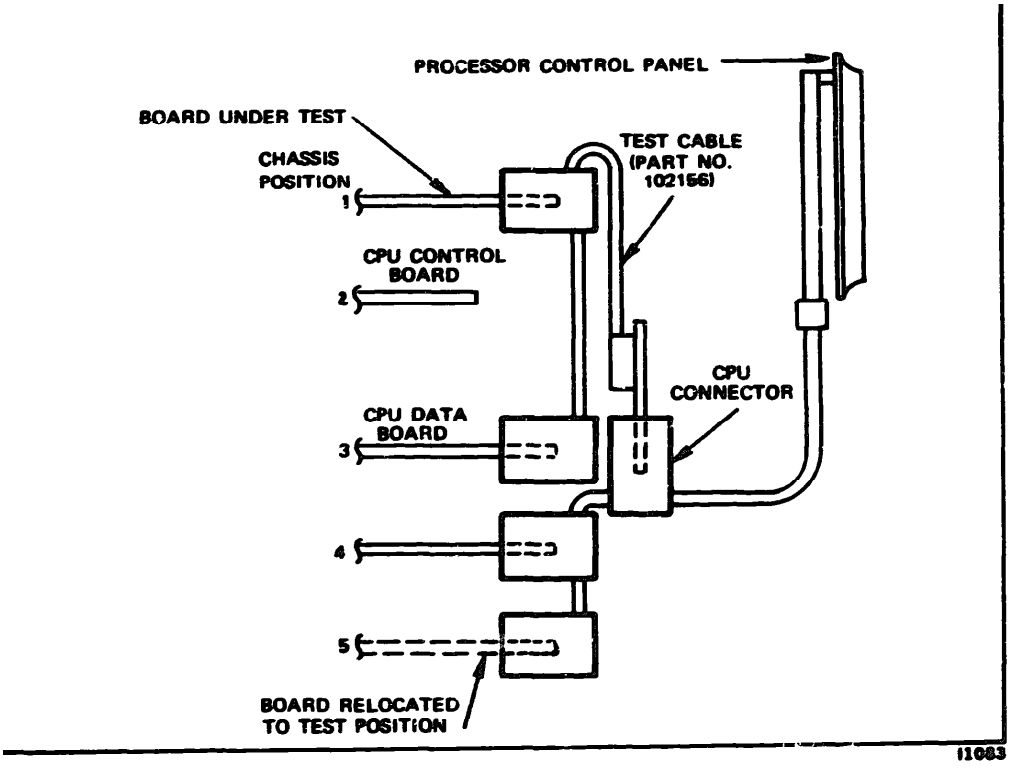

Figure 4-12. Test Cable Connection

The **PDC board is shown** in Figure 4-13; the DCI board is shown in Figure 4-14. The boards are viewed from the component side. The physical pin designations of the edge connectors are also shown. Note that the 30-pin connectors are odd numbered on the component side and even on the etch side of the boards. The 50-pin connectors are numbered in reverse, even on the component side, odd on the etch side. The electrical pin designations are listed alphabetically by mnemonic in Tables 4-2 through 4-4 for the PDC board, and in Tables 4-5 through 4-8 for the DCI board. *For* numerical by *pin* number signal assignments refer to sheet 4 of engineering drawings 300337 and 300352, respectively, in Appendix C.

For a test set-up of either the PDC *or* DCI board, proceed as follows:

a. Turn off electrical power by setting the OFF/ON/LOCK key operated switch on the processor control panel, to OFF.

b. Temporarily *remove* the processor control panel per procedural steps b, c and d of Board Removal paragraph 4.4.1.

c. Remove all cabling in front and rear of the board to be tested, per procedural steps e and f of Board **Removal** paragraph 4.4.1.

d. Remove the board retaining *strip* securing the board in position.

e. From the front of the chassis, pull the board to be tested forward with evenly applied controlled force, until the power edge connector P14 disengages from the **backplane** power supply bus. Gently slide the board out of the chassis.

f. Insert the board into the test slot, i.e., the number 1 (top) board position in the chassis, right above the CPU control board. Slide the board in all the way until the power edge connector P14 contacts the power supply bus P14. With controlled force push the board back into the chassis until J14 fully engages P14 and the board is completely contained within the chassis.

g. Loosen and remove the screws securing the card cage chassis to the cabinet frame.

h. Recable the boards per procedural steps h, i, and j of Board Installation paragraph 4.4.2.

i. Re-install the processor control panel per procedural steps k and l of Board installation paragraph 4.4.2.

j. Pull the card cage forward and all the way out.

k. Loosen the six quarter-turn fasteners holding the top cover to the chassis, and remove top cover. The board to be tested is now completely accessible and can be tested under operational conditions.

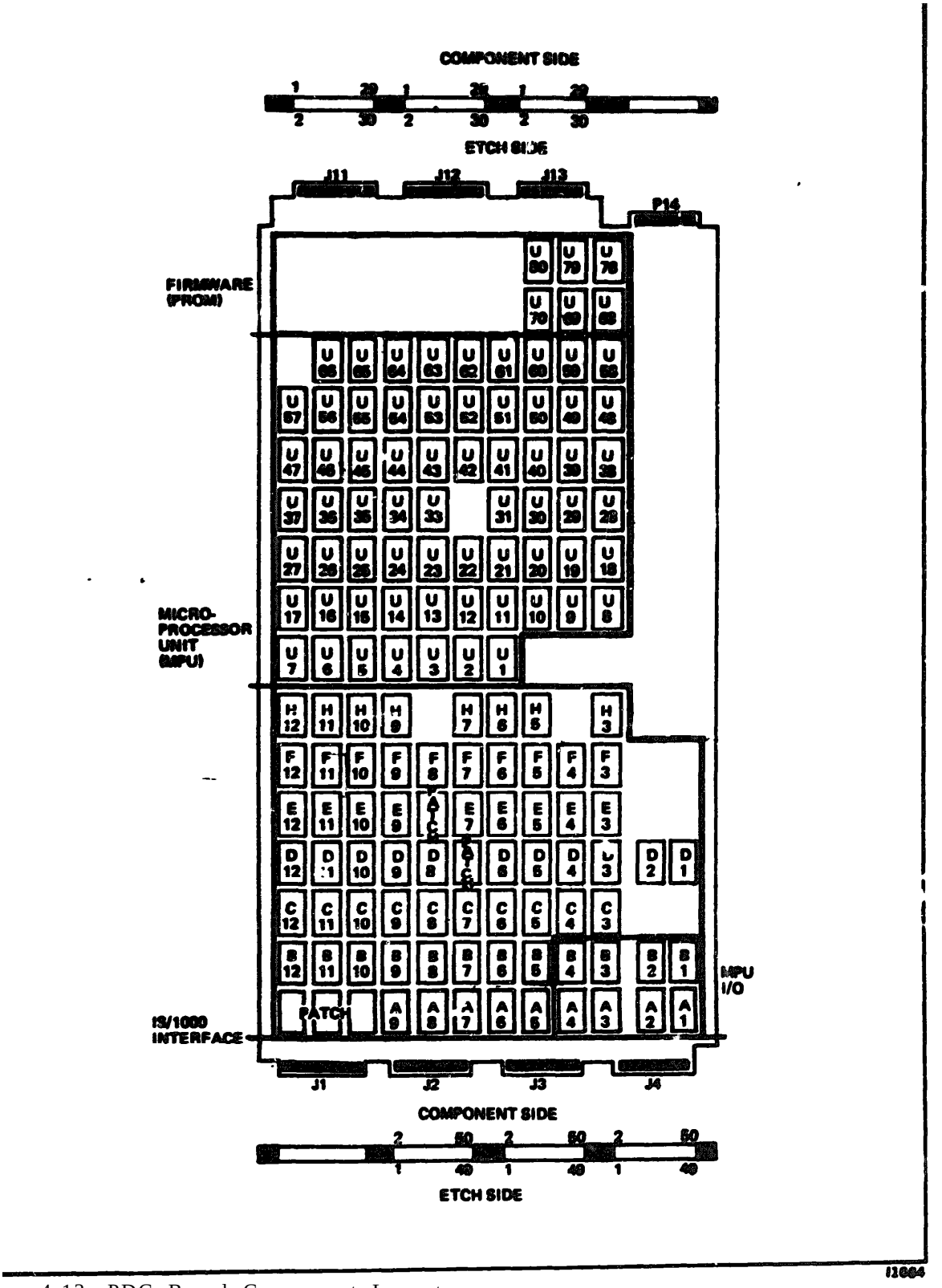

Figure 4-13. PDC Board Component Layout

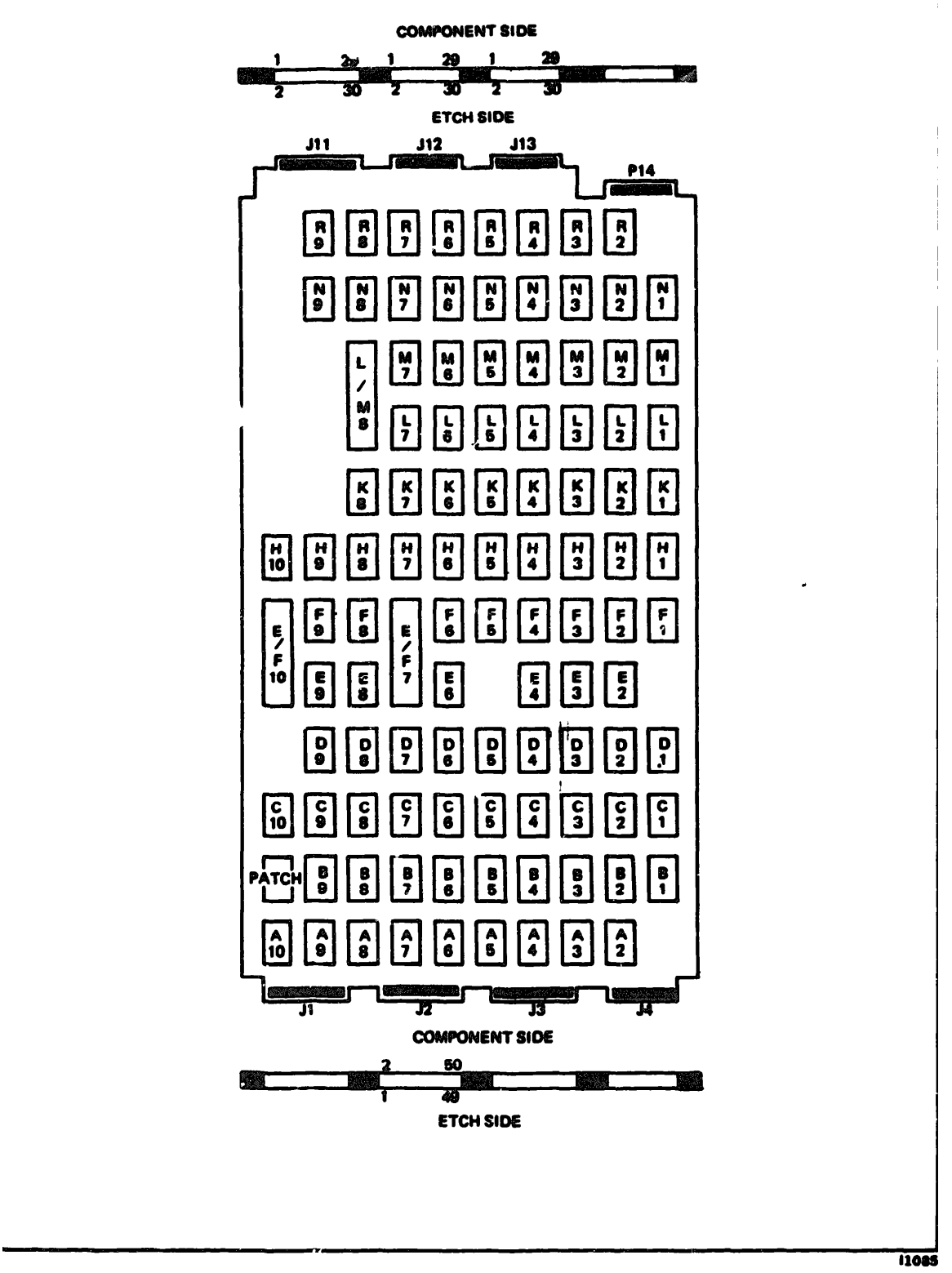

Figure 4-14. IOC Board Component Layout

4.4.4 Card Removal

All cards in the card file can be removed as follows:

a. Turn off electrical power by setting the OFF/ON/LOCK key operated switch on the processor control panel to OFF.

b. If applicable, open the front door or front cover.

c. With both hands, grasp the card to be removed, firmly between thumb and index finger of each hand at top and bottom at the front edge.

d. Evenly apply controlled force to pull the card forward and out of the edge connector.

e. After the edge connectors disengage, slide the card gently out of the card slot.

4.4.5 Card Installation

All cards can be installed into the card file as follows:

a. Turn off electrical power by setting the OFF/ON/LOCK key operated switch on the processor control panel to OFF.

b. If applicable, open front door or front cover.

c. Guide the card into the appropriate card slot, ensuring that the card properly engages the top and bottom guide rails.

d. Gently slide the card into the chassis until the edge connector contacts the edge connector receptacle.

e. With controlled force push the card back into the chassis until it **is** fully seated in the edge connector receptacle.

4.4.6 Card Test

All cards in the card file, when suspect of intermittent failure, can be dynamically tested within the system, by extending the card outside the card file chassis, as **shown** in Figure 4-15. **This** can be accomplished as follows:

a. Turn off electrical power by setting the *OFF/ON/LOCK* key operated switch on the processor control panel to OFF.

b. If applicable, open the front door or front cover.

c. Remove card to be tested using steps c, d, and e of Card Removal paragraph 4.4.4.

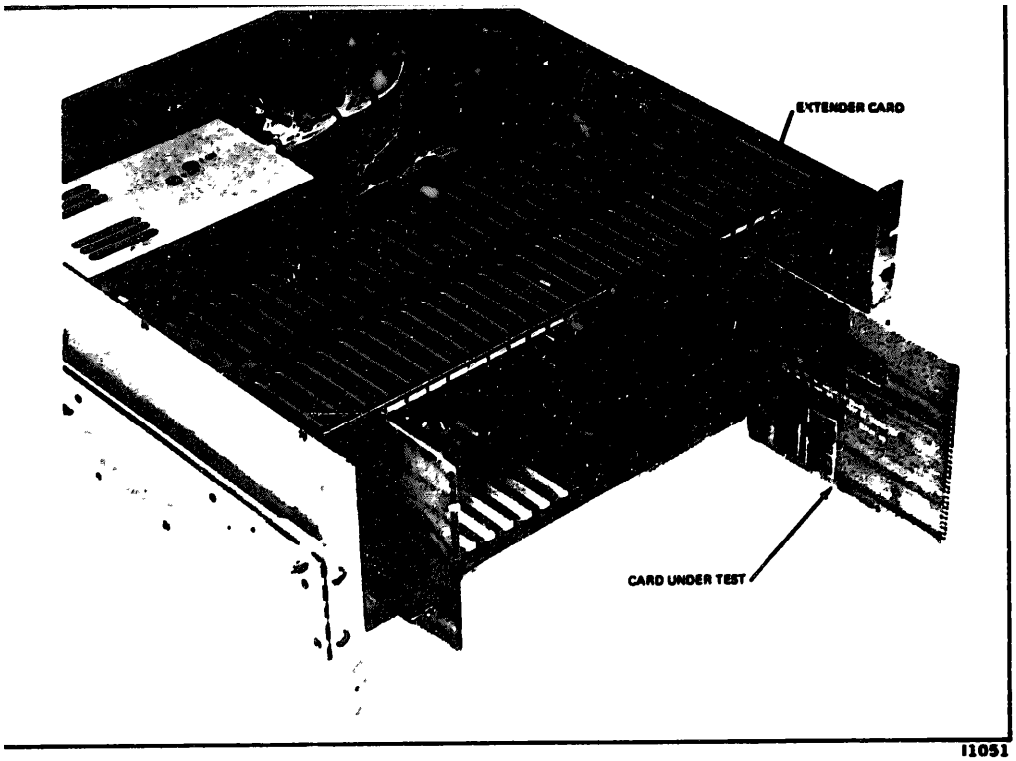

Figure 4-15. Card Test Set-up

d. Insert extender card, assembly number 101158, into **location** of the just removed card, using steps c, d and **e of Card** Installation paragraph 4.4.5.

e. Insert card to be tested into the edge connector **receptacle at** front edge of the extender card. The **card** to **be tested is** now completely accessible and can be tested under operational conditions.

The IOL (interface logic) card is shown in Figure 4-16, the PLO (phase locked oscillator) card in Figure **4-17,** the **SMX (simplex) and** MUX (multiplex) cards in Figures 4-18 and 4-19 respectively, and the ***PSQ*** **(power** sequencer) card in Figure 4-20. Figure 4-21 shows the extender card, which is used to test any of the other **cards.**

The cards **are** all viewed from the component side. The physical pin designations of the edge connectors are also shown. As can be seen the 80-pin edge connectors are odd numbered on the component side and even on the etch side of the cards.

The electrical pin designations, i.e., logic signal name and ground pin assignments, are listed alphabetically by mnemonic in **Tables** 4-14 through 4-22. For numerical by pin number signal assignments, refer to engineering drawings 300112, 300332, 300333, 300334 and 300364, in Appendix C.

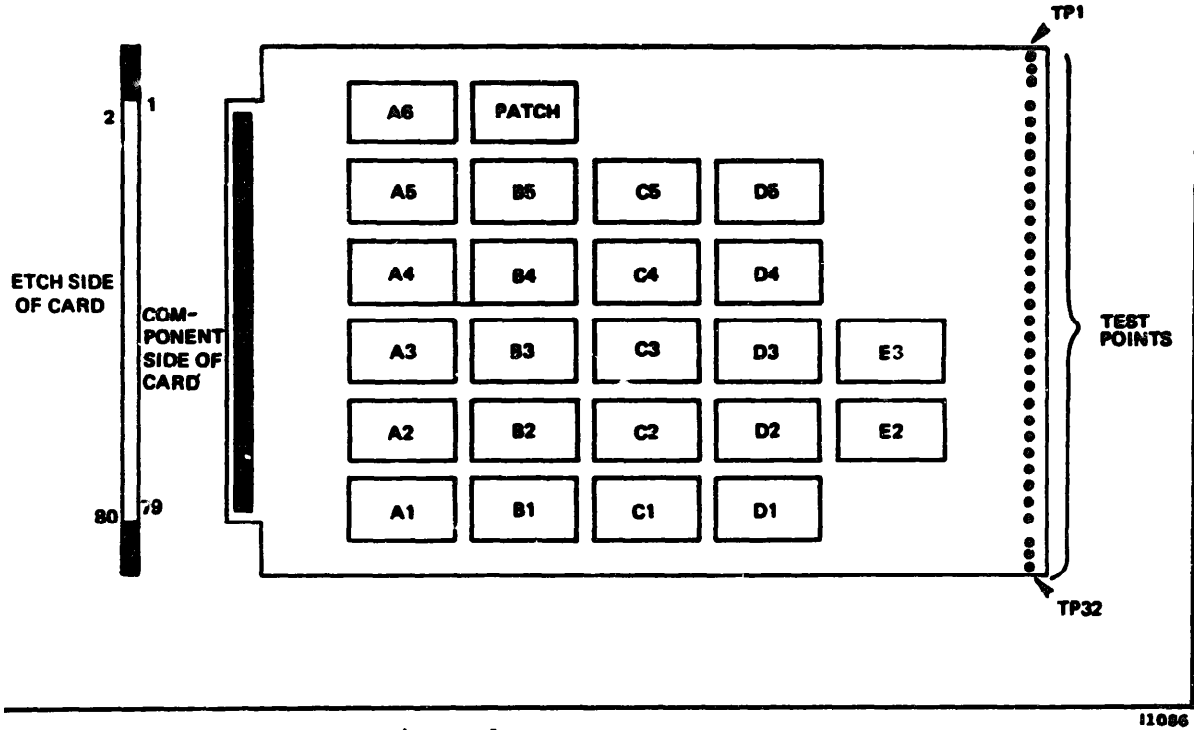

Figure 4-16. Interface Logic Card Component Layout

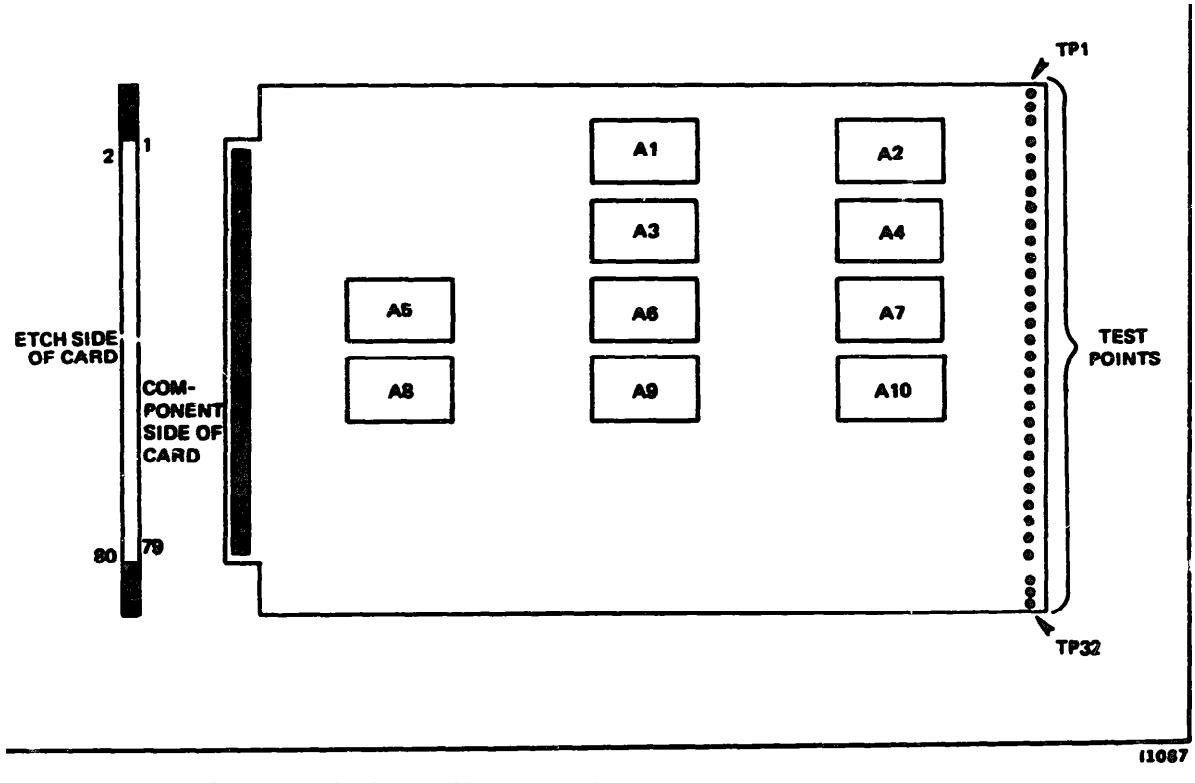

Figure 4-17. **Phase** Locked Oscillator Card Component Layout

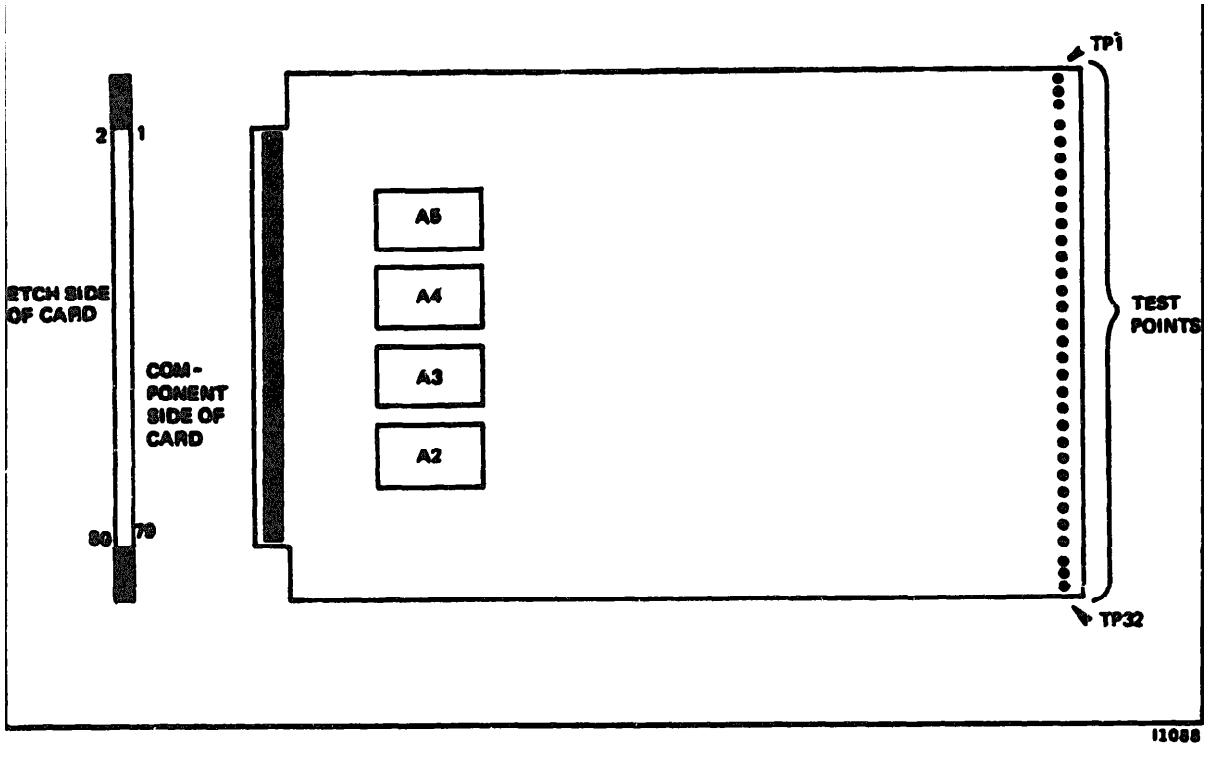

Figure 4-18. Simplex Card Component Layout

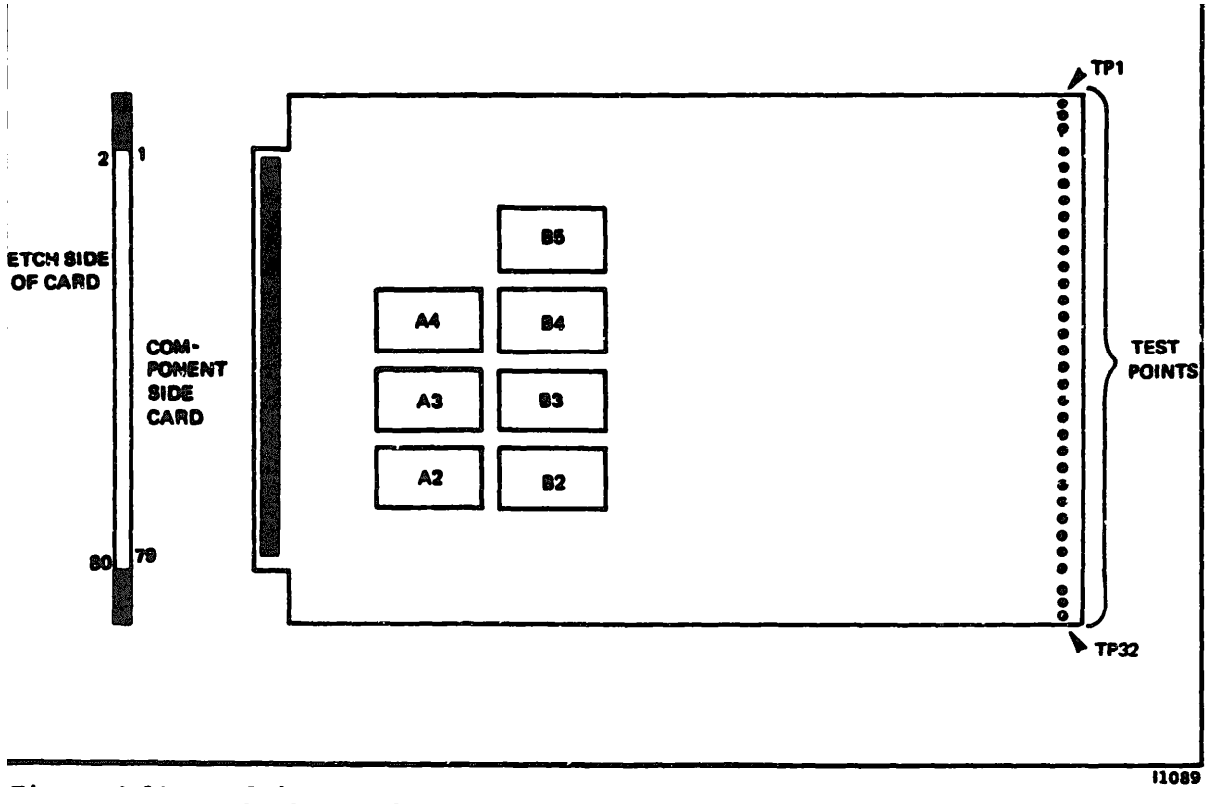

Figure 4-19. Multiplex card Component Layout

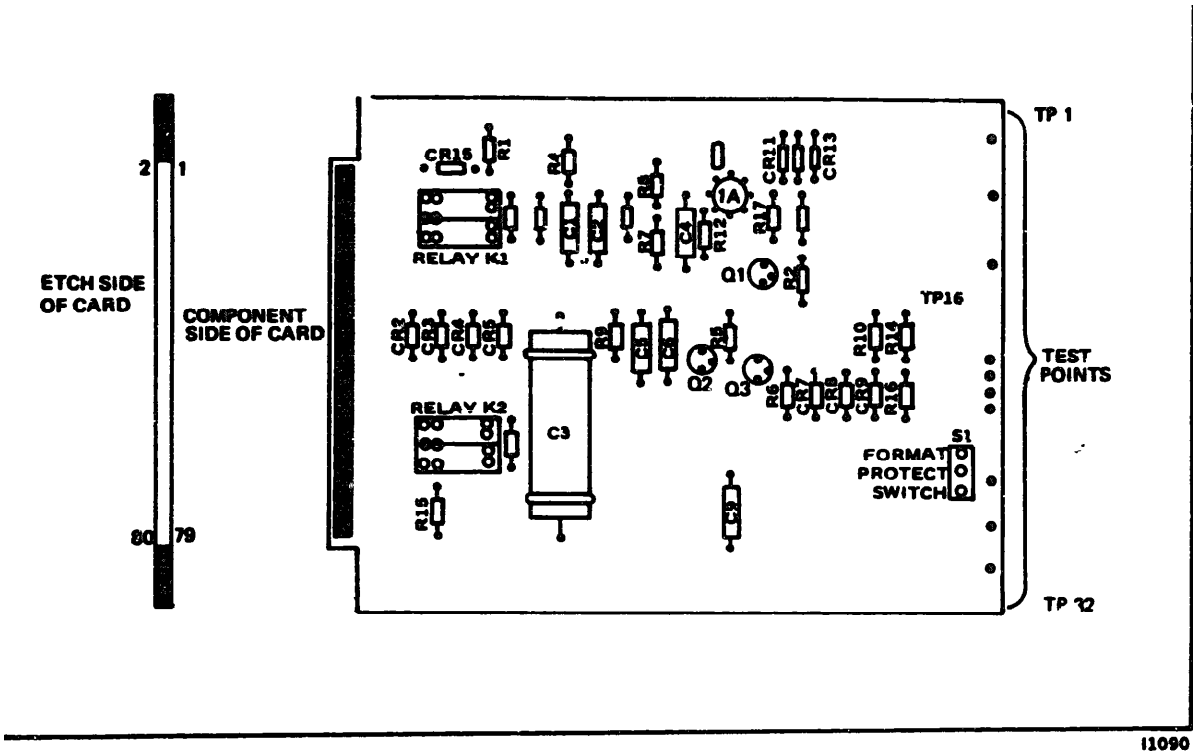

Figure 4-20. Power Sequence Card Component Layout

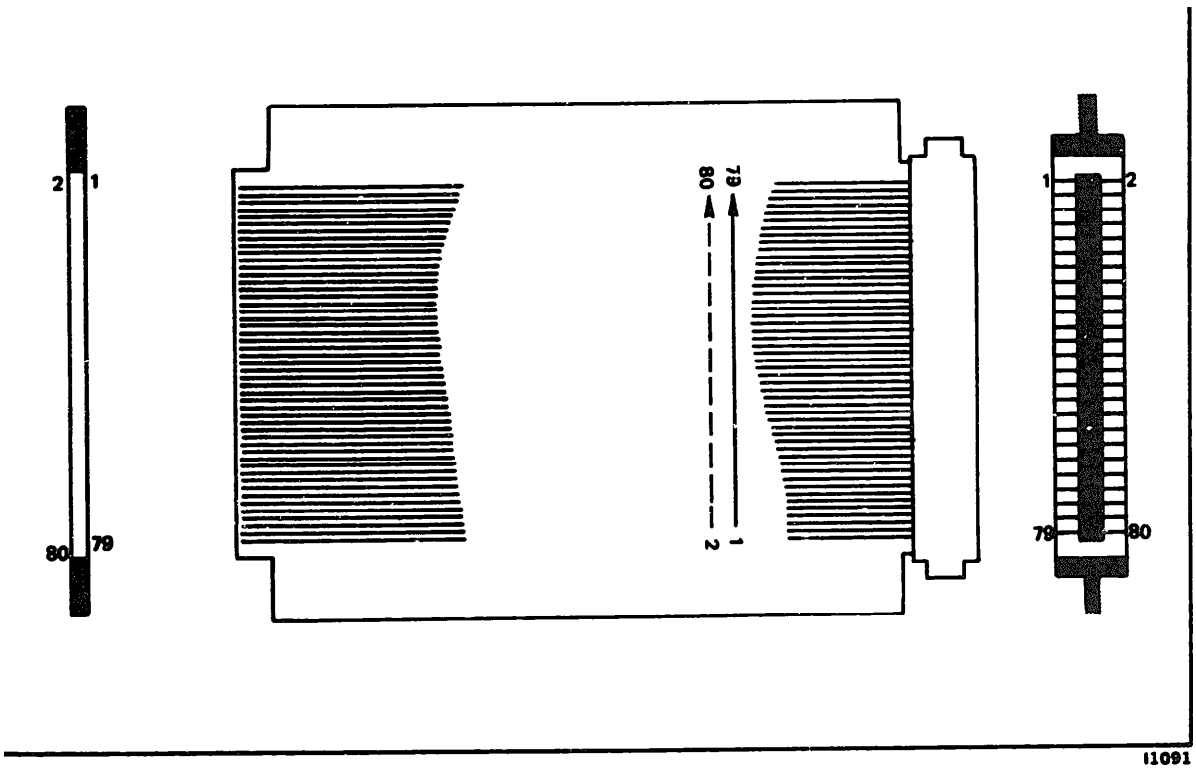

Figure 4-21. Extender Card

Table 4-14. IOL Card, Edge Connector J1

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
CKA2-	64	4	GND	ONOTRY-	55		
CKB2-	65	72	GND	OWTDAT-1	11		
CNTRL-1	47	74	GND	RDDAT0+	23		
DBUS5-1	46	76	GND	RDDAT1+	17		
DMSEL0+	51			RDDAT2+	18		
DMSEL1+	52			RDDAT3+	24		
DMSEL2+	53			RDDAT4+	31		
DMSEL3+	50			RDDAT5+	32		
DMSEL4+	49			RDDAT6+	38		
DMSEL5+	58			RDDAT7+	37		
DMSEL6+	57			RDDAT-1	66		
DMSEL7+	48			SEPCK+	68		
DSERR-1	63			SEPONE-	13		
DSLDM0+	21			SRDDAT0-	22		
DSLDM1+	20			SRDDAT1-	19		
DSLDM2+	15			SRDDAT2-	14		
DSLDM3+	25			SRDDAT3-	26		
DSLDM4+	30			SRDDAT4-	29		
DSLDM5+	33			SRDDAT5-	34		
DSLDM6+	39			SRDDAT6-	40		
DSLDM7+	36			SRDDAT7-	35		
ENWROS+	27			SYNC-1	45		
FDEVA1-1	61			VFO+	54		
FDEVA2-1	60			WRTCK-	43		
FDEVA4-1	59			WRTDAT+	12		
FINHCK-1	28			WRTDAT-1	44		
FLIP-	62			XTAL+	56		
FSEP-	41			+5V	73		
FSEP+	42			+5V	75		
NOCK-1	67			+5V	77		

Table 4-15 PLO Card Edge Connector J1

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
OWTDAT+1	38	76	GND	SRDDAT5-	58		
OWTDAT-1	50			SRDDAT6-	56		
ENWROS+	24			SRDDAT7-	54		
FLIP-	30			SEPCK+	42		
FSEP+	25			SEPCK-	36		
FSEP+	33			SEPONE+	46		
ONOTRY+	27			SEPONE-	44		
ONOTRY-	32			VFO+	67		
SRDDAT0-	68			VFO-	48		
SRDDAT1-	66			WRTCK-	22		
SRDDAT2-	64			XTAL+	20		
SRDDAT3-	62			+5V	77		
SRDDAT4-	60			+10V	80		
					4		GND

Table 4-16. PSQ Card, Edge Connector J1

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
CNTRST	67			WCNTGD-	61		
COM	4			WINDEXT-	63		
COM	76			-3Vdc	5		
KVCTL+	49			12Vac	46		
KVCTL-	25			12Vac	44		
SWFMTP-	65						

Table 4-17. SMX Card, Edge Connector J1, Card Slot 22

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
DSLDM0+	8	4	GND	SELM2-	34	33	GND
DSLDM1+	18	7	GND	SELM3-	44	35	GND
DSLDM2+	28	9	GND	WDAT+	56	37	GND
DSLDM3+	38	11	GND	WDAT+	58	39	GND
RDATA0-	12	13	GND	WDAT+	60	41	GND
RDATA1-	22	15	GND	WDAT+	62	43	GND
RDATA2-	32	17	GND	WDATA0-	16	45	GND
RDATA3-	42	19	GND	WDATA1-	26	55	GND
RDDAT0+	10	21	GND	WDATA2-	36	57	GND
RDDAT1+	20	23	GND	WDATA3-	46	59	GND
RDDAT2+	30	25	GND	+5V	73	61	GND
RDDAT3+	40	27	GND	+5V	75	76	GND
SELM0-	14	29	GND	+5V	77		
SELM1-	24	31	GND				

Table 4-18. SMX Card, Edge Connector J1, Card Slot 23

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
DSLDM4+	8	4	GND	SELM6-	34	33	GND
DSLDM5+	18	7	GND	SELM7-	44	35	GND
DSLDM6+	28	9	GND	WDAT+	56	37	GND
DSLDM7+	38	11	GND	WDAT+	58	39	GND
RDATA4-	12	13	GND	WDAT+	60	41	GND
RDATA5-	22	15	GND	WDAT+	62	43	GND
RDATA6-	32	17	GND	WDATA4-	16	45	GND
RDATA7-	42	19	GND	WDATA5-	26	55	GND
RDDAT4+	10	21	GND	WDATA6-	36	57	GND
RDDAT5+	20	23	GND	WDATA7-	46	59	GND
RDDAT6+	30	25	GND	+5V	73	61	GND
RDDAT7+	40	27	GND	+5V	75	76	GND
SELM4-	14	29	GND	+5V	77		
SELM5-	24	31	GND				

Table 4-19. MUX Card, Edge Connector J1, Card Slot 18

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
ATTEND0-1	36	4	GND	DBUS3-1	56	37	GND
ATTEN1-1	34	11	GND	DMSEL0+	66	39	GND
BUSY-	18	13	GND	DMSEL1+	68	49	GND
BUSY-1	32	15	GND	GATTEN0-	22	51	GND
CA001-	26	17	GND	GATTEN1-	20	53	GND
CA002-	24	19	GND	HDEXT-	14	55	GND
CA004-	12	21	GND	HDEXT-1	40	57	GND
DBUS0-	28	23	GND	MSEL0-	60	59	GND
DBUS1-	30	25	GND	MSEL1-	58	63	GND
DBUS2-	64	27	GND	ONLIN-	16	65	GND
DBUS3-	62	29	GND	ONLIN-1	38	67	GND
DBUS0-1	50	31	GND	+5V	73	76	GND
DBUS1-1	52	33	GND	+5V	75		
DBUS2-1	54	35	GND	+5V	77		

Table 4-20. MUX Card, Edge Connector J1, Card Slot 19

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
ATTEN2-1	36	4	GND	DMSEL2+	66	35	GND
ATTEN3-1	34	11	GND	DMSEL3+	68	37	GND
CA008-	26	13	GND	GATTEN2-	22	39	GND
CA016-	24	15	GND	GATTEN3-	20	49	GND
CA032-	12	17	GND	INDEX-	18	51	GND
DBUS4-	28	19	GND	INDEX-1	32	53	GND
DBUS5-	30	21	GND	MSEL2-	60	57	GND
DBUS6-	64	23	GND	MSEL3-	58	59	GND
DBUS7-	62	25	GND	UNSAF-	16	63	GND
DBUS4-1	50	27	GND	UNSAF-1	38	65	GND
DBUS5-1	52	29	GND	+5V	73	67	GND
DBUS6-1	54	31	GND	+5V	75	76	GND
DBUS7-1	56	33	GND	+5V	77		

Table 4-21. MUX Card, Edge Connector J1, Card Slot 20

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
ATTEN4-1	36	4	GND	GATTEN5-	20	37	GND
ATTEN5-1	34	11	GND	MSEL4-	60	39	GND
CA064-	26	13	GND	MSEL5-	58	49	GND
CA128-	24	15	GND	SKINC-	18	51	GND
CA256-	12	17	GND	SKINC-1	32	53	GND
CNTRL-	62	19	GND	STCYL-	30	55	GND
CNTRL-1	56	21	GND	STCYL-1	52	57	GND
DBUS8-	28	23	GND	STHED-	64	59	GND
DBUS8-1	50	25	GND	STHED-1	54	61	GND
DMSEL4+	66	27	GND	+5V	73	63	GND
DMSEL5+	68	29	GND	+5V	75	65	GND
ENDCYL-	16	31	GND	+5V	77	67	GND
ENDCYL-1	38	33	GND			76	GND
GATTEN4-	22	35	GND				

Table 4-22. MUX Card, Edge Connector J1, Card Slot 21

Signal Name	Pin No.		Ground	Signal Name	Pin No.		Ground
ATTEN6-1	36	4	GND	+5V	77	37	GND
ATTEN7-1	34	11	GND			39	GND
DMSEL6+	66	13	GND			49	GND
DMSEL7+	68	15	GND			51	GND
GATTEN6-	22	17	GND			53	GND
GATTEN7-	20	19	GND			55	GND
MSEL6-	60	21	GND			57	GND
MSEL7-	58	23	GND			59	GND
PKCHG-	18	25	GND			61	GND
PKCHG-1	32	27	GND			63	GND
WCEN-	16	29	GND			65	GND
WCEN-1	38	31	GND			67	GND
+5V	73	33	GND			76	GND
+5V	75	35	GND				

From one to thirty-two test points, designated as TP1 through TP32, are available on the outer edge of each card on the component side.

As can be seen from Figure 4-21, the Extender card provides straight one-for-one signal propagation from the socket in the chassis slot, to the card under test.

4.4.7 Interface Assembly Removal

The Interface Assembly is shown in Figure 4-22. Refer also to Figure 4-24, where necessary, for an illustration of the cable and connector locations, when performing the cable connect/disconnect installation and removal steps.

a. Turn *off* electrical *power* by setting the *OFF/ON/LOCK* key operated switch *on* the *processor* control panel to OFF.

b. If applicable, open front and rear *doors* or covers of the cabinet.

c. Disconnect the power cable going to the *Power* Distribution Box (PDB), from the 110 Vac switched outlet on the *PDB.*

d. Disconnect the ac control cable (Figure 4-7 and 4-9) from J45. Release connector by holding it between thumb and index finger, **pressing** forward on the forward slanted lip with thumb, and backward on the backward slanted lip with index finger. Then remove by evenly pulling the plug backward.

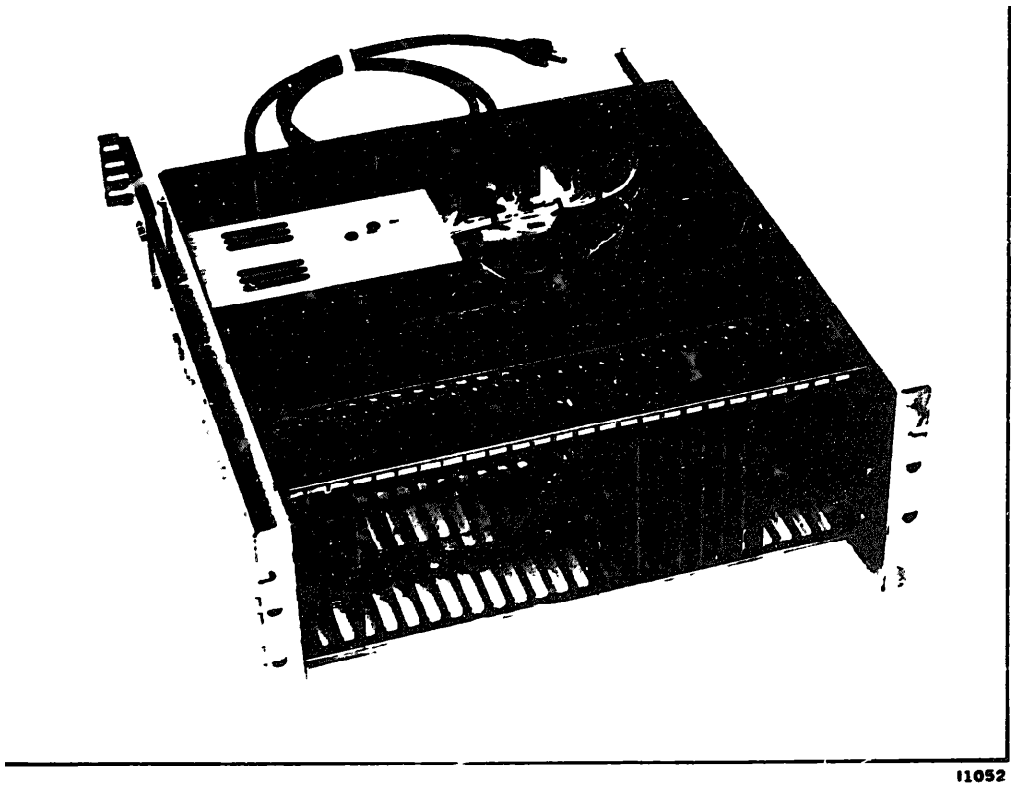

Figure 4-22. Interface Assembly

e. Disconnect the power regulator cable (Figure 4-4 and 4-9) from J46. Release and remove connector as described in preceding step d for the ac control cable.

f. Disconnect any DC cable(s) from J34, J35, J36, J37, J38, J39, J40 or J41 (Figure 4-6 and 4-9). Disconnect the cables(s) as follows:

- With a flat screwdriver, loosen the retaining screw on the back of the connector bulkhead.
- With one hand cupped under the connector bulkhead for support, rotate the retaining screw counter-clockwise with the **other** hand.
- Hold and guide the cable and connector so that the **connector and** receptacle *faces* **remain** parallel to each other while separating. This prevents pins **from** bending and **other** connector damage from occurring.

g. Disconnect the three interface control cables (Figure 4-4 and 4-9) from connectors J31, J32 and J33. Disconnect each cable following the procedure given in the preceding step f for removal of the dc cable.

h. Disconnect the signal cable (Figure 4-5 and 4-9) from connector J42. Disconnect the cable as ***follows:***

- With a long narrow flat screwdriver, loosen and turn the bottom retaining ***screw*** one full turn counter-clockwise.
- Repeat for the top retaining screw.
- Continue to alternately turn each screw one full turn counterclockwise until the bottom **screw** completely disengages.
- Hold the cable and connector bulkhead steady with one **hand** while turning the top retaining screw counterclockwise until it too completely disengages.

This enables the **connector** to separate from the receptacle in an even manner, with connector and receptacle faces remaining parallel with each **other,** thus preventing pin bending and other *connector* damage, which may later become the source of hard to diagnose intermittent failures.

NOTE: It is recommended that the next step be performed by two persons.

i. With a Phillips *screwdriver,* loosen and remove the screws **attaching** the sliding rails in front and rear of the cabinet, to the frame. During removal of the screws, another ***person*** should assist in holding **and supporting** the chassis to prevent it from dropping. The chassis can then be lifted out of the cabinet.

4.4.8 Interface Assembly Installation

The interface assembly (Figure 4-22) can be installed as follows:

a.. Turn off electrical power by setting the OFF/ON/LOCK key operated switch on the processor control panel to OFF.

b. If applicable, open front end **rear** *doors* or covers *of* the cabinet.

NOTE: ***It is recommended that the next step be*** performed by two ***persons.***

c. Position the chassis in the cabinet at the desired height. Fasten the sliding rails in front and rear of the cabinet, to the cabinet frame.

d. Connect the signal cable (Figure 4-5 and 4-9) to connector J42. Connect the cable as follows:

- Place the connector bulkhead in position, opposite and as close as possible to the connector receptacle, holding and supporting the connector bulkhead with one hand so that its face is parallel with that of the receptacle.
- With a long narrow flat screwdriver, engage the top retaining screw and turn it one full turn clockwise.
- **Repeat** for the bottom retaining screw.
- Continue to alternately turn each screw one full turn clockwise, until the two connector halves are fully engaged. Gently tighten each screw with an additional quarter turn.

This enables the connector to engage the receptacle as straight and evenly as possible, thus preventing pin bending and connector damage due to uneven stresses.

e. Connect the three interface control cables (Figure 4-4 and 4-9) coming from DCI board ***connectors*** J11, J12 and J13, to connectors J31, J32 and J33 respectively. Connect each cable as follows:

- With one hand, hold and guide the connector so that it is precisely aligned with the receptacle for straight forward movement.
- With the other hand, turn the knurled screwhead knob on the back of the **connector** bulkhead clockwise until the ***connector*** fully engages the receptacle.
- Tighten by turning the knurled screwhead a quarter **turn** with a screwdriver.

f. Connect every dc cable to either J34, J35, J36, J37, J38, J39, J40 or J41 (Figures 4-6 and 4-9). Connect each cable following the procedure given in the preceding step e.

g. Connect the ac control cable (Figure 4-9) from the AC ***power*** distribution panel, to J45, **by** simply pressing it onto the receptacle.

h. Connect the *power* regulator cable (Figure 4-4 and 4-9) from the power distribution board, to J46, by simply pressing it onto the receptacle.

i. Connect the power cable to the 110 Vac switched outlet of the Power Distribution Box.

4.4.9 AC Power Distribution Panel Removal

The AC Power Distribution Panel is shown in Figure 4-23. Refer also to Figure 4-24, where necessary, for an illustration of the power control cable connection to the Interface Assembly chassis.

a. Turn off electrical **power** by setting the OFF/ON/LOCK key operated switch on the processor control panel to OFF.

b. If applicable, open the back door or cover.

c. On the PDP, place the ON/OFF switch in the OFF position.

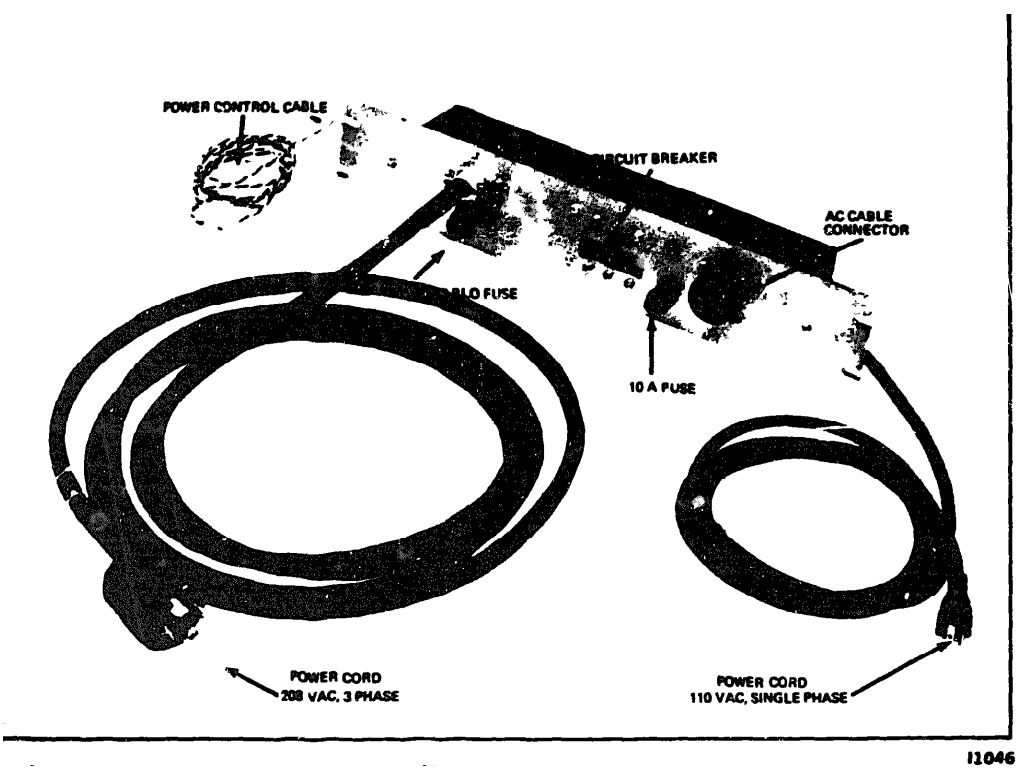

Figure 4-23. AC Power Distributor Panel

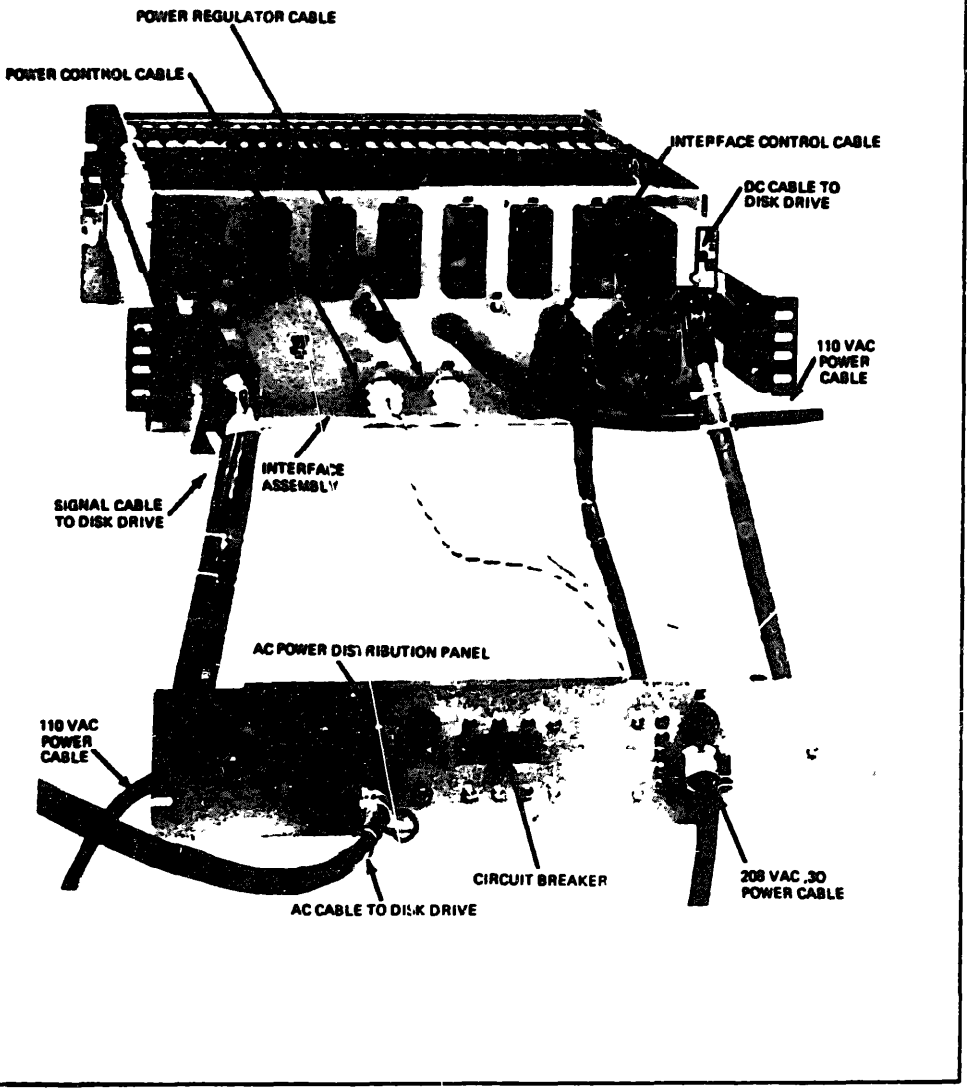

Figure 4-24. Cabling System

d. Unplug the 208 Vac, three phase power cable from outlet receptacle.

e. Unplug the 110 Vac, single phase power cable from Power Distribution Box.

f. Disconnect the *AC* control cable going to the interface assembly, from the J45 connector on the interface assembly (Figure 4-9).

g. Disconnect the AC cable (Figure 4-9) going to the disk drive by holding the connector bulkhead with one hand, gently pulling it outward while rotating the retaining ***ring*** counterclockwise until the cable can be removed.

h. With a Phillips screwdriver, loosen and remove the four Phillips head screws securing the PDP to the frame.

4.4.10 AC Power Distribution Panel Installation

The ***AC power*** distribution panel (PDP) **can** be installed as follows:

a. Turn off electrical power by setting the OFF/ON/LOCK key operated switch on the processor control panel to OFF.

b. If applicable, open the back door or cover.

c. On the PDP, place the ON/OFF switch in the OFF position.

d. Position the PDP in place at the desired height and fasten with four screws.

e. Connect the AC cable **(Figure** 4-7) by inserting the bulkhead connector into the AC receptacle or the PDP, then fastening it by turning the retaining ring clockwise until tight.

f. Connect the AC control cable (Figure 4-9) to the J45 connector on the interface assembly.

g. Plug the 110 Vac power cord into the power outlet on the power distribution box (PDP).

h. Plug the 208 Vac power cord in an appropriate power outlet.

4.5 PACKING AND UNPACKING

The logic boards and cards are shipped in a cardboard container, fully insulated with convoluted foam. To prevent damage to either boards or cards, care must be taken when removing them from the container, or when preparing them for shipment. When shipping, ensure that the insulation (convoluted foam or equivalent) and container are fully protective. A listing of parts and assemblies most likely to be needed for ordering or re-ordering, is given in Table 4-23.

Table 4-23. Useful Part Numbers (Sheet 1 of 2)

Item	Description	Part Number
Disk Pack	Eleven disks, 20 surfaces	350103
Cable assembly	AC, 25 feet	350174
Cable assembly	AC, 6 feet	350175
Cable assembly	DC, 25 feet	350305
Cable assembly	Interface control	103999
Cable assembly	Power Regulator	102651
Cable assembly	Signal, 25 feet	350176
Cable assembly	Signal, 6 feet	350177
Cable assembly	Test	102156
Terminator		350306
Jack Screw	Male, fixed	850108
Jack screw	Male, floating	880150
Jack screw	Female, fixed	850107
Jack screw	Female, floating	880149
Shrink Tubing		770089
Interface Assembly		103982
Line Cord	110 Vac, single phase	850046
Power Supply	5 Vdc, 5A	350045
AC Power Distribution Panel		101335
Line Cord	110 Vac, single phase	850046
Line Cord	208 Vac, three phase	770086
Cable assembly	Power control	850024
Circuit breaker		870027
Power Rectifier	Standard and Extended Chassis	102075
Power Rectifier, Booster	Extended Chassis	103079

Table 4-23. Useful Part Numbers (Sheet 2 of 2)

Item	Description	Part Number
Logic Board	Regulator	101777
Logic Board	Regulator, Booster	103076
Cable Assembly	Power Rectifier to Power Regulator Board	102070
Fuse	1A, Slo blo	860015
Fuse	3A	860004
Fuse	8A	860020
Fuse	10A	860002
Logic board	Programmable Device Controller Type II	104104
Crystal	PDC oscillator	870063
Logic board	Disk Controller Interface	104095
Logic card	Interface logic	103966
Logic card	Multiplex logic	103968
Logic card	Simplex Logic	103970
Logic card	Phase Locked Oscillator	101340
Crystal	PLO oscillator	350036
Logic card	Power Sequencer	103979
Relay	DPDT, 5A - PSQ Card	870025
Switch	SPDT - PSQ card	870047
Clip	Retaining - PSQ card	350146
Transistor	2N3725 - PSQ card, Q1, 2, 3	810002
Diode	PSQ card, CR 6, 7, 8, 9, 11, 12	810006
Diode	PSQ card, CR 1, 2, 3, 4, 5, 10, 13	810010
PC Card	Extender Board	101158

SECTION 5
MAINTENANCE

5.1 GENERAL

This section provides information to aid in both preventive and corrective maintenance. The corrective maintenance information in this section is for the purpose of failure isolation, and correction of equipment malfunction to the extent of replacement of the malfunctioning assemblies.

The controller units covered in this manual are:

- Logic boards.
- Logic cards.
- Interconnecting cables.
- Power Supply.
- Power Distribution Panel
- Interface Assembly

When in this section, reference is made to manuals supplied with the equipment, the other manuals supplied depend on the system configuration. All applicable manuals and system support maintenance drawings are sent with the support documentation.

5.1.1 Service Reports and Usage Logs

Service reports should be kept to establish a case history for each unit. When these records are kept up to date and contain all particulars of each failure or malfunction, time of incidence, and diagnostic and corrective work performed on the unit, they become a useful reference for future repairs.

A usage log to record daily service, service duration and, if applicable, programs run, is also recommended. Such a log provides a record of preventive maintenance periods and establishes a workable MTBF (mean-time-between-failures) indicator. By recording the type and time of the application programs run, patterns of repetitive failures during certain types of programs can be pin-pointed when present.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance involves correct installation, periodic inspections, testing and verification of proper operation and normalcy of operating conditions. Aiding an effective and efficient preventive maintenance program are the aforementioned usage logs and service reports, which provide timely indications of performance trends and failure patterns, should they develop.

The following paragraphs describe procedures for checking and maintaining proper operation and operating conditions.

5.2.1 Periodic Maintenance

Table 5-1 is a preventive maintenance checklist that should be followed at the specified intervals to ensure that equipment operation and operating conditions are, and remain within tolerance range.

5.2.2 Power Supply Voltage Measurement

Power Supply voltage levels can be measured at the test points on the left-hand front edge of the **Regulator board see** Figure 5-1 for test point location and pin designations; refer to Table 5-2 for test parameters. Alternately, voltage levels can be measured at the common power bus, through test openings provided in the upper left-hand ***corner*** of the back panel of the chassis; see Figure 5-2 for test point location and pin designations; refer to Table 5-3 for test parameters.

5.2.3 Logic Voltage Level Measurement

With a calibrated oscilloscope or voltmeter, measure the logic voltage levels as follows:

- Good high logic-level indication is from +2.4 Vdc to +5.0 Vdc. If the high logic level indicates less than +2.4 Vdc, a faulty logic element must be suspected.
- Good low logic-level indication is from 0.0 Vdc to +0.5 Vdc. A low logic level slightly greater than +0.5 Vdc, is normally due to an OR tie. If a low logic level is indicated without the measured signal being OR tied, a faulty logic element must be suspected.

5.3 CORRECTIVE MAINTENANCE

The following paragraphs provide information to aid in trouble-shooting and isolating system failures. Correction of these system failures is by replacement of the malfunctioning unit or assembly.

5.3.1 Failure Isolation

Perform the following preliminary tests and checks in the sequence given:

- Check switches and controls on all units to verify that all settings are correct for the application in which the failure has *occurred.*
- Check all I/O and power connectors to ensure that all connectors are fully seated in or on ***the proper*** receptacles.
- Verify that all units are connected to a proper power source.
- Verify that power is present and of correct magnitude, i.e., all voltage levels are as listed in paragraph 5.2.2.

Table 5-1. Preventive Maintenance Checklist

Task	Interval	Procedure
Perform system level tasks.	As specified.	Refer to GTE/IS manual A0003.
Inspect cables.	4 months.	Look for frayed cables and wires. Check to be sure that no wires are squeezed between structural members. Inspect connectors for damage.
Inspect resistors.	12 months	Discoloration of coding bands or loss of coating indicates abnormal power dissipation; remove resistor and measure resistance.
Clean connectors.	12 months.	Dissolve and wipe away grease deposits with a cotton swab dipped in Freon TF or alcohol. All connectors are gold plated and must not be burnished.
Clean chassis.	Regular overhaul periods.	Wipe the chassis interior and exterior with a cloth moistened with Freon TF or alcohol. Remove dust with a vacuum cleaner.
Measure power supply voltage.	12 months or during troubleshooting periods.	Test points and expected values are given in paragraph 5.2.2.
Execute performance test.	As required.	Execute the performance test given in section 5 after maintenance has been performed or after the controller has been idle for an extended period of time.
Power isolation.	As required.	There should be at least 2 ohms resistance between +5 Vac and GND. There should be at least 1 megohm resistance between +5 Vdc and chassis.
System Reset.	As required.	Ascertain that application of ground to the SRST- signal resets all applicable flip-flops as designated in the logic diagrams (see Appendix A).
Software Tests.		Ascertain that all applicable tests described in Section 5, run successfully.

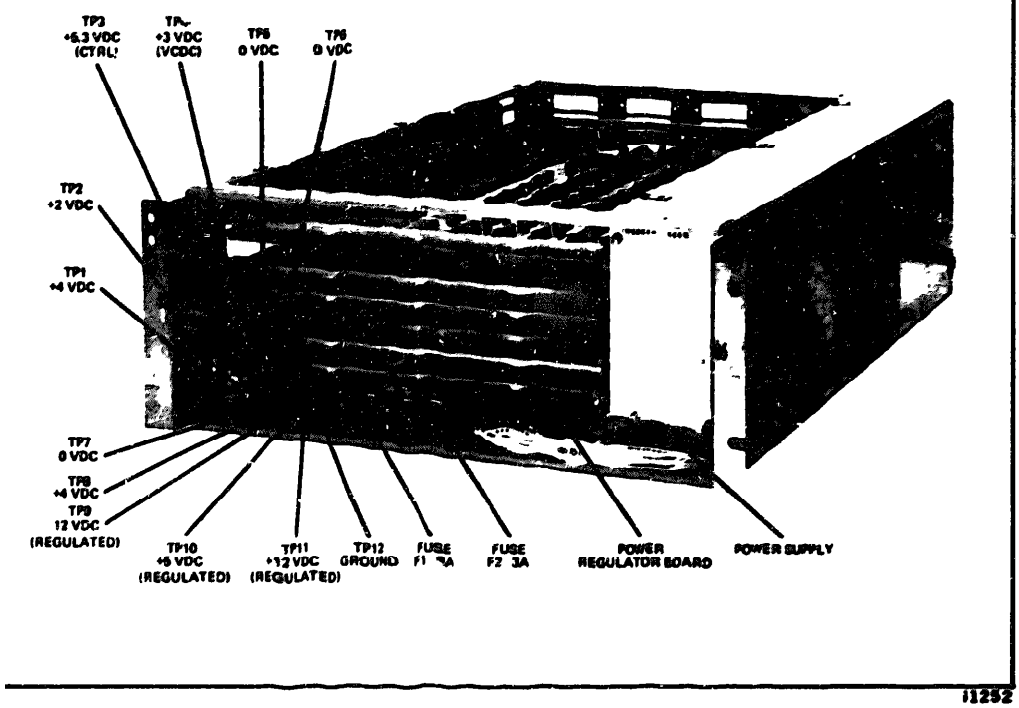

Figure 5-1. Power Regulator Board, Test Points

Table 5-2. Regulator Board Test Points

Test Point	Output	Test Point	Output
1	+4 Vdc	14	+7.5 Vdc
2	+2 Vdc	15	+5.5 Vdc
3	+5.3 Vdc (CTRL)	16	GROUND
4	+3 Vdc (VCDC)	17	GROUND
5	0 Vdc	18	-4.3 Vdc
6	0 Vdc	19	-6.3 Vdc
7	0 Vdc	20	-12 Vdc (raw)
8	+4 Vdc	21	+7 Vdc
9	-12 Vdc (regulated)	22	+5.5 Vdc
10	+5 Vdc (regulated)	23	+4 Vdc
11	+12 Vdc (regulated)	24	GROUND
12	GROUND	25	+5V (raw)
13	+12 Vdc (regulated)		

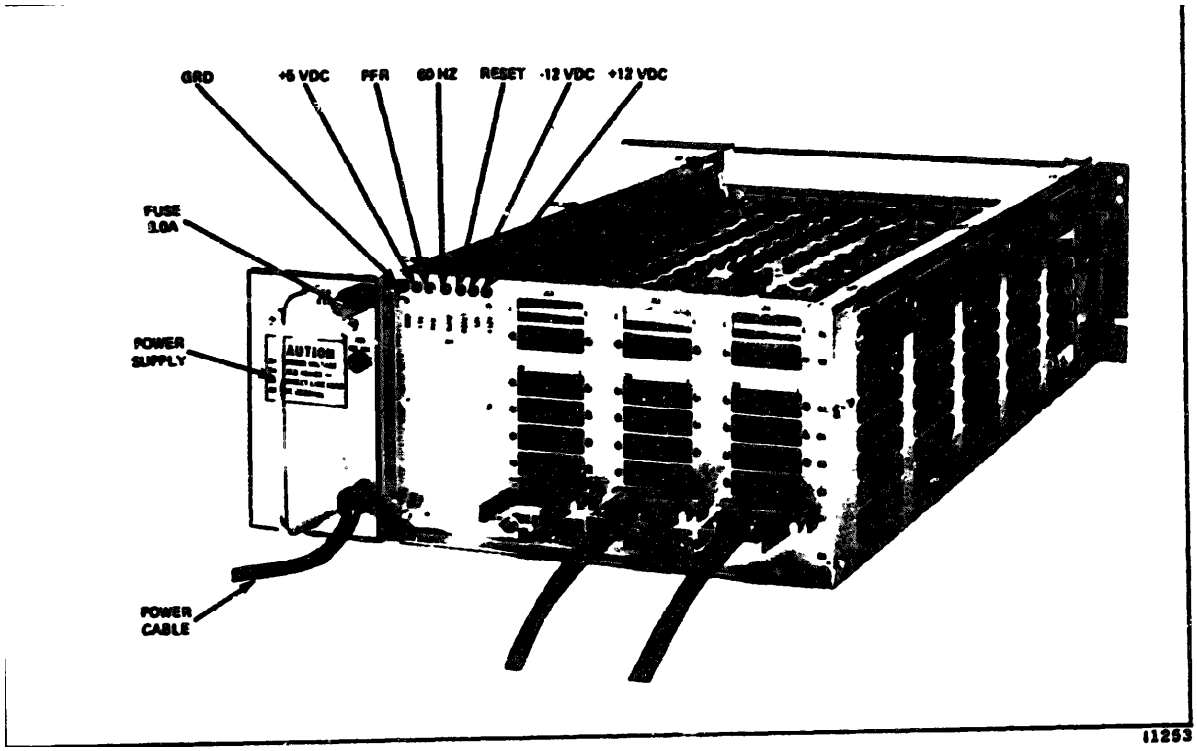

Figure 5-2. Chassis, Test Points

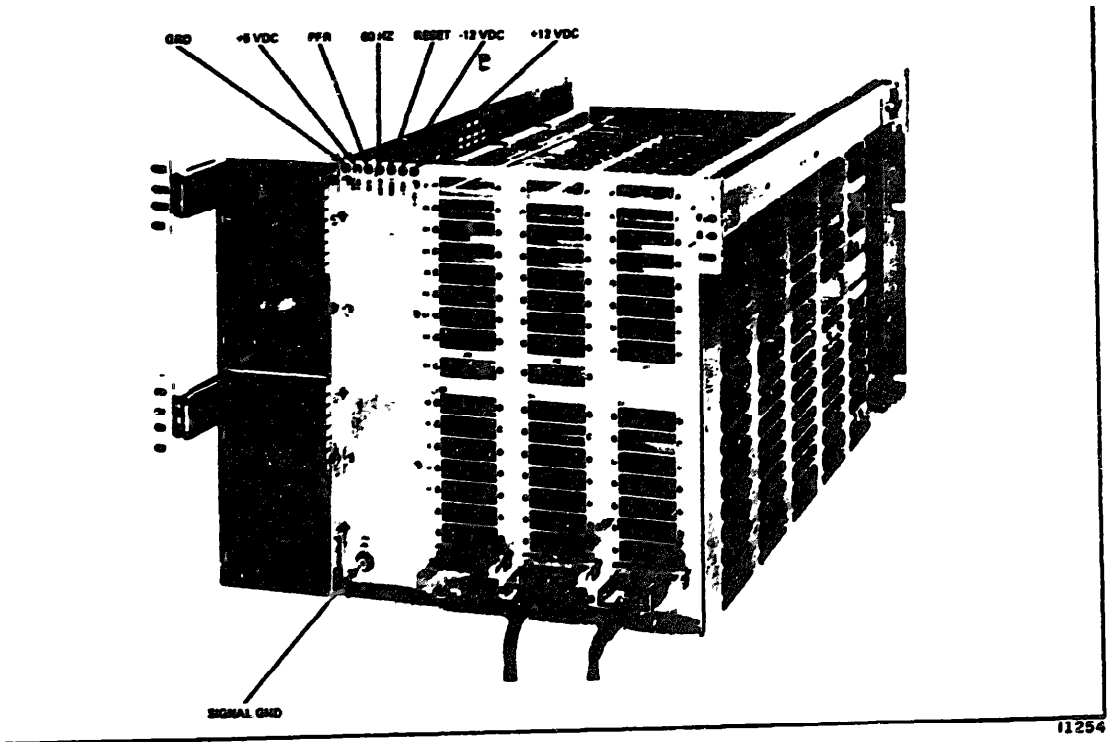

Figure 5-3. Extended Chassis, Test Points

Table 5-3. Chassis Backpanel Test Points

Test Point	Output
+5V	4.5 to 5.5 Vdc
-12V	-11.4 to -12.6 Vdc
+12V	11.4 to 12.6 Vdc
PFR (power failure reset)	5 Vdc (normal)
RESET (master reset)	5 Vdc (normal)
60 Hz (60 Hz clock signal)	60 Hz
GRD	GROUND

5.3.2 Failure Analysis

Three types of failures can occur:

1. Mechanical failures.
2. Electrical failures.
3. Software failures.

5.3.2.1 Mechanical Failures

Broken wires, damaged components, loose connectors, etc., are self-indicative of the required solution. Refer to the appropriate engineering drawings supplied with the equipment, for component identification and wire routing data.

5.3.2.2 Electrical Failures

Incorrect signals from peripheral equipment must be diagnosed and corrected using the manuals supplied with the equipment. Input signals and their source are shown in the logic diagrams and cable connector tables.

5.3.2.3 Software Failures

Failures occurring during the execution of programs, must be analyzed as follows:

- If a test program loads and executes without error indications, the application program(s) are likely to be at fault. Unless the application program has executed properly before, the application program must be suspected of causing the failure. If it is desired to ascertain this with a higher degree of certainty, the failure causing segment of the program may be found through the progressive insertion of branch instructions

around each major section of the program. Once the program section causing the failure has been located, the specific instructions which are in error can be found. However, this debugging technique requires detailed knowledge of the particular program.

If a test program does not load properly or if execution of the test program leads to gross error indications and/or erratic performance, the test should be considered inconclusive. If repeated attempts to load the test program lead to the same results, a larger system malfunction may be indicated.

5.3.3 Failure Correction

Failure correction is accomplished by rectification of the malfunction in the form of adjustment or repair, followed by verification of the effectiveness of that repair.

5.3.3.1 Adjustment and Repair

There are no adjustments on the MDC and repair of the MDC below the assembly level is beyond the scope of this manual. When component-level troubleshooting and replacement are required, the system support maintenance documentation consisting of logic diagrams, flow charts and other engineering drawings that are part of the overall system support package, should be used.

The disk interface card file power supply (Figure 2-6) contains factory set adjustments. Specifications for this power supply appear in Table 5-4. Refer to Appendix C for applicable schematics.

5.3.3.2 Proper Operation Verification

All maintenance activity must be finalized with the running of the appropriate performance test program(s). (Refer to Section 6.) This ensures that all error conditions have been corrected, none accidentally introduced, and that all equipment is operational.

Table 5-4. Disk Interface Power Supply Electrical Requirements

Input Power Specifications

Voltage:	**115 ± 10 Vac @ 47 - 420 Hz**
Current:	**600 Ma max**

Output Power Specifications

Voltage:	**+5.0 ± 0.5 Vdc (adjustable), floating output isolated to 300 V. Factory set at +5.00 ± 0.02 Vdc.**
Voltage Regulation:	**± 0.1% max, line and load**
Ripple:	**1 mv max, RMS**
Overshoot:	**No turn on/off or momentary transient voltage overshoot.**
Response Time:	**50 usec max, no load to full load.**
Overvoltage Protection:	**Adjustable, to limit overvoltage duration to 10 usec, max. Factory set at +6.0 ± 0.2 Vdc.**
Current:	**5.0 amperes dc max, at 50° C.**
Short Circuit Protection:	**Fold back current limiting with instantaneous recovery and automatic reset. 6.0 + 5%, -0%.**
Voltage Sensing:	**Local/remote sensing capability to be provided.**

SECTION 6
PERFORMANCE TESTS

6.1 GENERAL

This section describes the DISC UNIT TEST program, and ***provides*** test ***operating*** procedures as well ***as*** explanations of *error* indications. The performance test should be run after that equipment is installed, before being **placed** in operation after an extended idle period, or **after** any **corrective** maintenance has been **performed.**

6.2 DESCRIPTION

The DISC UNIT TEST **program** provides **a check** on the performance of the magnetic disk subsystem. The program consists of a series **of** test routines, each designed to test specific features of the subsystem. The structure of the DISC UNIT TEST program is illustrated in Figure 6-1.

Functionally, the DISC UNIT TEST program consists **of** the following three test modules:

- Command acceptance and PDC micro program test routine **tests.**
- Magnetic disk subsystem reliability tests.
- Troubleshooting tests.

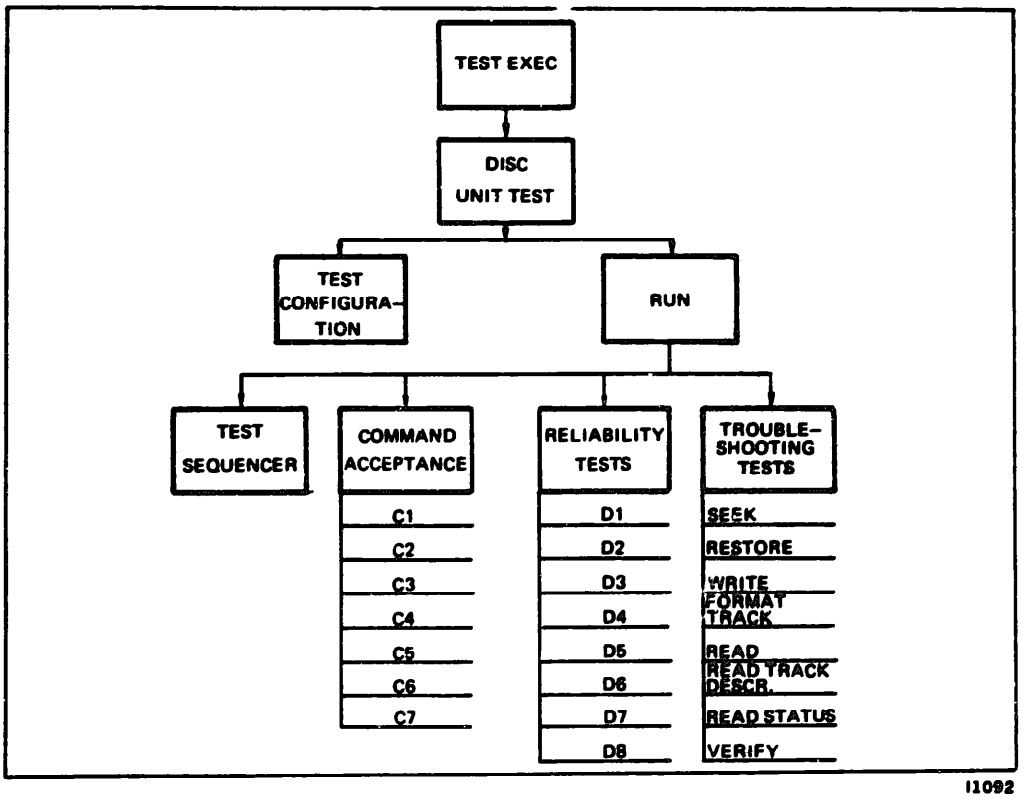

Figure 6-1. DISC UNIT TEST Program Structure

Physically, the DISC UNIT TEST program comprises the following:

- *A* software performance specification.
- A paper tape.
- *A* **program** assembly listing *for* the tape.

The DISC UNIT TEST program is executed by the **processor** under control of the Test Executive program TESTEXC, and consists of the test routines listed in Table 6-1. A minimum of 16K of memory is necessary to execute DISC UNIT TEST. *A* teletype is **required** as the communication link between operator and program. The test bed layout is shown in Figure 6-2.

Table 6-1. DISC UNIT TEST Test Routines (Sheet 1 of 2)

Test Routine	Test Routine Identifier (Directive)	Approximate Execution Time per Pass
Command Acceptance Test 1	C1	
Command Acceptance Test 2	C2	
Command Acceptance Test 3	C3	
Command Acceptance Test 4	C4	
Command Acceptance Test 5	C5	
Command Acceptance Test 6	C6	
Command Acceptance Test 7	C7	
Reliability Test 1	D1	5 minutes 10 seconds
Reliability Test 2	D2	1 minute 47 seconds
Reliability Test 3	D3	1 minute 47 seconds
Reliability Test 4	D4	1 minute 47 seconds
Reliability Test 5	D5	
Reliability Test 6	D6	6 seconds
Reliability Test 7	D7	25 seconds
Reliability Test 8	D8	47 seconds

Table 6-1. DISC UNIT TEST Test Routines (Sheet 2 of 2)

Test Routine	Test Routine Identifier (Directive)	Approximate Execution Time per Pass
Troubleshooting Tests	TS	
Run all Command Acceptance Tests	CA	
Run all Reliability Tests	DR	11 minutes 49 seconds
Run all command Acceptance and all Reliability Tests, except D1	BT	6 minutes 39 seconds
Test sequence of from 1 to 15 tests	SQ	
Run sequenced tests	RS	

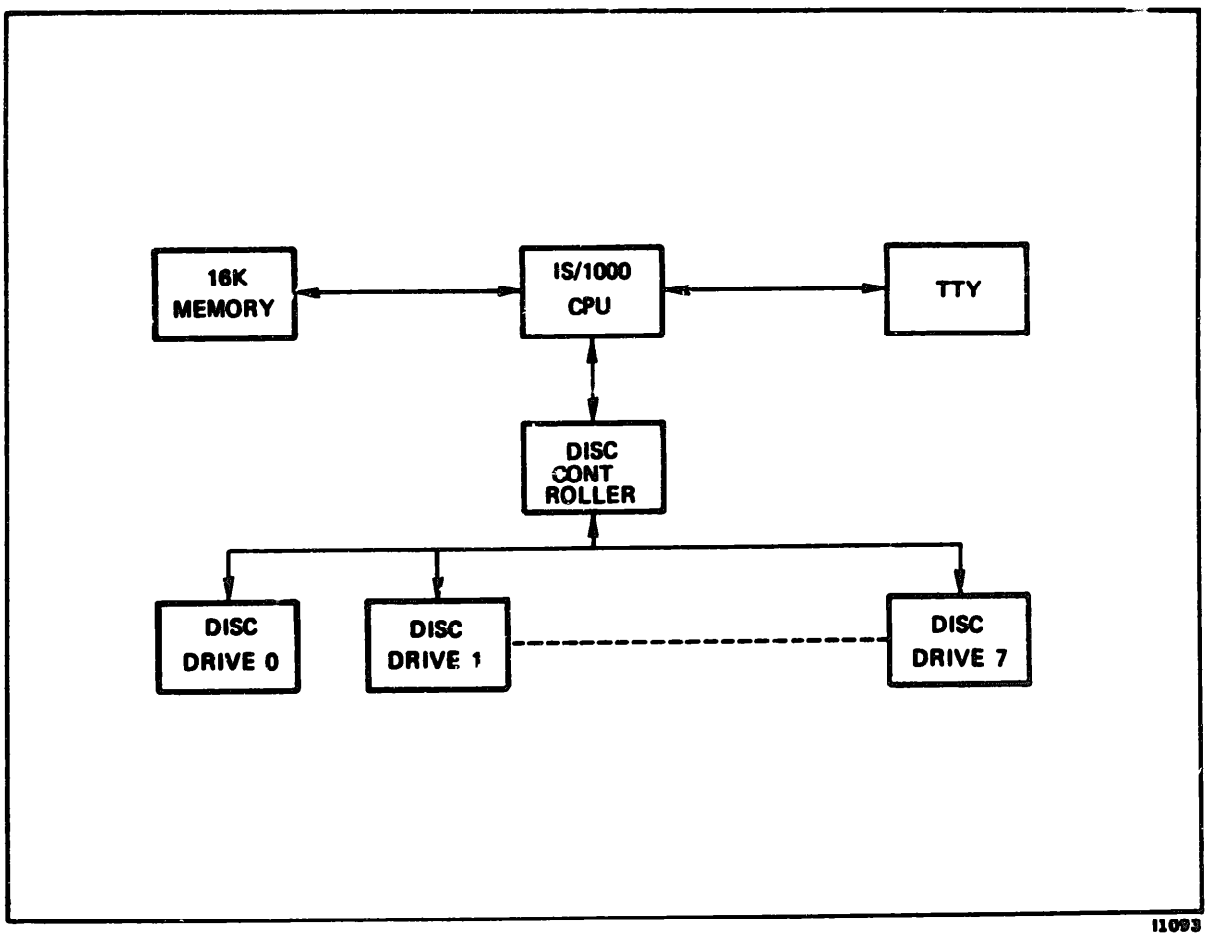

Figure 6-2. DISC UNIT TEST Test Bed Configuration

6.2.1 Command Acceptance Tests (Cn)

The command acceptance and PDC micro program routines test the PDC and the disk controller interface. They also initiate a micro-diagnostic routine in the PDC, which checks various registers and I/O command accessibility to the micro processor.

There are seven acceptance tests which can be executed sequentially or separately. In case of an error condition, with sense switch SS4 set, the program will not proceed with the next test, but loop on the particular test during which the error condition occurred.

The following is a description of the seven command acceptance tests.

6.2.1.1 Command Acceptance Test C1

The C1 test causes the following instructions to be executed:

- **EDF RST**
- **RDS**

The error conditions tested for, are:

- **No EKO for EDF RST.**
- **EKO for RDS.**
- **INTERRUPT for EDF RST.**

6.2.1.2 Command Acceptance Test C2

The C2 test causes the following instructions to be executed:

- **EDF RST**
- **EDF STR (Read Status)**
- **RDS**

The error conditions tested *for, are:*

- EDF STR ENABLE not being set by RST.
- NO INTERRUPT *for EDF STR.*
- INTERRUPT not being set by EDF STR.
- INTERRUPT not being set by RDS.

6.2.1.3 Command Acceptance Test C3

The C3 test causes the following instructions to be executed:

- EDF RST
- EDF STR (Read status)

- ICI
- RST

The ***error*** conditions tested for, are:

- No EKO for ICI.

6.2.1.4 Command Acceptance Test C4

The C4 test causes the following instructions to be executed:

- EDF RST
- EDF STR (Read Status)
- RDS
- ICI

The *error* conditions tested for, are:

- ICI not rejected.
- INTERRUPT reset by RDS.

6.2.1.5 Command Acceptance Test C5

The C5 test causes the following instructions to be executed:

- **EDF** RST
- EDF STR (Read Status)
- RDS
- ICI

The error conditions tested for, are:

- EDF STR not being rejected while the controller is busy.

6.2.1.6 Command Acceptance Test C6

During the C6 test all illegal ***EDF*** instructions are executed. The objective of the test is the rejection of all these instructions by the controller. An *error* condition will be indicated whenever one of these instructions is not rejected.

6.2.1.7 Command Acceptance Test C7

The objective of this test is to check the internal registers and enabling logic of the controller. The *micro* routine resides in the CROM of the microprocessor where it will be started by the EDF STR MEMORY ADDR = 0 instruction from the CPU. Pass and error conditions are sent to the microprocessor by setting the INTERRUPT FLAG and loading the DMA ADDRESS REGISTER with a predetermined code for either a pass condition ***or*** an error condition. See Table 6-4 for error messages.

6.2.2 Disk Subsystem Reliability Tests (Dn)

The reliability test program routines evaluate performance integrity of the system over (relatively) long periods of time.

There are eight reliability tests which are executed consecutively, For individual execution of each test, refer to the trouble-shooting tests.

The following is a description of the eight reliability tests:

6.2.2.1 Disk Subsystem Reliability Test D1

The D1 tests the Format Track operation. The format track routine formats all the disc packs specified by the test configuration. This routine formats a whole pack. Thus, if test limits have been entered for a drive, a message will be printed and D1 will not be executed. The message is: DRIVE N, TEST LIMITS HAVE BEEN ENTERED MUST FORMAT WHOLE PACK. The track flag in the track format table is set to zero. After each track format command the cylinder and head numbers are incremented and the track format table updated. At the completion of the format track routine, the whole pack is verified. At the successful completion of the verification routine, 5 track descriptors are read and compared. (Cylinders 0, 30, 95, 101, 165, 202, and heads 0, 4, 7, 10, 15, 19 respectively). At the successful completion of the track descriptor comparison, the test is completed. Errors are detected by checking the major status when an interrupt occurs. Major status word bits 0, 1, 2, 3 and 12 are monitored. If any of these bits are on, a request status command is issued and the 7 status words are printed. See Section 2 under Status for status words and their meaning. If the track descriptor words do not agree with the expected track descriptor words, all 9 IS and S/B words will be printed. See Section 2 under Track Format, for track descriptor word description. Test D1 completion time is 5 minutes and 10 seconds.

6.2.2.2 Disk Subsystem Reliability Test D2

The D2 tests the Write Command Chaining operation. This routine is designed to work on the whole pack, or within specified limits, in a minimum amount of time. This is accomplished by manipulating the sector address so as to take advantage of the rotational position of the disk pack. Two write commands are chained together with starting sector addresses, three sectors apart. The first write command causes the incrementing ONEs pattern shown in Figure 6-3, to be written. The second write command causes the WORST CASE pattern shown in Figure 6-4, to be written. At the occurrence of the termination interrupt the sector addresses are incremented by nine and the writing continues until the end of the pack or the specified test limit is reached. The length of the data buffer is 230 words, which covers a sector and a half. At the occurrence of each interrupt, the major status word is interrogated on bits 0, 1, 3, and 12. If any of these bits are set, a request status is executed and the 7 status words will be printed. The completion time for test D2 is 1 minute and 47 seconds, if the whole pack is written.

```
0001 0203 0405 0607 0809
0A0B 0C0D 0E0F 1011 1213 1415 1617 1819
1A1B 1C1D 1E1F 2021 2223 2425 2627 2829
2A2B 2C2D 2E2F 3031 3233 3435 3637 3839
3A3B 3C3D 3E3F 4041 4243 4445 4647 4849
4A4B 4C4D 4E4F 5051 5253 5455 5657 5859
5A5B 5C5D 5E5F 6061 6263 6465 6667 6869
6A6B 6C6D 6E6F 7071 7273 7475 7677 7879
7A7B 7C7D 7E7F 8081 8283 8485 8687 8889
8A8B 8C8D 8E8F 9091 9293 9495 9697 9899
9A9B 9C9D 9E9F A0A1 A2A3 A4A5 A6A7 A8A9
AAAB ACAD AEAF B0B1 B2B3 B4B5 B6B7 B8B9
BABB BCBD BEBF C0C1 C2C3 C4C5 C6C7 C8C9
CACB CCCD CECF D0D1 D2D3 D4D5 D6D7 D8D9
DADB DCDD DEDF E0E1 E2E3 E4E5 E6E7 E8E9
EAEB ECED EEEF F0F1 F2F3 F4F5 F6F7 F8F9
FAFB FCFD FEFF 0001 0203 0405 0607 0809
0A0B 0C0D 0E0F 1011 1213 1415 1617 1819
```

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Figure 6-3. Incrementing ONEs Pattern

```
A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
5A5A A5A5 5A5A A5A5 5A5A A5A5 5A5A A5A5
```

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Figure 6-4. **Worst Case Pattern**

6.2.2.3 Disk Subsystem Reliability Test **D3**

The D3 tests the verify operation. The verify routine verifies the entire disk pack. At the occurrence of an interrupt, the major status is interrogated on bits 0, 1, 3 and 12. If any of these bits are set, a request status is executed and the seven status words are printed. Completion time for test D3 is 1 minute and 47 seconds. Once this test has started it cannot be aborted until the terminating interrupt.

6.2.2.4 Disk Subsystem Reliability Test D4

The D4 tests the Chaining operation. This routine should not be executed unless D2 has been executed prior to it, to prevent data ***errors*** from being printed erroneously.

This routine is the same as D2 except that data are *read instead* of written and the write and read buffers are compared. If a data ***error*** is detected, the first word in error plus three succeeding words are printed. Completion time for D4 is 1 minute and **47** seconds.

6.2.2.5 Disk Subsystem Reliability Test D5

The D5 tests the Write/Read Data Chaining operation. This routine is designed to generate rate *errors* during the write and read operations. Nine write commands and nine data buffers are linked together and the commands **are** executed. **At the occurrence** of the interrupt, a request status command is executed and the rate error bit is checked. If it is set, the test continues by executing a write command that places valid data in that track. Nine read commands and nine data buffers are linked together and the commands are executed. At the occurrence of the interrupt, a request status is again executed and the rate **error** bit checked. If the rate error bit is not set, either for write ***or*** read, the message is printed that the rate *error* did not occur and all seven status words are output.

6.2.2.6 Disk Subsystem Reliability Test D6

The D6 tests the Seek Sequential operation. This routine is designed to verify sequential seeks by cylinder number. ***First the*** restore command is executed and a check is made to ensure that two interrupts occurred. Upon the occurrence of the first interrupt the controller busy bit is checked and a wait is initiated for the second interrupt. **At** the occurrence of the second interrupt, the read track descriptor command is executed to reset the gated attention bits. The cylinder number is converted to **binary sector** address and the seek command is executed. Two interrupts are processed for the seek command and the read pack descriptor command is executed. The cylinder ***numbers*** are **compared** to determine that the seek was to the specified cylinder address. If the cylinder numbers ***compare,*** the cylinder number is incremented and another seek command and read track descriptor command are executed until all cylinders have been processed. At the completion of each

seek command, the appropriate gated attention bit is checked for its status. Completion time for D6 is 6 seconds.

6.2.2.7 Disk Subsystem Reliability Test D7

The D7 tests the Seek Increment/Decrement operation. In this routine four commands are linked together. Seek first cylinder, read track descriptor of the first cylinder, seek last cylinder and read track descriptor of last cylinder. The interrupt is only enabled on the last command. Upon the occurrence of the interrupt, the major status is interrogated and the cylinder numbers are compared. If the comparison is satisfactory, the first cylinder number is incremented, the last cylinder number decremented, and the four commands are executed again. This continues until the first cylinder number equals 202, and the last cylinder number equals zero. In case of a status error or seek error, the restore command is executed and error messages will be printed. Completion time for test D7 is 25 seconds.

6.2.2.8 Disk Subsystem Reliability Test D8

The D8 tests the Write/Read Random operation. This routine writes, reads, and compares random data. Random cylinder, head and sector numbers are generated and converted to binary sector address. (See Figure 6-5). The random cylinder number is multiplied by two and used as the random record length to be written and read. The write and the read commands are linked together and they are executed 500 times. At the occurrence of the interrupt, the drive number is changed in the control word and again the commands are executed. In this manner all drives will be exercised simultaneously. This is different from all the other tests where the complete test is run consecutively from one drive to the next. Completion time for the D8 test is 47 seconds.

6.2.3 Troubleshooting Tests (TS)

The troubleshooting test routines enables the operator to configure his own test procedures, criteria and parameters. There are eight troubleshooting tests as follows:

- Seek
- Restore
- Write
- Format Track
- Read
- Read Track Descriptor
- Read Status
- Verify

A total of eight commands can be entered and executed sequentially. Each time the program outputs CMD, the operator enters a command,

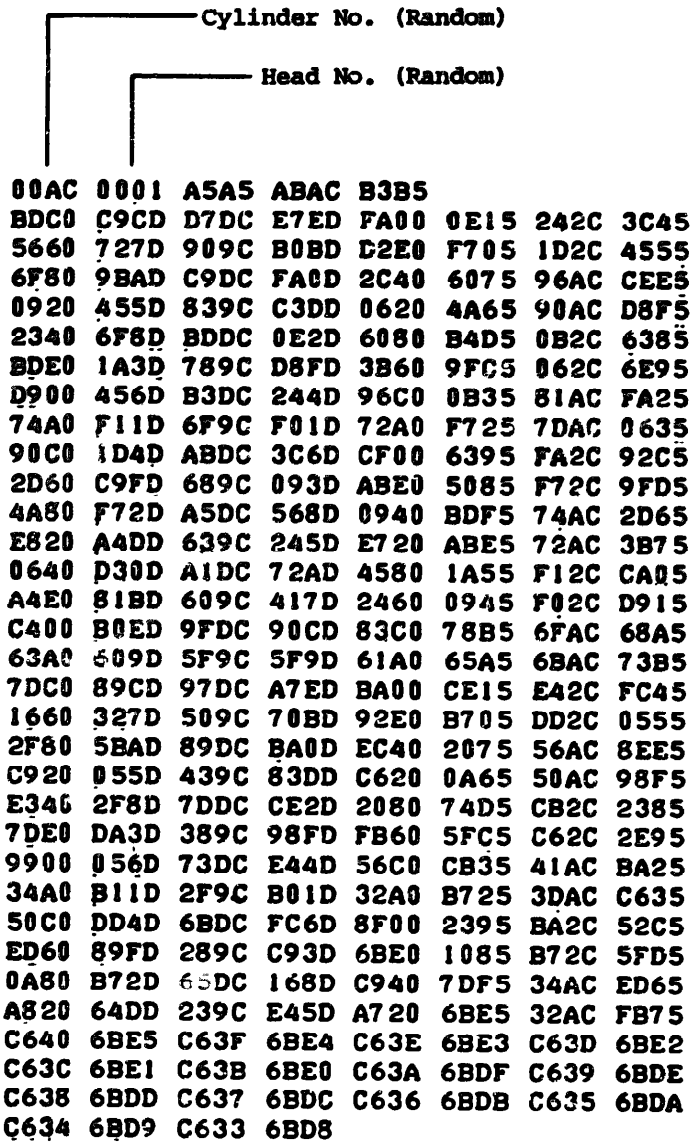

Figure 6-5. Random Data Pattern

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as described under the Operating Procedures. Each command requires, and will request, information *for* the five program control words.

Care must be taken in entering the responses; for example the last command entered in a string must have the interrupt enabled and it cannot be linked. All linking is done forward. Thus, if the last command entered is linked it will be linked to something unknown and anything can happen. Initially the time delay for the troubleshooting tests is set for 32 seconds. If this value is changed and the execution of a command or commands takes longer than the time delay entered, the program will output NO INTERRUPT. This message in this case will not signify an equipment error but instead it is the result of an *operator* (output) error.

If the major status word indicates some problems in the disk subsystem, the read statue is executed and 7 status words are output. As a result of the CB (compare data), directive, if data do not compare, four data words IS and S/B are output starting at *the first* error. As a result of the RT (read track descriptor) command, if the track **descriptor** words do not agree, the IS track descriptor words are printed. When ***a seek*** command is *entered and is* linked *to another* command whose interrupt is enabled, in cases an unexpected interrupt may be output. This is due to the fact that the terminate interrupt is disabled and the controller starts processing the command which is linked to the seek command and at this point the interrupts are enabled. Thus two interrupts can occur - the terminate interrupt of the second command and the gated attention interrupt of the seek command, which in this case will be an unexpected interrupt.

6.3 PREREQUISITES

The following equipment is required to perform the **DISK** UNIT TEST:

- GTE/IS Model IS/1000 Processor with 16k memory.
- Model ASR 33 Teletype, **or** equivalent.

When the DISC UNIT TEST is used for troubleshooting purposes, an oscilloscope, Tektronics Model 7403N or equivalent, is recommended.

6.4 TEST SETUP

See Figure 6-2 for the test setup required to test the magnetic disk subsystem.

6.5 OPERATING PROCEDURES

The following outlines the general procedure for performing the DISC UNIT TEST:

- Load the TESEXC tape. Refer to engineering drawing 380689, which is shipped with the equipment, for complete instructions regarding the use of all features of TESEXC.

When the TESEXC program has been loaded, the teletype prints out

```
EXECUTIVE READY
←
```

The keyboard is now enabled for input.

- Place the DISC UNIT TEST program tape in the reader station of the teletype. The DISC UNIT TEST program can now be loaded by typing L(CR). If the system has a version 2 (V2) CPU with a 4-segment ROM, execute a B (branch) 55 instead.
- After the DISC UNIT TEST has been loaded, the teletype will output the following:

```
DISC UNIT TEST PROGRAM


SPS 382747  LI 382749  BA 382751
REV X1 -  · OCT 74

DISC UNIT TEST ROUTINES AND ID'S
  BT  RUN ALL CA AND DR TESTS
  CA  RUN ALL CA TESTS
  C1  EDF RST AND RDS
  C2  EDF RST, EDF STR(READ STATUS), RDS
  C3  EDF RST, EDF STR(READ STATUS), ICI  RST
  C4  EDF RST, EDF STR(READ STATUS), RDS  ICI
  C5  EDF RST, EDF STR, EDF STR, RDS
  C6  ILLEGAL EDF'S
  C7  R/P MICRO ROUTINE
  DR  ALL RELIABILITY TESTS
  D1  FORMAT TRACK
  D2  WRITE COMMAND CHAINING
  D3  VERIFY WHOLE PACK
  D4  READ COMMAND CHAINING
  D5  WRITE/READ DATA CHAINING
  D6  SEEK SEQUENTIAL
  D7  SEEK INCREMENT/DECREMENT
  D8  WRITE/READ RANDOM
  TS  TROUBLESHOOTING TESTS
  SQ  TEST SEQUENCER
  RS  RUN SEQUENCED TESTS
```

This printout will only occur after an initial program load procedure; it will not be printed out after a restart operation. When the print out is not desired, placing sense switch 8 in the up (on) position, will prevent it from being output. Sense switch 8 must be turned off after completion of the load operation.

- At the processor control panel, set the Sense switches as required, by referring to Table 6-2.
- A series of messages is then output requesting control parameters for the execution of the DISC UNIT TEST test routines. By entering the appropriate control parameters in response to each message, the operator determines which routines are to be executed and how they are executed. As the program outputs a message, the operator simply enters the desired parameter followed by a CR. The format, meaning and required responses for this initial test configuring procedure are listed in Table 6-3.

Once all the required system configuration parameters have been initially entered, the Disc Unit Test Program will continue to use these parameters until the system is reloaded or control is transferred to location zero.

a. The first message is:

DISC UNIT TEST PROGRAM

No response to this message is required.

Table 6-2. Sense Switch Settings

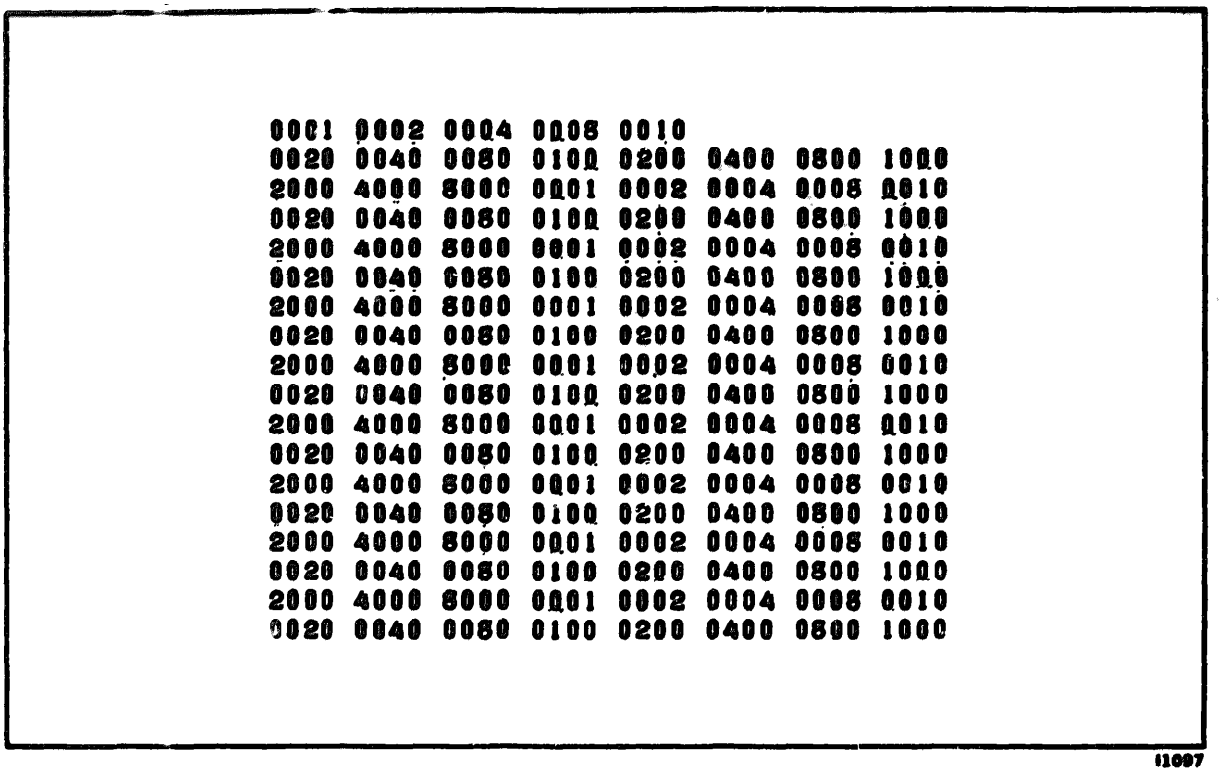
Sense Switch	Position of Switch	
	Up	Down
SSW1	Halt when an error is encountered. Pertinent information is displayed in the registers.	Continue.
SSW3	Suppress all error messages.	Output error messages.
SSW4	Repeat the module under test.	Continue.
SSW8	Abort the test module currently being executed and return control to the Test Executive.	Continue.

Table 6-3. DISC UNIT TEST Control Parameters (Sheet 1 of 2)

Control Message	Description	Required Response
CMD	The buffer area for the troubleshooting commands will be cleared.	CL
	The commands entered will be executed.	RU
	The program will return to the RUN statement.	RN
	Compare the contents of the write buffer against the contents of the read buffer.	CB
	Read	RD
	Write	WR
	Format Track	FM
	Read track description	RT
	Verify	VR
	Seek	SK
	Read Status	RS
	Restore	RR
DRIVE=	Drive number C-7	N
TIMEOUT	The time delay is set at 32 seconds. If no input is made the time delay will stay at 32 sec. The range is from 0-32,767. The time delay is in 1 ms increments.	NNNN
LINK	The command will be linked to the next command entered if Y is input. The interrupt will be disabled for this command. If n is input the command will not be linked.	Y or N
DISABL INT	If Y is entered the interrupt will be disabled for this command. If N is entered the interrupt will not be disabled.	Y or N
DATA CHAIN	If Y is entered the data buffers are linked. If n is entered there will be no buffer linking. This is for write/read operations only.	Y or N

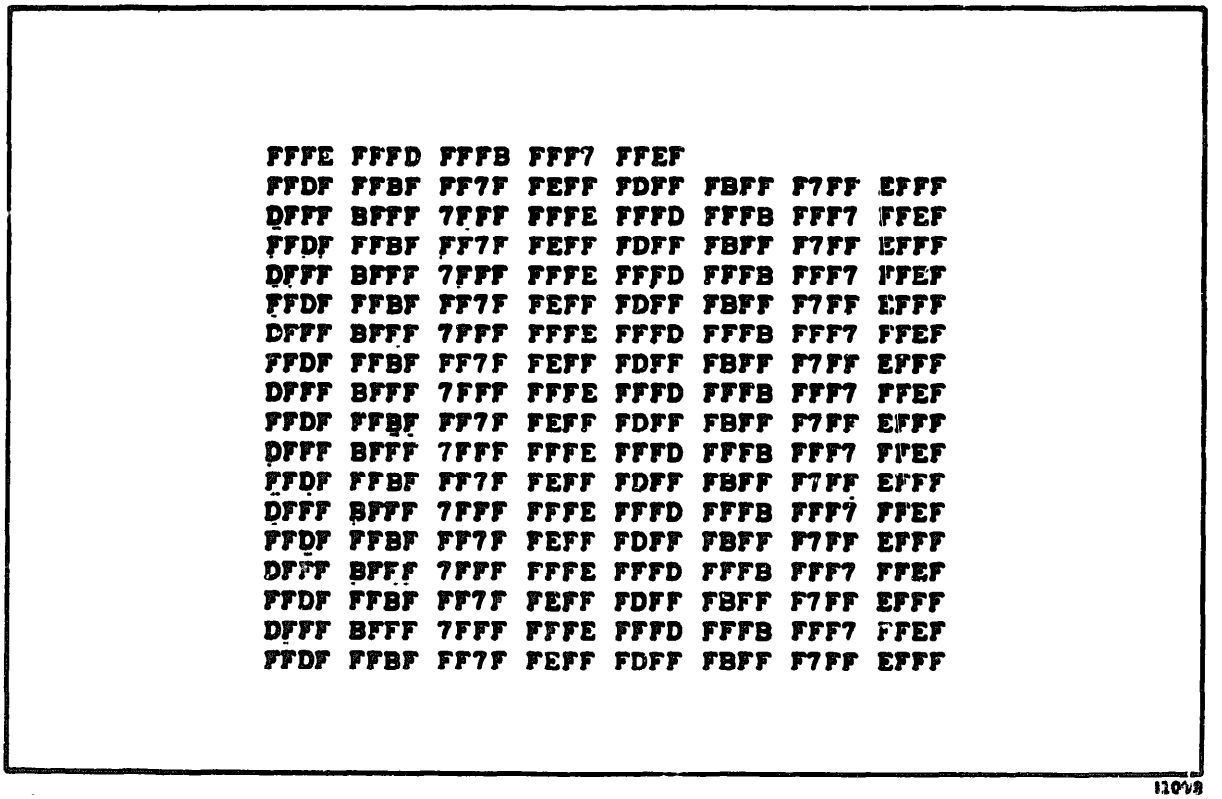
Table 6-3. DISC UNIT TEST Control Parameter (Sheet 2 of 2)

Control Message	Description	Required Response
TRACK FLAG	0 - Good primary track 1 - Good alternate track 2 - Defective primary track 3 - Defective alternate track	0-3
SEC. ADDR	Sector address 0-64,959$_{10}$ maximum address in hex is FDBF. From 0-32,767$_{10}$ the sector address can be entered in decimal. Sector address greater than 32,767$_{10}$ must be entered in hexadecimal. Refer to Table 6-5 for sector address listing.	NNNNN
WORD COUNT	The word count range is from 1-1000$_{10}$. It can be entered in decimal or hexadecimal.	NNNN
DATA PATT.	I - Incrementing ONEs pattern (Figure 6-3). O - Sliding ONEs pattern (Figure 6-6). Z - Sliding ZEROs pattern (Figure 6-7). W - Worst cass pattern (Figure 6-4). P - Operator chooses pattern N - Do previous pattern	A
PATTERN	Enter data pattern desired.	NNNN
CYLINDER NO.	The cylinder number ranges from 0-202. It can be entered in decimal or hexa-decimal. Refer to Table 6-5 for Cylinder and Sector address listing.	NNN
HEAD NO.	The head number ranges from 0-19. It can be entered in decimal or hexadecimal. Refer to Table 6-5.	NN
SECT COUNT	Sector count range is from 0-64,959$_{10}$. Refer to Table 6-5 for Sector count.	NNNNN
PRINT STATUS	If Y is entered the seven status words are printed. If N is entered the status will not be printed.	Y or N
BUFFER FULL	This message will be printed if more than 8 commands have been entered.	



```
0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
2000 4000 8000 0001 0002 0004 0008 0010
0020 0040 0080 0100 0200 0400 0800 1000
```

Figure 6-6. Sliding ONEs Pattern



```
FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
DFFF BFFF 7FFF FFFE FFFD FFFB FFF7 FFEF
FFDF FFBF FF7F FEFF FDFF FBFF F7FF EFFF
```

Figure 6-7. Sliding ZEROs Pattern

b. The next message is:

DEV. ADDR=

In response to this request, the operator must input a decimal (0-63) or hexadecimal ($0-$3F) value defining the device address.

c. The next message is:

INT LINE=

In response to this request the operator must input a decimal (8-15) or hexadecimal ($8-$F) value defining the interrupt line used by the Disc Subsystem.

d. The next message is:

ICI BIT ASSIGN=

If the interrupt is on a common interrupt line, the user must respond by inputting a decimal or hexadecimal value defining the common interrupt status bit position (Data Input Bus) assigned to the device. Otherwise, enter the letter N indicating no common interrupt assignment.

e. The next message is:

NO. OF DRIVES=

In response to this request, the user must enter the number of drives present in the system to be tested (1-8).

f. The next message is:

DRIVE=

The user must enter the drive numbers for the drives to be tested. One number per request.

g. The next message is:

TEST LIM Y N

If the user enters N, the program will go to RUN and the whole pack is operated on.

If the user enters Y the following is printed: DRIVE N FCN=, FHN=, LCN=, LHN=, This will be printed for all the drives entered previously:

FCN=First Cylinder number. The decimal input is 0-202.

FHN=First head number. The decimal input is 0-19.

LCN=Last cylinder number. (Same range as FCN).

LHN=Last head number. (Same range as FHN).

Refer to Table 6-5, for head and cylinder **numbers,** and the sectors contained within the segment selected by the first and last head and cylinder numbers.

6.5.1 Test Selection

Whenever the Disc Unit Test Program has completed system configuration or control is passed to location two (2), the keyboard is enabled **for** input of the "RUN" statement as follows:

RUN ID, PASS (C/R) - Execute ID, pass number of times

RUN ID (C/R) - **Execute** until manually halted

RUN GO (C/R) - Use previous ID and *PASS*

ID - This is a two character name that identifies the **test** to be executed.

PASS - This is an optional decimal value in the range of 0 to 32,767 which specifies the number of times to execute the selected test.

Refer to Table 6-1 for test identifiers.

6.5.2 Troubleshooting Routine (TS)

The troubleshooting routines are provided to assist the operator in troubleshooting the Disk Subsystem. The routine will **request** various items to build the operation stack and the associated queues. Table 6-3 depicts the **requests, responses** and the description.

6.5.3 Test Sequence Routine (SQ)

This routine allows the user to select up to 15 tests and sequence them in any order he desires.

6.5.4 Input Rejection

Input rejects are indicated by a single question mark (?).

6.6 ERROR INDICATIONS

When the test program detects an error, an ***error message may be*** output or ***the*** test may be stopped by an error halt if these functions are enabled. Error indications and their probable causes are listed in Table 6-4. Error halts are identified by I-Register contents. The operator can resume operations after an error halt condition, by pressing the RUN switch. The R2 register contains the test ID.

Table 6-4. DISC UNIT TEST Error Indications (Sheet 1 of 2).

I-Register Contents	Test Module	Error Message and Probable Cause
01	ANY	ID EDF RST REJECT AT
02	ANY	ID EDF RDS REJECT AT
03	ANY	ID EDF STR REJECT AT
04	C3	C3 ICI REJECT AT
05	C1	C1 NO RDS REJECT AT
06	C3,C4	ID NO ICI REJECT AT
07	C5	C5 NO EDF STR REJECT AT
08	C6	C6 NO EDF INI REJECT AT
09	C6	C6 NO EDF INV REJECT AT
10	C6	C6 NO WTO REJECT AT
11	C6	C6 NO WTI REJECT AT
12	ANY	ID NO INTERRUPT
13	C3	C3 DESIGNATED ICI BIT MISSING
14	TS	TS NO INTERRUPT
15	ANY	ID UNEXPECTED INTERRUPT
*16	C7	C7 CONTROLLER FAILURE 0080 (DMA ADDR FAILURE) 00C0 (FIFO OVERFLOW) 00E0 (FIFO DATA PATTERN ALL ONES) 00F0 (CRC UPPER FAILURE) 00F8 (FIFO DATA PATTERN ALL ZEROS) 00FC (CRC LOWER FAILURE)
17	D1	D1 DRIVE=N IS S/B TRACK DESCRIPTOR WORDS XXXX XXXX (9 TRACK DESCRIPTOR WORDS WILL BE PRINTED).

*On a halt without printout Register 8 will contain the error code. In the case of C7, if no interrupt is printed out, check the FIFO.

Table 6-4. DISC UNIT TEST Error Indications (Sheet 2 of 2)

I-Register Contents	Test Module	Error Message and Probable Cause
18	DR	ID BAD STATUS DRIVE=N XXXX (7 STATUS WORDS WILL BE PRINTED).
19	D4,D8	ID DATA ERROR DRIVE=N IS S/B SEC.ADR ED.NO XXXX XXXX XXXX XXXX XXXX XXXX
20	D5	NO RATE EPROR FOR WRITE DRIVE=N D5 BAD STATUS XXXX (7 STATUS WORDS WILL BE PRINTED)
21	D5	NO RATE ERROR FOR READ DRIVE=N D5 BAD STATUS XXXX (7 STATUS WORDS WILL BE PRINTED)
22	D6,D7	DRIVE=N
23	D6	ID NO SECOND INT FOR RESTORE DRIVE=N
24	D6	D6 GATED ATTENTION NOT OFF DRIVE=N
25	D6	D6 NO SECOND INT FOR SEEK DRIVE=N
26	D6	D6 GATED ATTENTION NOT ON D6 DRIVE=N IS S/B CYLINDER NO. XXXX XXXX
27	D7	D7 DRIVE=N IS S/B CYLINDER NO. XXXX XXXX XXXX XXXX
28		CHECKSUM ERROR IS S/B XXXX XXXX

Table 6-5a. Sector Addresses, Cylinders 0-F

Cylinder																	
Decimal:		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal:		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Track (Head) Dec.	Hex.																
0	0	0000	0140	0280	03C0	0500	0640	0780	08C0	0A00	0B40	0C80	0DC0	0F00	1040	1180	12C0
1	1	0010	0150	0290	03D0	0510	0650	0790	08D0	0A10	0B50	0C90	0DD0	0F10	1050	1190	12D0
2	2	0020	0160	02A0	03E0	0520	0660	07A0	08E0	0A20	0B60	0CA0	0DE0	0F20	1060	11A0	12E0
3	3	0030	0170	02B0	03F0	0530	0670	07B0	08F0	0A30	0B70	0CB0	0DF0	0F30	1070	11B0	12F0
4	4	0040	0180	02C0	0400	0540	0680	07C0	0900	0A40	0B80	0CC0	0E00	0F40	1080	11C0	1300
5	5	0050	0190	02D0	0410	0550	0690	07D0	0910	0A50	0B90	0CD0	0E10	0F50	1090	11D0	1310
6	6	0060	01A0	02E0	0420	0560	06A0	07E0	0920	0A60	0BA0	0CE0	0E20	0F60	10A0	11E0	1320
7	7	0070	01B0	02F0	0430	0570	06B0	07F0	0930	0A70	0BB0	0CF0	0E30	0F70	10B0	11F0	1330
8	8	0080	01C0	0300	0440	0580	06C0	0800	0940	0A80	0BC0	0D00	0E40	0F80	10C0	1200	1340
9	9	0090	01D0	0310	0450	0590	06D0	0810	0950	0A90	0BD0	0D10	0E50	0F90	10D0	1210	1350
10	A	00A0	01E0	0320	0460	05A0	06E0	0820	0960	0AA0	0BE0	0D20	0E60	0FA0	10E0	1220	1360
11	B	00B0	01F0	0330	0470	05B0	06F0	0830	0970	0AB0	0BF0	0D30	0E70	0FB0	10F0	1230	1370
12	C	00C0	0200	0340	0480	05C0	0700	0840	0980	0AC0	0C00	0D40	0E80	0FC0	1100	1240	1380
13	D	00D0	0210	0350	0490	05D0	0710	0850	0990	0AD0	0C10	0D50	0E90	0FD0	1110	1250	1390
14	E	00E0	0220	0360	04A0	05E0	0720	0860	09A0	0AE0	0C20	0D60	0EA0	0FE0	1120	1260	13A0
15	F	00F0	0230	0370	04B0	05F0	0730	0870	09B0	0AF0	0C30	0D70	0EB0	0FF0	1130	1270	13B0
16	10	0100	0240	0380	04C0	0600	0740	0880	09C0	0B00	0C40	0D80	0EC0	1000	1140	1280	13C0
17	11	0110	0250	0390	04D0	0610	0750	0890	09D0	0B10	0C50	0D90	0ED0	1010	1150	1290	13D0
18	12	0120	0260	03A0	04E0	0620	0760	08A0	09E0	0B20	0C60	0DA0	0EE0	1020	1160	12A0	13E0
19	13	0130	0270	03B0	04F0	0630	0770	08B0	09F0	0B30	0C70	0DB0	0EF0	1030	1170	12B0	13F0

Table 6-5b. Sector Addresses, Cylinders 10-1F

Cylinder																	
Decimal:		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Hexadecimal:		10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Track (Head) Dec.	Hex.																
0	0	1400	1540	1680	17C0	1900	1A40	1B80	1CC0	1E00	1F40	2080	21C0	2300	2440	2580	26C0
1	1	1410	1550	1690	17D0	1910	1A50	1B90	1CD0	1E10	1F50	2090	21D0	2310	2450	2590	26D0
2	2	1420	1560	16A0	17E0	1920	1A60	1BA0	1CE0	1E20	1F60	20A0	21E0	2320	2460	25A0	26E0
3	3	1430	1570	16B0	17F0	1930	1A70	1BB0	1CF0	1E30	1F70	20B0	21F0	2330	2470	25B0	26F0
4	4	1440	1580	16C0	1800	1940	1A80	1BC0	1D00	1E40	1F80	20C0	2200	2340	2480	25C0	2700
5	5	1450	1590	16D0	1810	1950	1A90	1BD0	1D10	1E50	1F90	20D0	2210	2350	2490	25D0	2710
6	6	1460	15A0	16E0	1820	1960	1AA0	1BE0	1D20	1E60	1FA0	20E0	2220	2360	24A0	25E0	2720
7	7	1470	15B0	16F0	1830	1970	1AB0	1BF0	1D30	1E70	1FB0	20F0	2230	2370	24B0	25F0	2730
8	8	1480	15C0	1700	1840	1980	1AC0	1C00	1D40	1E80	1FC0	2100	2240	2380	24C0	2600	2740
9	9	1490	15D0	1710	1850	1990	1AD0	1C10	1D50	1E90	1FD0	2110	2250	2390	24D0	2610	2750
10	A	14A0	15E0	1720	1860	19A0	1AE0	1C20	1D60	1EA0	1FE0	2120	2260	23A0	24E0	2620	2760
11	B	14B0	15F0	1730	1870	19B0	1AF0	1C30	1D70	1EB0	1FF0	2130	2270	23B0	24F0	2630	2770
12	C	14C0	1600	1740	1880	19C0	1B00	1C40	1D80	1EC0	2000	2140	2280	23C0	2500	2640	2780
13	D	14D0	1610	1750	1890	19D0	1B10	1C50	1D90	1ED0	2010	2150	2290	23D0	2510	2650	2790
14	E	14E0	1620	1760	18A0	19E0	1B20	1C60	1DA0	1EE0	2020	2160	22A0	23E0	2520	2660	27A0
15	F	14F0	1630	1770	18B0	19F0	1B30	1C70	1DB0	1EF0	2030	2170	22B0	23F0	2530	2670	27B0
16	10	1500	1640	1780	18C0	1A00	1B40	1C80	1DC0	1F00	2040	2180	22C0	2400	2540	2680	27C0
17	11	1510	1650	1790	18D0	1A10	1B50	1C90	1DD0	1F10	2050	2190	22D0	2410	2550	2690	27D0
18	12	1520	1660	17A0	18E0	1A20	1B60	1CA0	1DE0	1F20	2060	21A0	22E0	2420	2560	26A0	27E0
19	13	1530	1670	17B0	18F0	1A30	1B70	1CB0	1DF0	1F30	2070	21B0	22F0	2430	2570	26B0	27F0

Table 6-5c. Sector Addresses, Cylinders 20-2F

Cylinder																	
Decimal:		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
Hexadecimal:		20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
Track (Head)																	
Dec.	Hex.																
0	0	2800	2940	2A80	2BC0	2D00	2E40	2F80	30C0	3200	3340	3480	35C0	3700	3840	3980	3AC0
1	1	2810	2950	2A90	2BD0	2D10	2E50	2F90	30D0	3210	3350	3490	35D0	3710	3850	3990	3AD0
2	2	2820	2960	2AA0	2BE0	2D20	2E60	2FA0	30E0	3220	3360	34A0	35E0	3720	3860	39A0	3AE0
3	3	2830	2970	2AB0	2BF0	2D30	2E70	2FB0	30F0	3230	3370	34B0	35F0	3730	3870	39B0	3AF0
4	4	2840	2980	2AC0	2C00	2D40	2E80	2FC0	3100	3240	3380	34C0	3600	3740	3880	39C0	3B00
5	5	2850	2990	2AD0	2C10	2D50	2E90	2FD0	3110	3250	3390	34D0	3610	3750	3890	39D0	3B10
6	6	2860	29A0	2AE0	2C20	2D60	2EA0	2FE0	3120	3260	33A0	34E0	3620	3760	38A0	39E0	3B20
7	7	2870	29B0	2AF0	2C30	2D70	2EB0	2FF0	3130	3270	33B0	34F0	3630	3770	38B0	39F0	3B30
8	8	2880	29C0	2B00	2C40	2D80	2EC0	3000	3140	3280	33C0	3500	3640	3780	38C0	3A00	3B40
9	9	2890	29D0	2B10	2C50	2D90	2ED0	3010	3150	3290	33D0	3510	3650	3790	38D0	3A10	3B50
10	A	28A0	29E0	2B20	2C60	2DA0	2EE0	3020	3160	32A0	33E0	3520	3660	37A0	38E0	3A20	3B60
11	B	28B0	29F0	2B30	2C70	2DB0	2EF0	3030	3170	32B0	33F0	3530	3670	37B0	38F0	3A30	3B70
12	C	28C0	2A00	2B40	2C80	2DC0	2F00	3040	3180	32C0	3400	3540	3680	37C0	3900	3A40	3B80
13	D	28D0	2A10	2B50	2C90	2DD0	2F10	3050	3190	32D0	3410	3550	3690	37E0	3920	3A50	3B90
14	E	28E0	2A20	2B60	2CA0	2DE0	2F20	3060	31A0	32E0	3420	3560	36A0	37E0	3920	3A60	3BA0
15	F	28F0	2A30	2B70	2CB0	2DF0	2F30	3070	31B0	32F0	3430	3570	36B0	37F0	3930	3A70	3BB0
16	10	2900	2A40	2B80	2CC0	2E00	2F40	3080	31C0	3300	3440	3580	36C0	3800	3940	3A80	3BC0
17	11	2910	2A50	2B90	2CD0	2E10	2F50	3090	31D0	3310	3450	3590	36D0	3810	3950	3A90	3BD0
18	12	2920	2960	2BA0	2CD0	2E20	2F60	30A0	31E0	3320	3460	35A0	36E0	3820	3960	3AA0	3BE0
19	13	2930	2970	2BB0	2CF0	2E30	2F70	30B0	31F0	3330	3470	35B0	36F0	3830	3970	3AB0	3BF0

Table 6-5d. Sector Addresses, *Cylinders* 30-3F

Cylinder																	
Decimal:		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Hexadecimal:		30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
Track (Head)																	
Dec.	Hex.																
0	0	3C00	3D40	3E80	3FC0	4100	4240	4380	44C0	4600	4740	4880	49C0	4B00	4C40	4D80	4EC0
1	1	3C10	3D50	3E90	3FD0	4110	4250	4390	44D0	4610	4750	4890	49D0	4B10	4C50	4D90	4ED0
2	2	3C20	3D60	3EA0	3FE0	4120	4260	43A0	44E0	4620	4760	48A0	49E0	4B20	4C60	4DA0	4EE0
3	3	3C30	3D70	3EB0	3FF0	4130	4270	43B0	44F0	4630	4770	48B0	49F0	4B30	4C70	4DB0	4EF0
4	4	3C40	3D80	3EC0	4000	4140	4280	43C0	4500	4640	4780	48C0	4A00	4B40	4C80	4DC0	4F00
5	5	3C50	3D90	3ED0	4010	4150	4290	43D0	4510	4650	4790	48D0	4A10	4B50	4C90	4DD0	4F10
6	6	3C60	3DA0	3EE0	4020	4160	42A0	43E0	4520	4660	47A0	48E0	4A20	4B60	4CA0	4DE0	4F20
7	7	3C70	3DB0	3EF0	4030	4170	42B0	43F0	4530	4670	47B0	48F0	4A30	4B70	4CB0	4DF0	4F30
8	8	3C80	3DC0	3F00	4040	4180	42C0	4400	4540	4680	47C0	4900	4A40	4B80	4CC0	4E00	4F40
9	9	3C90	3DD0	3F10	4050	4190	42D0	4410	4550	4690	47D0	4910	4A50	4B90	4CD0	4E10	4F50
10	A	3CA0	3DE0	3F20	4060	41A0	42E0	4420	4560	46A0	47E0	4920	4A60	4BA0	4CE0	4E20	4F60
11	B	3CB0	3DF0	3F30	4070	41B0	42F0	4430	4570	46B0	47F0	4930	4A70	4BB0	4CF0	4E30	4F70
12	C	3CC0	3E00	3F40	4080	41C0	4300	4440	4580	46C0	4800	4940	4A80	4BC0	4D00	4E40	4F80
13	D	3CD0	3D10	3F50	4090	41D0	4310	4450	4590	46D0	4810	4950	4A90	4BD0	4D10	4E50	4F90
14	E	3CE0	3E20	3F60	40A0	41E0	4320	4460	45A0	46E0	4820	4960	4AA0	4BE0	4D20	4E60	4FA0
15	F	3CF0	3E30	3F70	40B0	41F0	4330	4470	45B0	46F0	4830	4970	4AB0	4BF0	4D30	4E70	4FB0
16	10	3D00	3E40	3F80	40C0	4200	4340	4480	45C0	4700	4840	4980	4AC0	4C00	4D40	4E80	4FC0
17	11	3D10	3E50	3F90	40D0	4210	4350	4490	45D0	4710	4850	4990	4AD0	4C10	4D50	4E90	4FD0
18	12	3D20	3E60	3FA0	40E0	4220	4360	44A0	45E0	4720	4860	49A0	4AE0	4C20	4D60	4EA0	4FE0
19	13	3D30	3E70	3FB0	40F0	4230	4370	44B0	45F0	4730	4870	49B0	4AF0	4C30	4D70	4EB0	4FF0

Table 6-5e. Sector Addresses, Cylinders 40-4F

	Cylinder															
Decimal:	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
Hexadecimal:	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
Track (Head) Dec.	Hex.															
0	0	5000	5140	5280	53C0	5500	5640	5780	58C0	5A00	5B40	5C80	5DC0	5F00	6040	6180	62C0
1	1	5010	5150	5290	53D0	5510	5650	5790	58D0	5A10	5B50	5C90	5DD0	5F10	6050	6190	62D0
2	2	5020	5160	52A0	53E0	5520	5660	57A0	58E0	5A20	5B60	5CA0	5DE0	5F20	6060	61A0	62E0
3	3	5030	5170	52B0	53F0	5530	5570	57B0	58F0	5A30	5B70	5CB0	5DF0	5F30	6070	61B0	62F0
4	4	5040	5180	52C0	5400	5540	5680	57C0	5900	5A40	5B80	5CC0	5E00	5F40	6080	61C0	6300
5	5	5050	5190	52D0	5410	5550	5690	57D0	5910	5A50	5B90	5CD0	5E10	5F50	6090	61D0	6310
6	6	5060	51A0	52E0	5420	5560	56A0	57E0	5920	5A60	5BA0	5CE0	5E20	5F60	60A0	61E0	6320
7	7	5070	51B0	52F0	5430	5570	56B0	57F0	5930	5A70	5BB0	5CF0	5E30	5F70	60B0	61F0	6330
8	8	5080	51C0	5300	5440	5580	56C0	5800	5940	5A80	5BC0	5D00	5E40	5F80	60C0	6200	6340
9	9	5090	51D0	5310	5450	5590	56D0	5810	5950	5A90	5BD0	5D10	5E50	5F90	60D0	6210	6350
10	A	50A0	51E0	5320	5460	55A0	56E0	5820	5960	5AA0	5BE0	5D20	5E60	5FA0	60E0	6220	6360
11	B	50B0	51F0	5330	5470	55B0	56F0	5830	5970	5AB0	5BF0	5D30	5E70	5FB0	60F0	6230	6370
12	C	50C0	5200	5340	5480	55C0	5700	5840	5980	5AC0	5C00	5D40	5E80	5FC0	6100	6240	6380
13	D	50D0	5210	5350	5490	55D0	5710	5850	5990	5AD0	5C10	5D50	5E90	5FD0	6110	6250	6390
14	E	50E0	5220	5360	54A0	55E0	5720	5860	59A0	5AE0	5C20	5D60	5EA0	5FE0	6120	6260	63A0
15	F	50F0	5230	5370	54B0	55F0	5730	5870	59B0	5AF0	5C30	5D70	5EB0	5FF0	6130	6270	63B0
16	10	5100	5240	5380	54C0	5600	5740	5880	59C0	5B00	5C40	5D80	5EC0	6000	6140	6280	63C0
17	11	5110	5250	5390	54D0	5610	5750	5890	59D0	5B10	5C50	5D90	5ED0	6010	6150	6290	63D0
18	12	5120	5260	53A0	54E0	5620	5760	58A0	59E0	5B20	5C60	5DA0	5EE0	6020	6160	62A0	63E0
19	13	5130	5270	53B0	54F0	5630	5770	58B0	59F0	5B30	5C70	5DB0	5EF0	6030	6170	62B0	63F0

Table **6-5f. Sector Addresses, Cylinders 50-5F**

	Cylinder															
Decimal:	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
Hexadecimal:	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
Track (Head) Dec.	Hex.															
0	0	6400	6540	6680	67C0	6900	6A40	6B80	6CC0	6E00	6F40	7080	71C0	7300	7440	7580	76C0
1	1	6410	6550	6690	67D0	6910	6A50	6B90	6CD0	6E10	6F50	7090	71D0	7310	7450	7590	76D0
2	2	6420	6560	66A0	67E0	6920	6A60	6BA0	6CE0	6E20	6F60	70A0	71E0	7320	7460	65A0	76E0
3	3	6430	6570	66B0	67F0	6930	6A70	6BB0	6CF0	6E30	6F70	70B0	71F0	7330	7470	75B0	76F0
4	4	6440	6580	66C0	6800	6940	6A80	6BC0	6D00	6E40	6F80	70C0	7200	7340	7480	75C0	7700
5	5	6450	6590	66D0	6810	6950	6A90	6BD0	6D10	6E50	6F90	70D0	7210	7350	7490	75D0	7710
6	6	6460	65A0	66E0	6820	6960	6AA0	6BE0	6D20	6E60	6FA0	70E0	7220	7360	74A0	75E0	7720
7	7	6470	65B0	66F0	6830	6970	6AB0	6BF0	6D30	6E70	6FB0	70F0	7230	7370	74B0	75F0	7730
8	8	6480	65C0	6700	6840	6980	6AC0	6C00	6D40	6E80	6FC0	7100	7240	7380	74C0	7600	7740
9	9	6490	65D0	6710	6850	6990	6AD0	6C10	6D50	6E90	6FD0	7110	7250	7390	74D0	7610	7750
10	A	64A0	65E0	6720	6860	69A0	6AE0	6C20	6D60	6EA0	6FE0	7120	7260	73A0	74E0	7620	7760
11	B	64B0	65F0	6730	6870	69B0	6AF0	6C30	6D70	6EB0	6FF0	7130	7270	73B0	74F0	7630	7770
12	C	64C0	6600	6740	6880	69C0	6B00	6C40	6D80	6EC0	7000	7140	7280	73C0	7500	7640	7780
13	D	64D0	6610	6750	6890	69D0	6B10	6C50	6D90	6ED0	7010	7150	7290	73D0	7510	7650	7790
14	E	64E0	6620	6760	68A0	69E0	6B20	6C60	6DA0	6EE0	7020	7160	72A0	73E0	7520	7660	77A0
15	F	64F0	6630	6770	68B0	69F0	6B30	6C70	6DB0	6EF0	7030	7170	72B0	73F0	7530	7670	77B0
16	10	6500	6640	6780	68C0	6A00	6B40	6C80	6DC0	6F00	7040	7180	72C0	7400	7540	7680	77C0
17	11	6510	6650	6790	68D0	6A10	6B50	6C90	6DD0	6F10	7050	7190	72D0	7410	7550	7690	77D0
18	12	6520	6660	67A0	68E0	6A20	6B60	6CA0	6DE0	6F20	7060	71A0	72E0	7420	7560	76A0	77E0
19	13	6530	6670	67B0	68F0	6A30	6B70	6CB0	6DF0	6F30	7070	71B0	72F0	7430	7570	76B0	77F0

Table 6-5g. Sector Addresses, Cylinders 60-6F

Cylinder																	
Decimal:		96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
Hexadecimal:		60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
Track (Head) Dec.	Hex.																
0	0	7800	7940	7A80	7BC0	7D00	7E40	7F80	80C0	8200	8340	8480	85C0	8700	8840	8980	8AC0
1	1	7810	7950	7A90	7BD0	7D10	7E50	7F90	80D0	8210	8350	8490	85D0	8710	8850	8990	8AD0
2	2	7820	7960	7AA0	7BE0	7D20	7E60	7FA0	80E0	8220	8360	84A0	85E0	8720	8860	89A0	8AE0
3	3	7830	7970	7AB0	7BF0	7D30	7E70	7FB0	80F0	8230	8370	84B0	85F0	8730	8870	89B0	8AF0
4	4	7840	7980	7AC0	7C00	7D40	7E80	7FC0	8100	8240	8380	84C0	8600	8740	8880	89C0	8B00
5	5	7850	7990	7AD0	7C10	7D50	7E90	7FD0	8110	8250	8390	84D0	8610	8750	8890	89D0	8B10
6	6	7860	79A0	7AE0	7C20	7D60	7EA0	7FE0	8120	8260	83A0	84E0	8620	8760	88A0	89E0	8B20
7	7	7870	79B0	7AF0	7C30	7D70	7EB0	7FF0	8130	8270	83B0	84F0	8630	8770	88B0	89F0	8B30
8	8	7880	79C0	7B00	7C40	7D80	7EC0	8000	8140	8280	83C0	8500	8640	8780	88C0	8A00	8B40
9	9	7890	79D0	7B10	7C50	7D90	7ED0	8010	8150	8290	83D0	8510	8650	8790	88D0	8A10	8B50
10	A	78A0	79E0	7B20	7C60	7DA0	7EE0	8020	8160	82A0	83E0	8520	8660	87A0	88E0	8A20	8B60
11	B	78B0	79F0	7B30	7C70	7DB0	7EF0	8030	8170	82B0	83F0	8530	8670	87B0	88F0	8A30	8B70
12	C	78C0	7A00	7B40	7C80	7DC0	7F00	8040	8140	82C0	8400	8540	8680	87C0	8900	8A40	8B80
13	D	78D0	7A10	7B50	7C90	7DD0	7F10	8050	8190	82D0	8410	8550	8690	87D0	8910	8A50	8B90
14	E	78E0	7A20	7B60	7CA0	7DE0	7F20	8060	81A0	82E0	8420	8560	86A0	87E0	8920	8A60	8BA0
15	F	78F0	7A30	7B70	7CB0	7DF0	7F30	8070	81B0	82F0	8430	8570	86B0	87F0	8930	8A70	8BB0
16	10	7900	7A40	7B80	7CC0	7E00	7F40	8080	81C0	8300	8440	8580	86C0	8800	8940	8A80	8BC0
17	11	7910	7A50	7B90	7CD0	7E10	7F50	8090	81D0	8310	8450	8590	86D0	8800	8950	8A90	8BD0
18	12	7920	7A60	7BA0	7CD0	7E20	7F60	80A0	81E0	8320	8460	85A0	86E0	8820	8960	8AA0	8BE0
19	13	7930	7A70	7BB0	7CF0	7E30	7F70	80B0	81F0	8330	8470	85B0	86F0	8830	8970	8AB0	8BF0

Table 6-5h. Sector Addresses, Cylinders 70-7F

Cylinder																	
Decimal:		112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
Hexadecimal:		70	71	72	73	74	75	75	77	78	79	7A	7B	7C	7D	7E	7F
Track (Head) Dec.	Hex.																
0	0	8C00	8D40	8E80	8FC0	9100	9240	9380	94C0	9600	9740	9880	99C0	9B00	9C40	9D80	9EC0
1	1	8C10	8D50	8E90	8FD0	9110	9250	9390	94D0	9610	9750	9890	99D0	9B10	9C50	9D90	9ED0
2	2	8C20	8D60	8EA0	8FE0	9120	9260	93A0	94E0	9620	9760	98A0	99E0	9B20	9C60	9DA0	9EE0
3	3	8C30	8D70	8EB0	8FF0	9130	9270	93B0	94F0	9630	9770	98B0	99F0	9B30	9C70	9DB0	9EF0
4	4	8C40	8D80	8EC0	9000	9140	9280	93C0	9500	9640	9780	98C0	9A00	9B40	9C80	9DC0	9F00
5	5	8C50	8D90	8ED0	9010	9150	9290	93D0	9510	9650	9790	98D0	9A10	9B50	9C90	9DD0	9F10
6	6	8C60	8DA0	8EE0	9020	9160	92A0	93E0	9520	9660	97A0	98E0	9A20	9B60	9CA0	9DE0	9F20
7	7	8C70	8DB0	8EF0	9030	9170	92B0	93F0	9530	9670	97B0	98F0	9A30	9B70	9CB0	9DF0	9F30
8	8	8C80	8DC0	8F00	9040	9180	92C0	9400	9540	9680	97C0	9900	9A40	9B80	9CC0	9E00	9F40
9	9	8C90	8DD0	8F10	9050	9190	92D0	9410	9550	9690	97D0	9910	9A50	9B90	9CD0	9E10	9F50
10	A	8CA0	8DE0	8F20	9060	91A0	92E0	9420	9560	96A0	97E0	9920	9A60	9BA0	9CE0	9E20	9F60
11	B	8CB0	8DF0	8F30	9070	91B0	92F0	9430	9570	96B0	97F0	9930	9A70	9BB0	9CF0	9E30	9F70
12	C	8CC9	8E00	8F40	9080	91C0	9300	9440	9580	96C0	9800	9940	9A80	9BC0	9D00	9D40	9F80
13	D	8CD0	8E10	8F50	9090	91D0	9310	9450	9590	96D0	9810	9950	9A90	9BD0	9D10	9E50	9F90
14	E	8CE0	8E20	8F60	90A0	91E0	9320	9460	95A0	96E0	9820	9960	9AA0	9BE0	9D20	9E60	9FA0
15	F	8CF0	8E30	8F70	90B0	91F0	9330	9470	95B0	96F0	9830	9970	9AB0	9BF0	9D30	9E70	9FB0
16	10	8D00	8E40	8F80	90C0	9200	9340	9480	95C0	9700	9840	9980	9AC0	9C00	9D40	9E80	9FC0
17	11	8D10	8E50	8F90	90D0	9210	9350	9490	95D0	9710	9850	9990	9AD0	9C10	9D50	9E90	9FD0
18	12	8D20	8E60	8FA0	90E0	9220	9360	94A0	95E0	9720	9860	99A0	9AE0	9C20	9D60	9EA0	9FE0
19	13	8D30	8E70	8FB0	90F0	9230	9370	94B0	95F0	9730	9870	99B0	9AF0	9C30	9D70	9EB0	9FF0

Table 6-5i. Sector Addresses, Cylinders 80-8F

Cylinder																	
Decimal:		128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
Hexadecimal:		80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Track (Head)																	
Dec.	Hex.																
0	0	A000	A140	A280	A3C0	A500	A640	A780	A8C0	AA00	AB40	AC80	ADC0	AF00	B040	B180	B2C0
1	1	A010	A150	A290	A3D0	A510	A650	A790	A8D0	AA10	AB50	AC90	ADD0	AF10	B050	B190	B2D0
2	2	A020	A160	A2A0	A3E0	A520	A660	A7A0	A8E0	AA20	AB60	ACA0	ADE0	AF20	B060	B1A0	B2E0
3	3	A030	A170	A2B0	A3F0	A530	A670	A7B0	A8F0	AA30	AB70	ACB0	ADF0	AF30	B070	B1B0	B2F0
4	4	A040	A180	A2C0	A400	A540	A680	A7C0	A900	AA40	AB80	ACC0	AE00	AF40	B080	B1C0	B300
5	5	A050	A190	A2D0	A410	A550	A690	A7D0	A910	AA50	AB90	ACD0	AE10	AF50	B090	B1D0	B310
6	6	A060	A1A0	A2E0	A420	A560	A6A0	A7E0	A920	AA60	ABA0	ACE0	AE20	AF60	B0A0	B1E0	B320
7	7	A070	A1B0	A2F0	A430	A570	A6B0	A7F0	A930	AA70	ABB0	ACF0	AE30	AF70	B0B0	B1F0	B330
8	8	A080	A1C0	A300	A440	A580	A6C0	A800	A940	AA80	ABC0	AD00	AE40	AF80	B0C0	B200	B340
9	9	A090	A1D0	A310	A450	A590	A6D0	A810	A950	AA90	ABD0	AD10	AE50	AF90	B0D0	B210	B350
10	A	A0A0	A1E0	A320	A460	A5A0	A6E0	A820	A960	AAA0	ABE0	AD20	AE60	AFA0	B0E0	B220	B360
11	B	A0B0	A1F0	A330	A470	A5B0	A6F0	A830	A970	AAB0	ABF0	AD30	AE70	AFB0	B0F0	B230	B370
12	C	A0C0	A200	A340	A480	A5C0	A700	A840	A980	AAC0	AC00	AD40	AE80	AFC0	B100	B240	B380
13	D	A0D0	A210	A350	A490	A5D0	A710	A850	A990	AAD0	AC10	AD50	AE90	AFD0	B110	B250	B390
14	E	A0E0	A220	A360	A4A0	A5E0	A720	A860	A9A0	AAE0	AC20	AD60	AEA0	AFE0	B120	B260	B3A0
15	F	A0F0	A230	A370	A4B0	A5F0	A730	A870	A9B0	AAF0	AC30	AD70	AEB0	AFF0	B130	B270	B3B0
16	10	A100	A240	A380	A4C0	A600	A740	A880	A9C0	AB00	AC40	AD80	AEC0	B000	B140	B280	B3C0
17	11	A110	A250	A390	A4D0	A610	A750	A890	A9D0	AB10	AC50	AD90	AED0	B010	B150	B290	B3D0
18	12	A120	A260	A3A0	A4E0	A620	A760	A8A0	A9E0	AB20	AC60	ADA0	AEE0	B020	B160	B2A0	B3E0
19	13	A130	A270	A3B0	A4F0	A630	A770	A8B0	A9F0	AB30	AC70	ADB0	AEF0	B030	B170	B2B0	B3F0

Table 6-5j. Sector Addresses, Cylinders 90-9F

Cylinder																	
Decimal:		144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
Hexadecimal:		90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
Track (Head)																	
Dec.	Hex.																
0	0	B400	B540	B680	B7C0	B900	BA40	BB80	BCC0	BE00	BF40	C080	C1C0	C300	C440	C580	C6C0
1	1	B410	B550	B690	B7D0	B910	BA50	BB90	BCD0	BE10	BF50	C090	C1D0	C310	C450	C590	C6D0
2	2	B420	B560	B6A0	B7E0	B920	BA60	BBA0	BCE0	BE20	BF60	C0A0	C1E0	C320	C460	C5A0	C6E0
3	3	B430	B570	B6B0	B7F0	B930	BA70	BBB0	BCF0	BE30	BF70	C0B0	C1F0	C330	C470	C5B0	C6F0
4	4	B440	B580	B6C0	B800	B940	BA80	BBC0	BD00	BE40	BF80	C0C0	C200	C340	C480	C5C0	C700
5	5	B450	B590	B6D0	B810	B950	BA90	BBD0	BD10	BE50	BF90	C0D0	C210	C350	C490	C5D0	C710
6	6	B460	B5A0	B6E0	B820	B960	BAA0	BBE0	BD20	BE60	BFA0	C0E0	C220	C360	C4A0	C5E0	C720
7	7	B470	B5B0	B6F0	B830	B970	BAB0	BBF0	BD30	BE70	BFB0	C0F0	C230	C370	C4B0	C5F0	C730
8	8	B480	B5C0	B700	B840	B980	BAC0	BC00	BD40	BE80	BFC0	C100	C240	C380	C4C0	C600	C740
9	9	B490	B5D0	B710	B850	B990	BAD0	BC10	BD50	BE90	BFD0	C110	C250	C390	C4D0	C610	C750
10	A	B4A0	B5E0	B720	B860	B9A0	BAE0	BC20	BD60	BEA0	BFE0	C120	C260	C3A0	C4E0	C620	C760
11	B	B4B0	B5F0	B730	B870	B9B0	BAF0	BC30	BD70	BEB0	BFF0	C130	C270	C3B0	C4F0	C630	C770
12	C	B4C0	B600	B740	B880	B9C0	BB00	BC40	BD80	BEC0	C000	C140	C280	C3C0	C500	C640	C780
13	D	B4D0	B610	B750	B890	B9D0	BB10	BC50	BD90	BED0	C010	C150	C290	C3D0	C510	C650	C790
14	E	B4E0	B620	B760	B8A0	B9E0	BB20	BC60	BDA0	BEE0	C020	C160	C2A0	C3E0	C520	C660	C7A0
15	F	B4F0	B630	B770	B8B0	B9F0	BB30	BC70	BDB0	BEF0	C030	C170	C2B0	C3F0	C530	C670	C7B0
16	10	B500	B640	B780	B8C0	BA00	BB40	BC80	BDC0	BF00	C040	C180	C2C0	C400	C540	C680	C7C0
17	11	B510	B650	B790	B8D0	BA10	BB50	BC90	BDD0	BF10	C050	C190	C2D0	C410	C550	C690	C7D0
18	12	B520	B660	B7A0	B8E0	BA20	BB60	BCA0	BDE0	BF20	C060	C1A0	C2E0	C420	C560	C6A0	C7E0
19	13	B530	B670	B7B0	B8F0	BA30	BB70	BCB0	BDF0	BF30	C070	C1B0	C2F0	C430	C570	C6B0	C7F0

Table 6-5k. Sector Addresses, Cylinders A0-AF

Cylinder																	
Decimal:		160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
Hexadecimal:		A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF
Track (Head)																	
Dec.	Hex.																
0	0	C800	C940	CA80	CBC0	CD00	CE40	CF80	D0C0	D200	D340	D480	D5C0	D700	D840	D980	DAC0
1	1	C810	C950	CA9C	CBD0	CD10	CE50	CF90	D0D0	D210	D350	D490	D5D0	D710	D850	D990	DAD0
2	2	C820	C960	CAA0	CBE0	CD20	CE60	CFA0	D0E0	D220	D370	D4A0	D5E0	D720	D860	D9A0	DAE0
3	3	C830	C970	CAB0	CBF0	CD30	CE70	CFB0	D0F0	D230	D370	D4B0	D5F0	D730	D870	D9B0	DAF0
4	4	C840	C980	CAC0	CC00	CD40	CE80	CFC0	D100	D240	D380	D4C0	D600	D740	D880	D9C0	DB00
5	5	C850	C990	CAD0	CC10	CD50	CE90	CFD0	D110	D250	D390	D4D0	D610	D750	D890	D9D0	DB10
6	6	C860	C9A0	CAE0	CC20	CD60	CEA0	CFE0	D120	D260	D3A0	D4E0	D620	D760	D8A0	D9E0	DB20
7	7	C870	C9B0	CAF0	CC30	CD70	CEB0	CFF0	D130	D270	D3B0	D4F0	D630	D770	D8B0	D9F0	DB30
8	8	C880	C9C0	CB00	CC40	CD80	CEC0	D000	D140	D280	D3C0	D500	D640	D780	D8C0	DA00	DB40
9	9	C890	C9D0	CB10	CC50	CD90	CED0	C010	D150	D290	D3D0	D510	D650	D790	D8D0	DA10	DB50
10	A	C8A0	C9E0	CB20	CC60	CDA0	CEE0	D020	D160	D2A0	D3E0	D520	D660	D7A0	D8E0	DA20	DB60
11	B	C8B0	C9F0	CB30	CC70	CDB0	CEF0	D030	D170	D2B0	D3F0	D530	D670	D7B0	D8F0	DA30	DB70
12	C	C8C0	CA00	CB40	CC80	CDC0	CF00	D040	D180	D2C0	D400	D540	D680	D7C0	D900	DA40	DB80
13	D	C8D0	CA10	CB50	CC90	CDD0	CF10	D050	D190	D2D0	D410	D550	D690	D7D0	D910	DA50	DB90
14	E	C8E0	CA20	CB60	CCA0	CDE0	CF20	D060	D1A0	D2E0	D420	D560	D6A0	D7E0	D920	DA60	DBA0
15	F	C8F0	CA30	CB70	CCB0	CDF0	CF30	D070	D1B0	D2F0	D430	D570	D6B0	D7F0	D930	DA70	DBB0
16	10	C900	CA40	CB80	CCC0	CE00	CF40	D080	D1C0	D300	D440	D580	D6C0	D800	D940	DA80	DBC0
17	11	C910	CA50	CB90	CCD0	CE10	CF50	D090	D1D0	D310	D450	D590	D6D0	D810	D950	DA90	DBD0
18	12	C920	CA60	CBA0	CCE0	CE20	CF60	D0A0	D1E0	D320	D460	D5A0	D6E0	D820	D960	DAA0	DBE0
19	13	C930	CA70	CBB0	CCF0	CE30	CF70	D0B0	D1F0	D330	D470	D5B0	D6F0	D830	D970	DAB0	DBF0

Table 6-5l. Sector Addresses, Cylinders B0-BF

Cylinder																	
Decimal:		176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
Hexadecimal:		B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
Track (Head)																	
Dec.	Hex.																
0	0	DC00	DD40	DE80	DFC0	E100	E240	E380	E4C0	E600	E740	E880	E9C0	EB00	EC40	ED80	EEC0
1	1	DC10	DD50	DE90	DFD0	E110	E250	E390	E4D0	E610	E750	E890	E9D0	EB10	EC50	ED90	EED0
2	2	DC20	DD60	DEA0	DFE0	E120	E260	E3A0	E4E0	E620	E760	E8A0	E9E0	EB20	EC60	EDA0	EEE0
3	3	DC30	DD70	DEB0	DFF0	E130	E270	E3B0	E4F0	E630	E770	E8B0	E9F0	EB30	EC70	EDB0	EEF0
4	4	DC40	DD80	DEC0	E000	E140	E280	E3C0	E500	E640	E780	E8C0	EA00	EB40	EC80	EDC0	EF00
5	5	DC50	DD90	DED0	E010	E150	E290	E3D0	E510	E650	E790	E8D0	EA10	EB50	EC90	EDD0	EF10
6	6	DC60	DDA0	DEE0	E020	E160	E2A0	E3E0	E520	E660	E7A0	E8E0	EA20	EB60	ECA0	EDE0	EF20
7	7	DC70	DDB0	DEF0	E030	E170	E2B0	E3F0	E530	E670	E7B0	E8F0	EA30	EB70	ECB0	EDF0	EF30
8	8	DC80	DDC0	DF00	E040	E180	E2C0	E400	E540	E680	E7C0	E900	EA40	EB80	ECC0	EE00	EF40
9	9	DC90	DDD0	DF10	E050	E190	E2D0	E410	E550	E690	E7D0	E910	EA50	EB90	ECD0	EE10	EF50
10	A	DCA0	DDE0	DF20	E060	E1A0	E2E0	E420	E560	E6A0	E7E0	E920	EA60	EBA0	ECE0	EE20	EF60
11	B	DCB0	DDF0	DF30	E070	E1B0	E2F0	E430	E570	E6B0	E7F0	E930	EA70	EBB0	ECF0	EE30	EF70
12	C	DCC0	DE00	DF40	E080	E1C0	E300	E440	E580	E6C0	E800	E940	EA80	EBC0	ED00	EE40	EF80
13	D	DCD0	DE10	DF50	E090	E1D0	E310	E450	E590	E6D0	E810	E950	EA90	EBD0	ED10	EE50	EF90
14	E	DCE0	DE20	DF60	E0A0	E1E0	E320	E460	E5A0	E6E0	E820	E960	EAA0	EBE0	ED20	EE60	EFA0
15	F	DCF0	DE30	DF70	E0B0	E1F0	E330	E470	E5B0	E6F0	E830	E970	EAB0	EBF0	ED30	EE70	EFB0
16	10	DD00	DE40	DF80	E0C0	E200	E340	E480	E5C0	E700	E840	E980	EAC0	EC00	ED40	EE80	EFC0
17	11	DD10	DE50	DF90	E0D0	E210	E350	E490	E5D0	E710	E850	E990	EAD0	EC10	ED50	EE90	EFD0
18	12	DD20	DE60	DFA0	E0E0	E220	E360	E4A0	E5E0	E720	E860	E9A0	EAE0	EC20	ED60	EEA0	EFE0
19	13	DD30	DE70	DFB0	E0F0	E230	E370	E4B0	E5F0	E730	E870	E9B0	EAF0	EC30	ED70	EEB0	EFF0

Table 6-5m. Sector Addresses, Cylinders C0-CA

Cylinder																	
Decimal:		192	193	194	195	196	197	198	199	200	201	202					
Hexadecimal:		C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA					
Track (Head)																	
Dec.	Hex.																
0	0	F000	F140	F280	F3C0	F500	F640	F780	F8C0	FA00	FB40	FC80					
1	1	F010	F150	F290	F3D0	F510	F650	F790	F8D0	FA10	FB50	FC90					
2	2	F020	F160	F2A0	F3E0	F520	F660	F7A0	F8E0	FA20	FB60	FCA0					
3	3	F030	F170	F2B0	F3F0	F530	F670	F7B0	F8F0	FA30	FB70	FCB0					
4	4	F040	F180	F2C0	F400	F540	F680	F7C0	F900	FA40	FB80	FCC0					
5	5	F050	F190	F2D0	F410	F550	F690	F7D0	F910	FA50	FB90	FCD0					
6	6	F060	F1A0	F2E0	F420	F560	F6A0	F7E0	F920	FA60	FBA0	FCE0					
7	7	F070	F1B0	F2F0	F430	F570	F6B0	F7F0	F930	FA70	FBB0	FCF0					
8	8	F080	F1C0	F300	F440	F580	F6C0	F800	F940	FA80	FBC0	FD00					
9	9	F090	F1D0	F310	F450	F590	F6D0	F810	F950	FA90	FBD0	FD10					
10	A	F0A0	F1E0	F320	F460	F5A0	F6E0	F820	F960	FAA0	FBE0	FD20					
11	B	F0B0	F1F0	F330	F470	F5B0	F6F0	F830	F970	FAB0	FBF0	FD30					
12	C	F0C0	F200	F340	F480	F2C0	F700	F840	F980	FAC0	FC00	FD40					
13	D	F0D0	F210	F350	F490	F5D0	F710	F850	F990	FAD0	FC10	FD50					
14	E	F0E0	F220	F360	F4A0	F5E0	F720	F860	F9A0	FAE0	FC20	FD60					
15	F	F0F0	F230	F370	F4B0	F5F0	F730	F870	F9B0	FAF0	FC30	FD70					
16	10	F100	F240	F380	F4C0	F600	F740	F880	F9C0	FB00	FC40	FD80					
17	11	F110	F250	F390	F4D0	F610	F750	F890	F9D0	FB10	FC50	FD90					
18	12	F120	F260	F3A0	F4E0	F620	F760	F8A0	F9E0	FB20	FC60	FDA0					
19	13	F130	F270	F3B0	F4F0	F630	F770	F8B0	F9F0	FB30	FC70	FDB0					

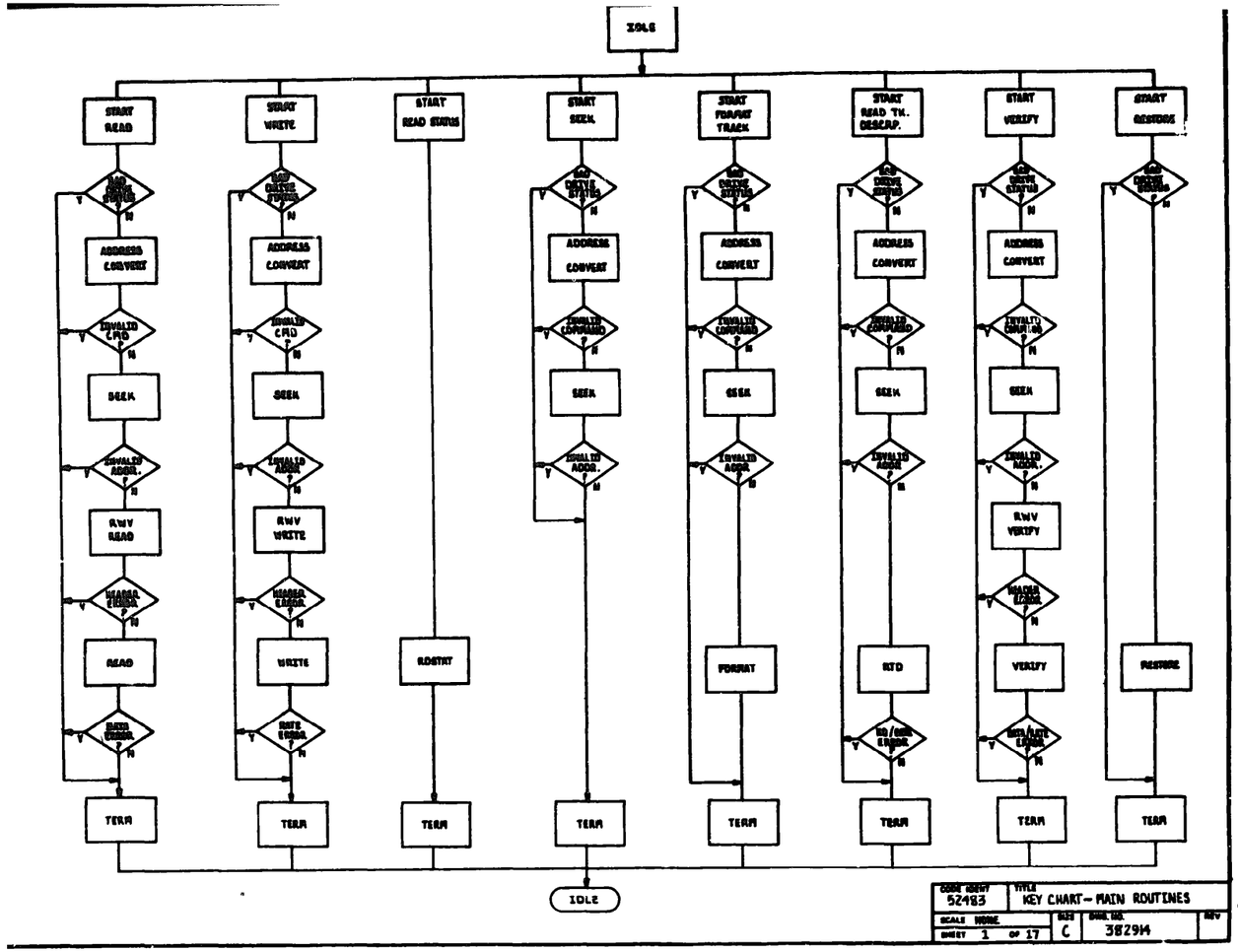
APPENDIX A
MICROPROGRAM FLOWCHARTS

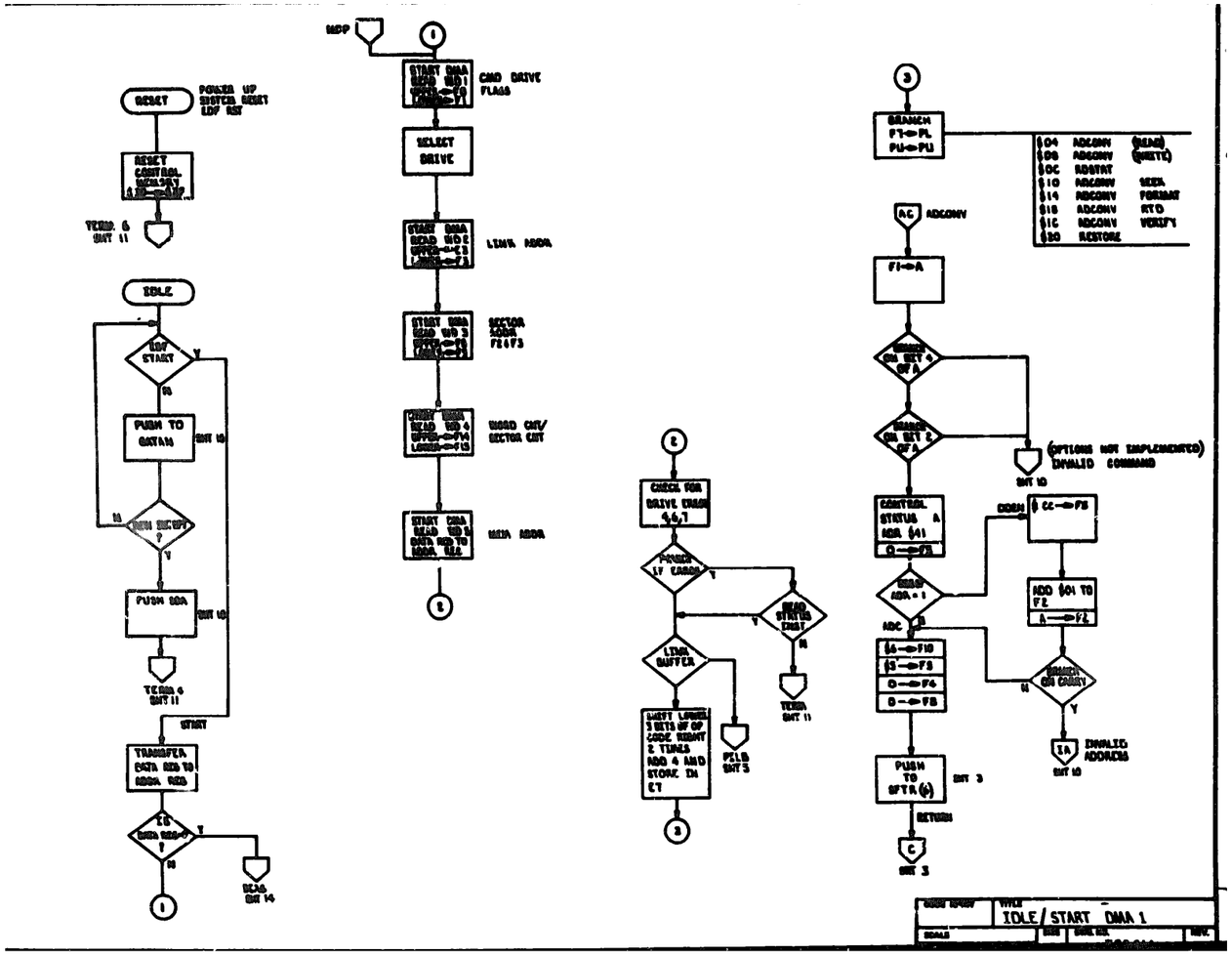
A.1 GENERAL

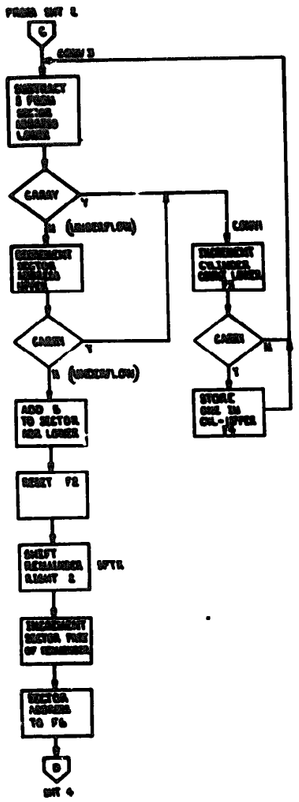
This appendix contains the flowcharts for the microprogram logic. The first flowchart is the keychart. Each rectangular block represents a subroutine. The first eight blocks indicate the initiating routines for the eight operational functions of the controller, which are:

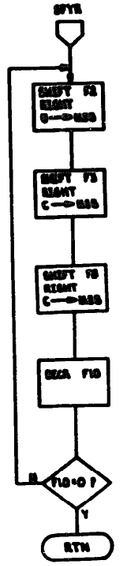
- *Seek*
- *Restore*
- Write
- Format Track
- Read
- Read Track *Descriptor*
- Verify
- Read Status

Starting from the idle state each operation is started with the initiating routine. *Under* it are listed the various subroutines that *are* needed to implement the function. Each subroutine cross references to the succeeding flowcharts where the particular subroutine can be found. After each subroutine, a check is made for proper execution. At the successful completion of the entire operation, the controller reverts back to the idle state.

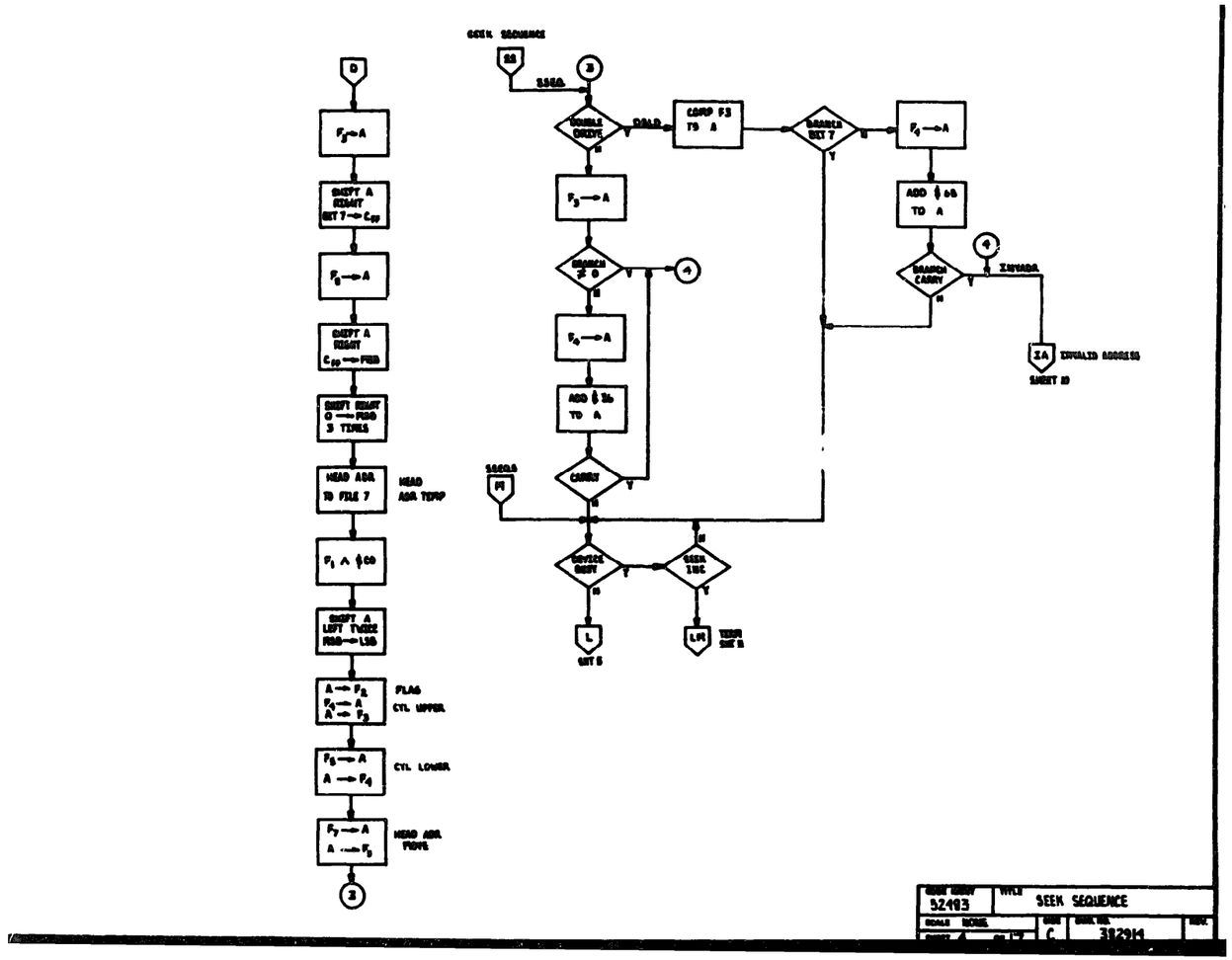

IOS.S
START READ
START WRITE
START READ STATUS
START SEEK
START FORMAT TRACK
START READ TK. DESCRIP.
START VERIFY
START RESTORE
ADDRESS CONVERT
SEEK
RWV READ
RWV WRITE
RWV VERIFY
READ
WRITE
VERIFY
FORMAT
RSTRT
RESTORE
RTD
TERM
IDLE
KEY CHART - MAIN ROUTINES
52483
382914
C
SHEET 1 OF 17

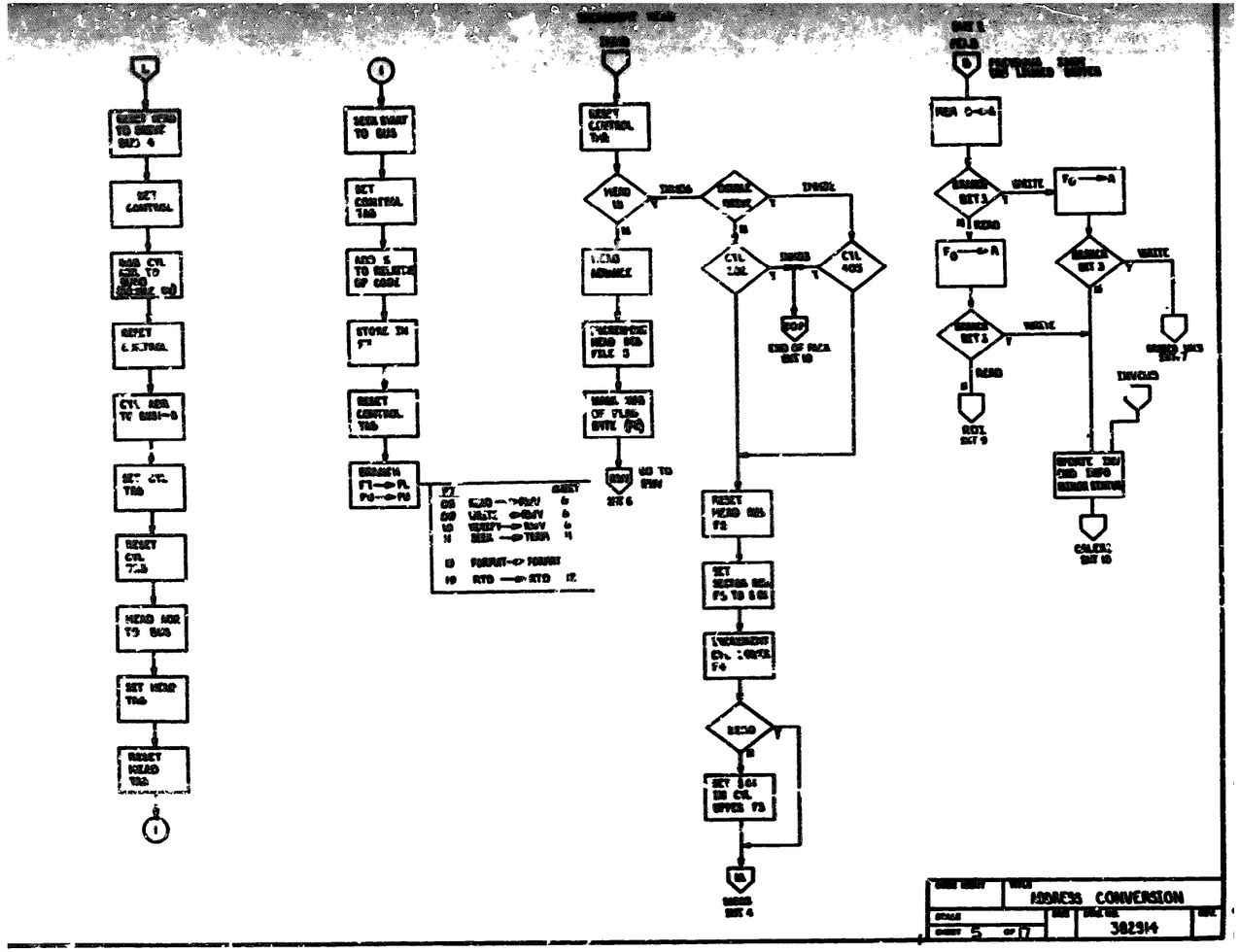

RESET
POWER UP
RESET
IDLE
IDLE START ?
PUSH TO
PUSH SDA
TRANSFER
START
MPP
SELECT
DRIVE
LINK ADDR
SECTOR
HEAD CNT/
SECTOR CNT
DATA ADDR
CHECK FOR
DRIVE ERROR
5,6,7
LINK
BUFFER
FIELD
BRANCH
FI→PL
PU→PU
ADCONV
FI→A
CONTROL
STATUS A
ADR $41
ADD $01 TO
F2
PUSH
TO
INVALID
ADDRESS
IDLE / START DMA 1


FROM INT 1
C
COMM 3
SUBTRACT
CARRY
Y
N (UNDERFLOW)
CARRY
Y
N (UNDERFLOW)
ADD 1
RESET F2
SHIFT
SHIFT
INT 4

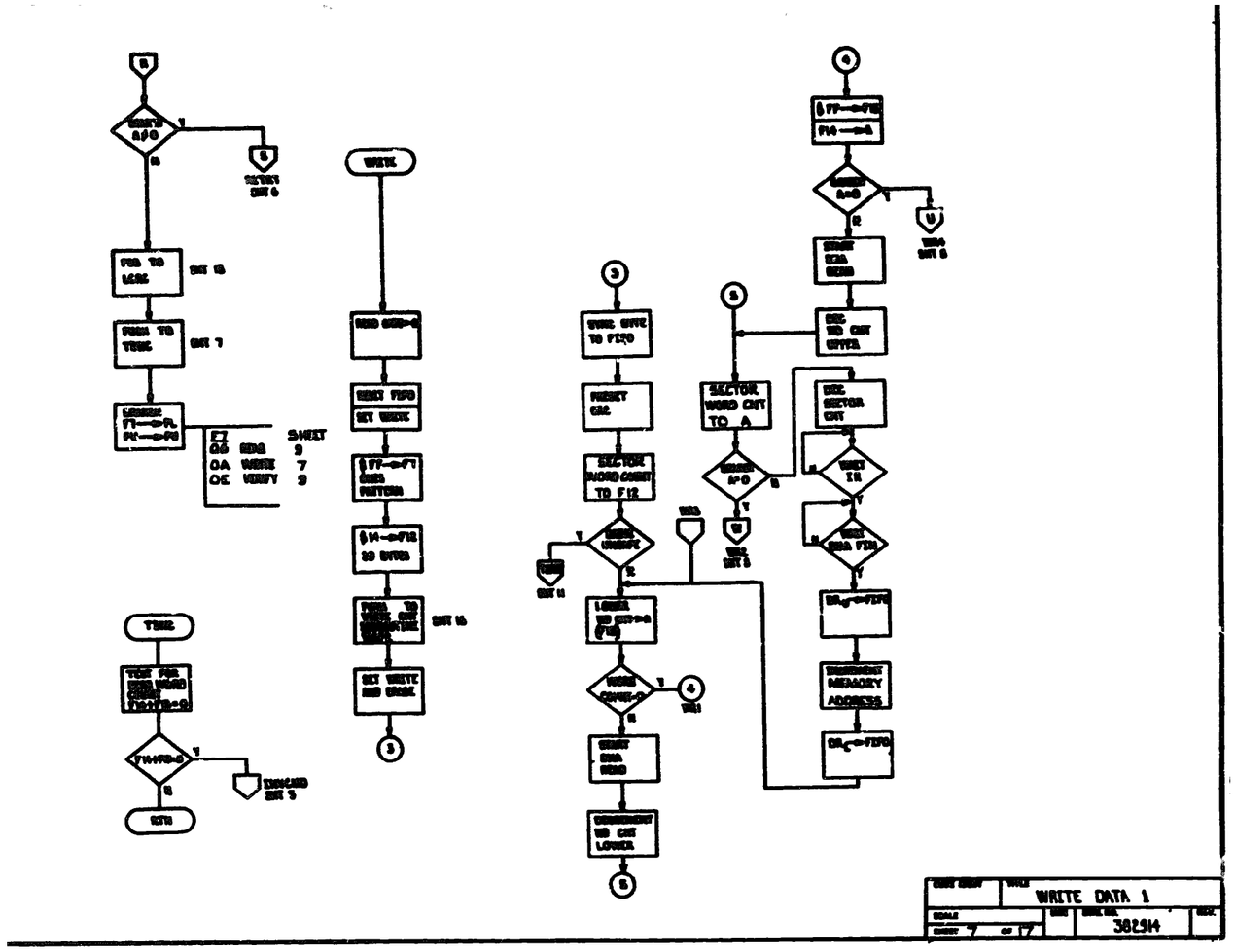

SFTR
SHIFT F2
SHIFT F3
SHIFT F8
DECR F10
F10=0 ?
Y
RTN

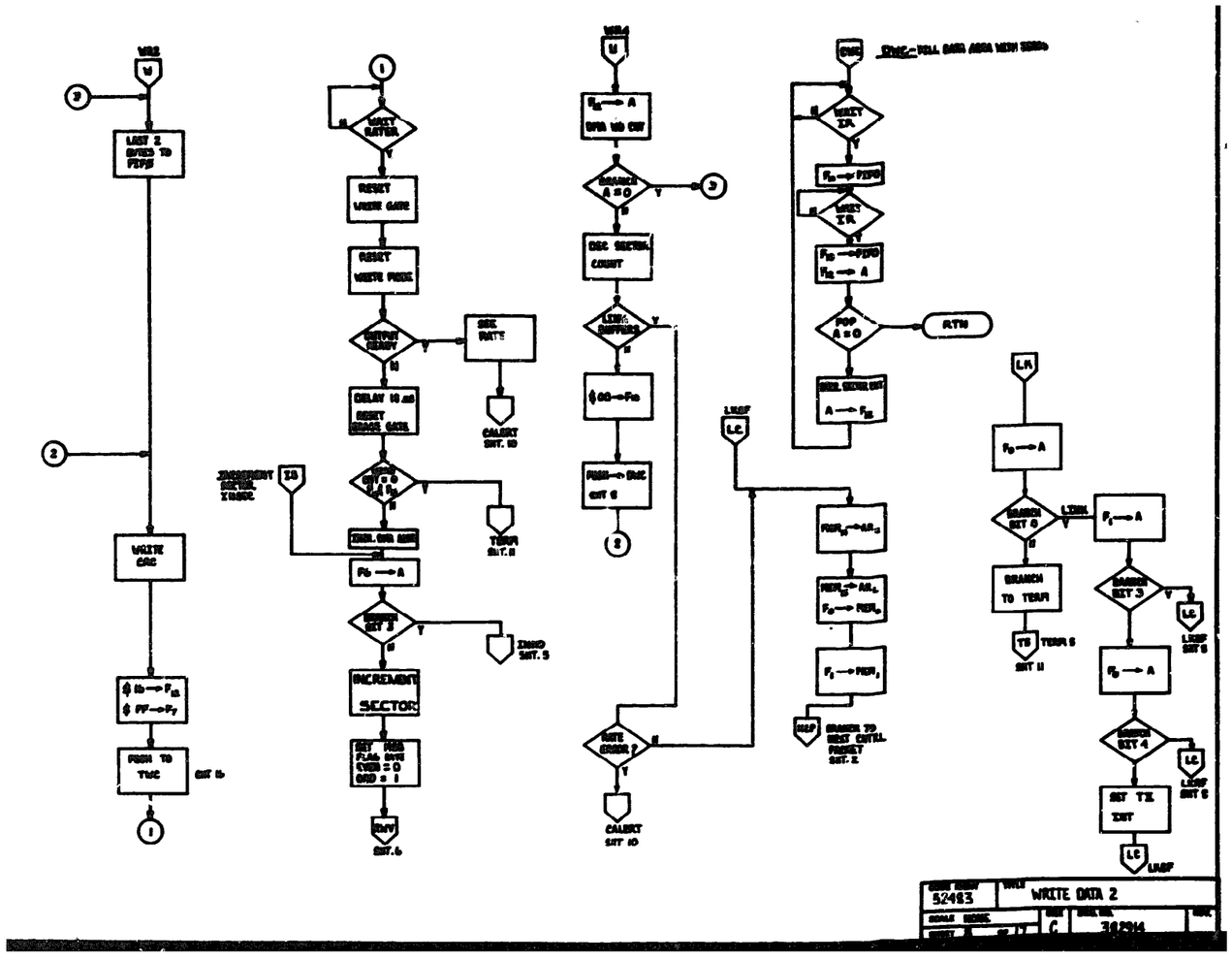
TITLE
START DMA & SFTR
382914

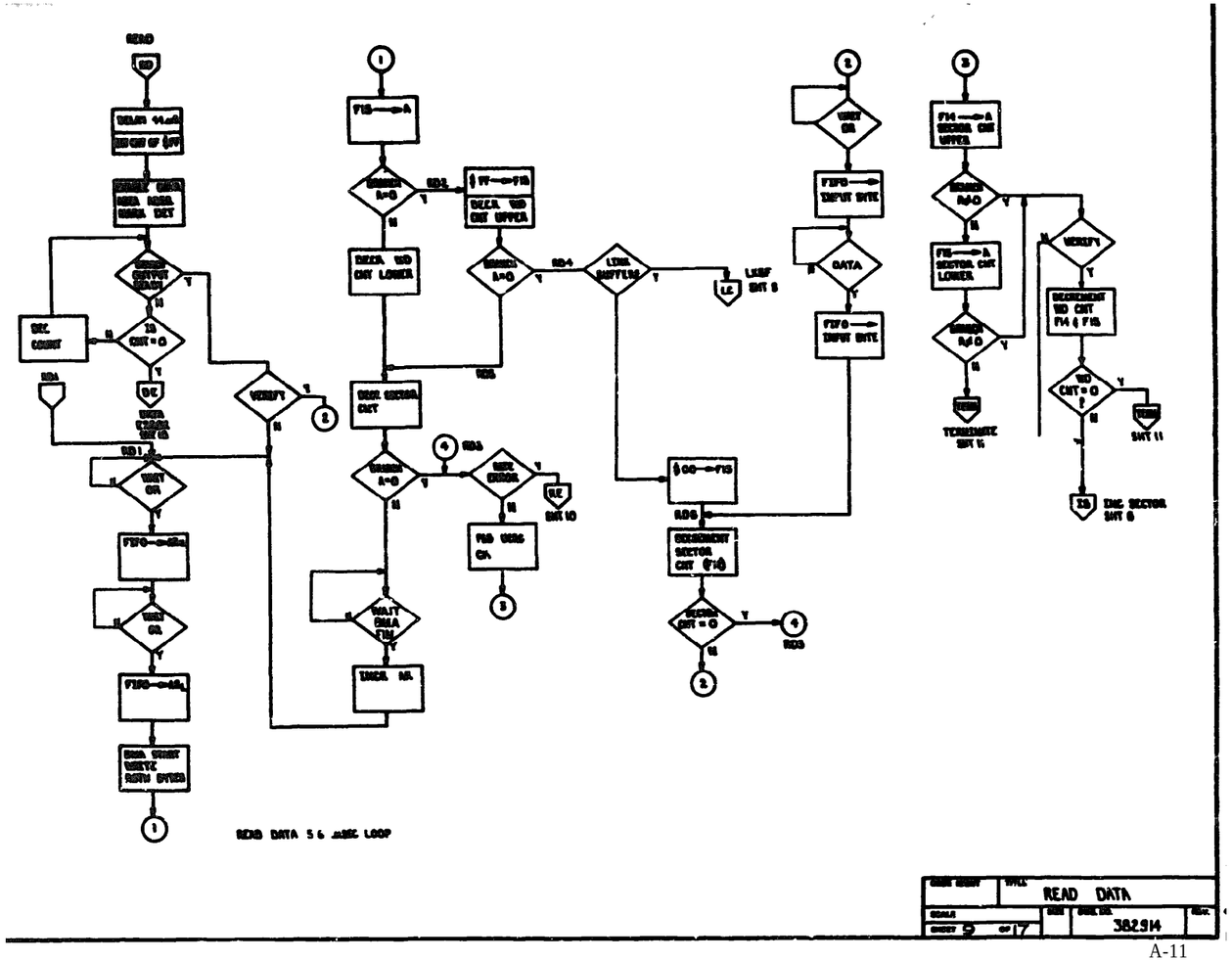

SEEK SEQUENCE
SS
SSEQA
B
DOUBLE DENSITY
SSEQB
CONV F3 TO A
BRANCH BIT 7
F4 → A
F3 → A
ADD $40 TO A
BRANCH ≠ 0
A
BRANCH CARRY
IA
INVADA
INVALID ADDRESS
SHEET 10
F2 → A
ADD $36 TO A
CARRY
SSEQB
F8
DEVICE BUSY
SEEK INC
L
SET S
LM
SET S
D
F1 → A
SHIFT A RIGHT BIT 7 → C80
F0 → A
SHIFT A RIGHT C80 → F0B0
SHIFT RIGHT 0 → F0B0 3 TIMES
HEAD ADR TO FILE 7
HEAD ADR TEMP
F1 A $60
SHIFT A LEFT TWICE F0B0 → LSB
A → F2
F1 → A
A → F3
FLAG CYL UPPER
F5 → A
A → F4
CYL LOWER
F7 → A
A → F5
HEAD ADR FIVE
B
52493
SEEK SEQUENCE
C
382914

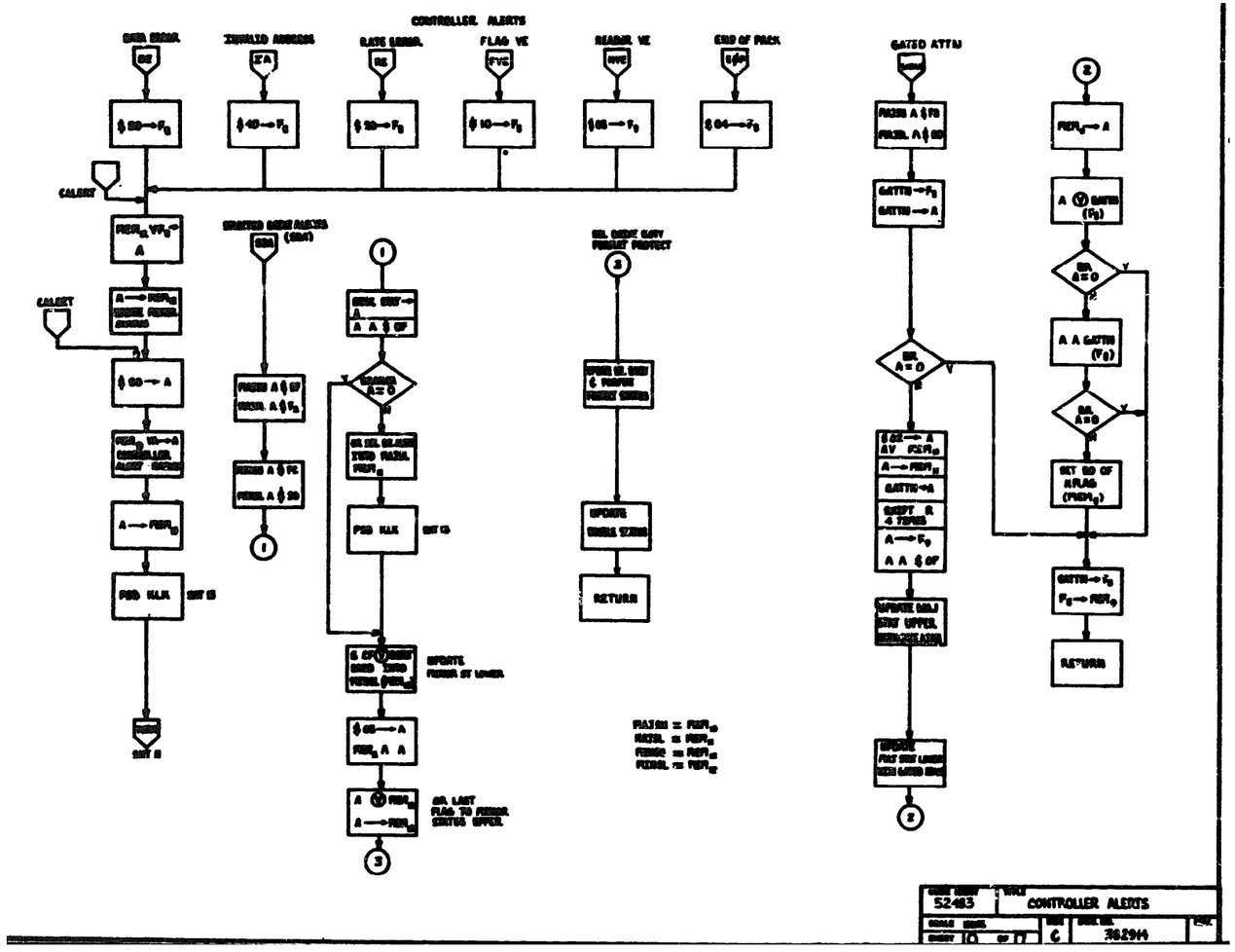

ADDRESS CONVERSION
382914

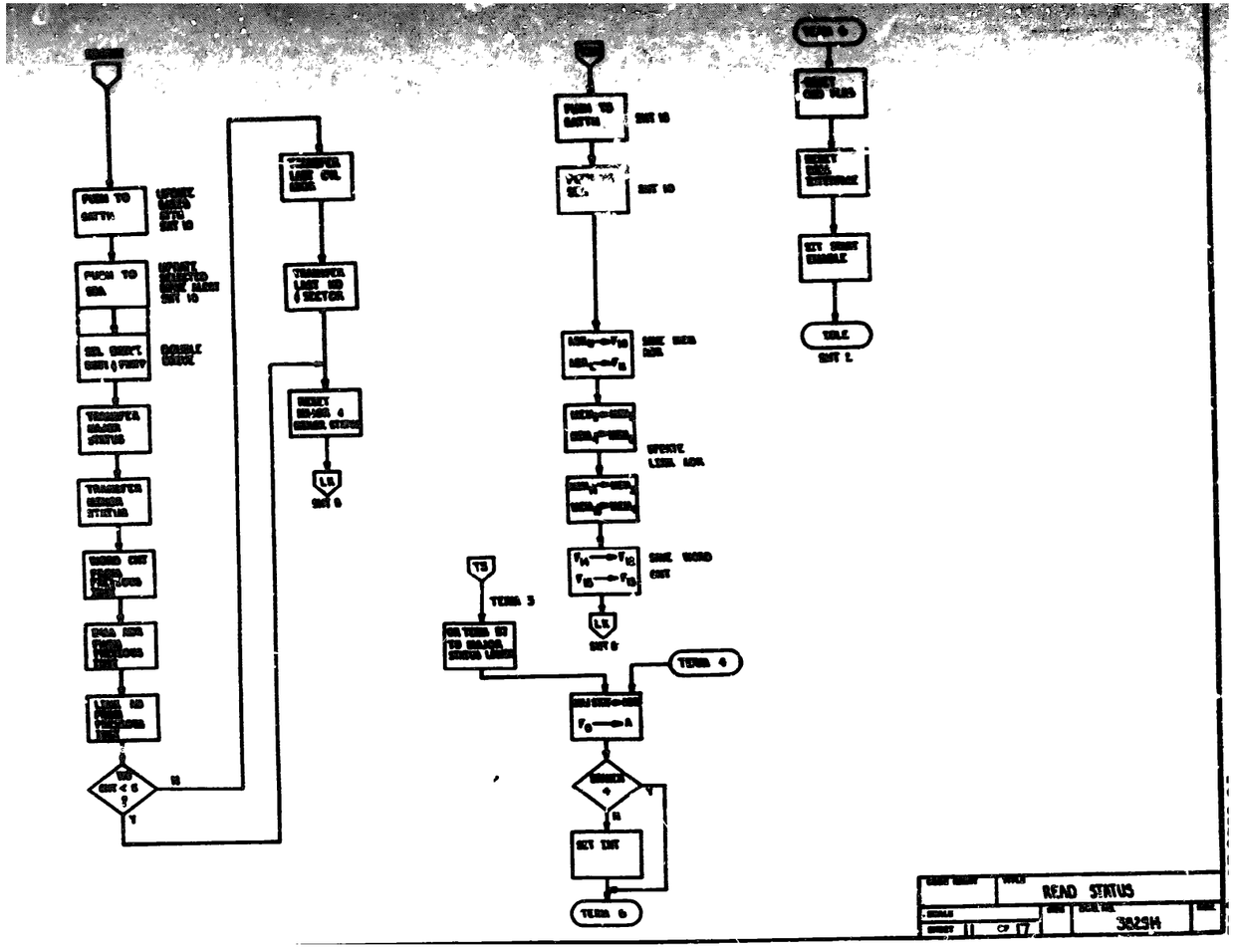
DRIVE READY
SET SELECT HD & HEAD GATE
DELAY 10 SEC
SET: AM SEC, 2 ERROR & RD RR
SELECT FIFO
CONTROL BYTE → A R/O
RETRY
DRIVE READY
YES
NO
DRIVE LOOP CNT
LOOP CNT = 0
RESET AM SEC.
RETRY SHT. 5
FLAG BYTE TO FACH 0
A ⓥ F2
ERROR SET 0
ERROR SET 4,7
FVE
FLAG VERIFY ERROR, ANT. RD
FIFO → A UPPER CYL BYTE
A ⓥ F3
2
FIFO → A LOWER CYL BYTE
A ⓥ F4
ERROR A ≠ 0
DATA
FIFO → A ZERO CNT.
3
FIFO → A HEAD ADR.
A ⓥ F5
FIFO → A SECTOR
A ⓥ F6
FIFO → A ZERO DATA
4
01 → F15
A ⓥ F15
5A → F15
FIFO → A BYTE 1 OF DATA LENGTH
FIFO → A BYTE 2 OF DATA LENGTH
A ⓥ F15
R
FIND AND COMPARE DATA (BYTE) HEADERS
52485
READ/WRITE/VERIFY
C

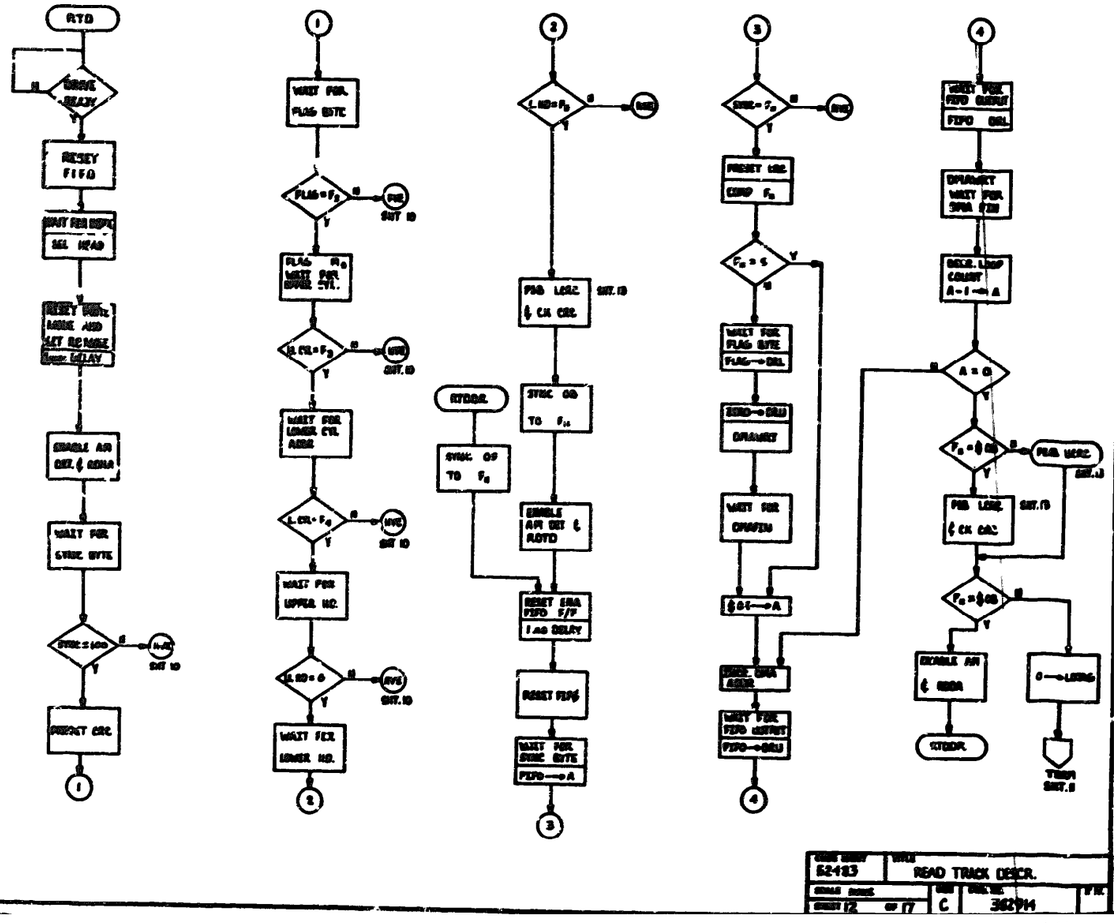

WRITE
TEST
WRITE DATA 1
382914

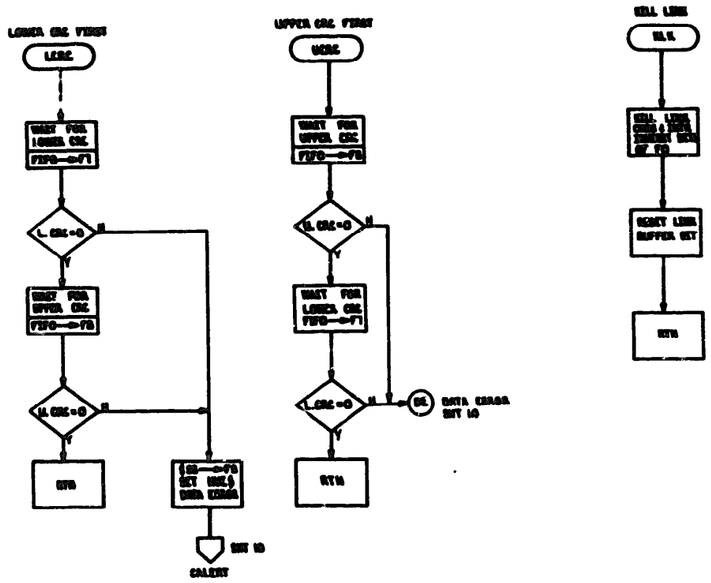

WRITE DATA 2
52483
C
30294


READ
DATA 14 mS
SEC COUNT
VERIFY
DMA ERROR
SEC ERROR
WAIT DMA FIN
INCR SR
LOAD BUFFER
LEOF BIT 8
BIT 10
DECREMENT SECTOR CNT (FA)
DECREMENT WD CNT FA & FB
WD CNT = 0
BIT 11
INC SECTOR BIT 6
TERMINATE BIT 14
READ DATA S & SEC LOOP
READ DATA
38291H

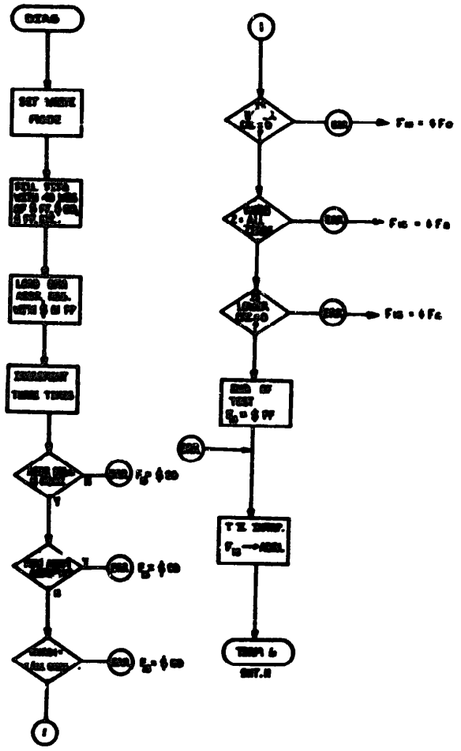

CONTROLLER ALERTS
CALLSET
RETURN
52483
CONTROLLER ALERTS
C
36294


READ STATUS
3829M

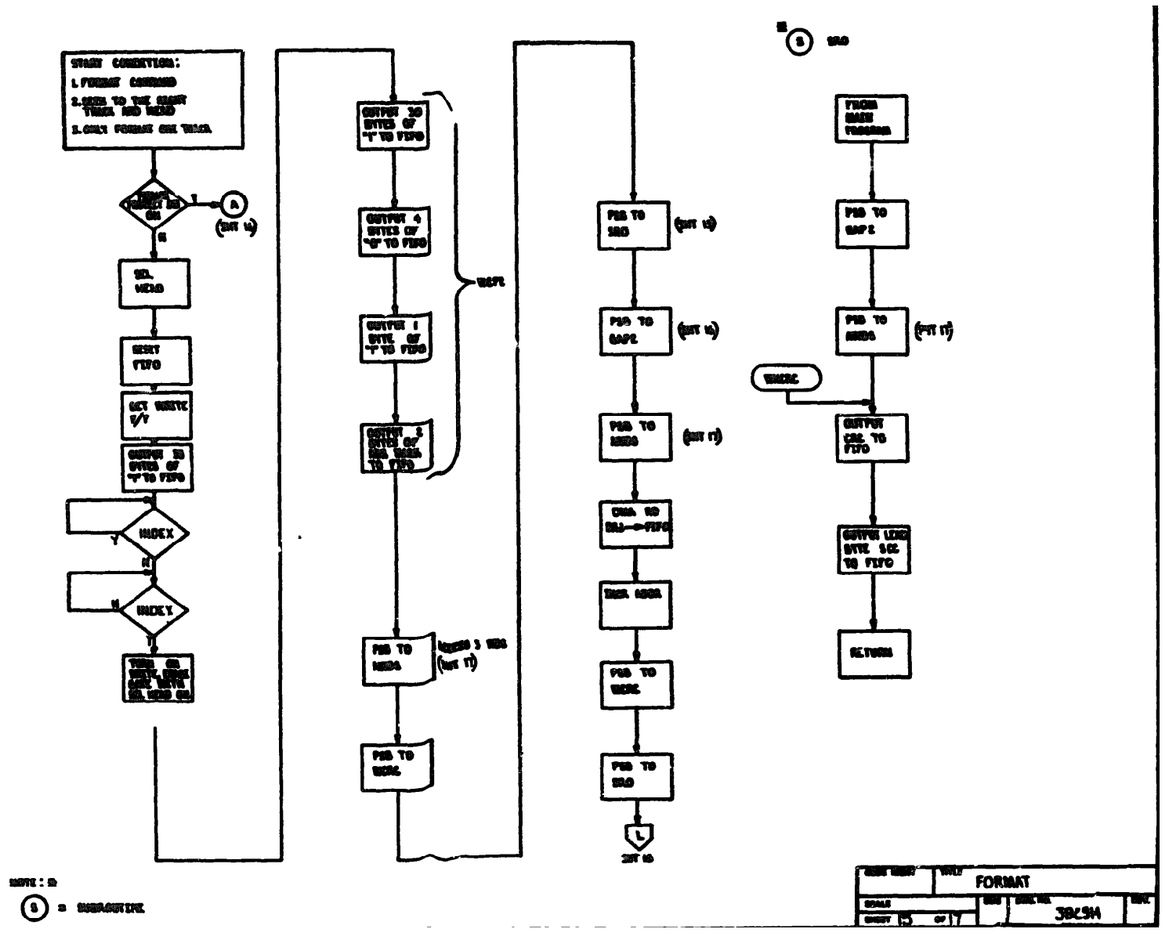

RTD
RESET FIFO
ENABLE AIR DET. & ADMA
WAIT FOR SYNC BYTE
DISREGT CRC
WAIT FOR FLAG BYTE
WAIT FOR UPPER NO.
WAIT FOR LOWER NO.
WAIT FOR SYNC OR TO $_{16}$
ENABLE AIR DET & ADMA
RESET ERR FIFO F/F
1 us DELAY
RESET FIFO
WAIT FOR SYNC BYTE
FIFO → A
WAIT FOR FLAG BYTE
FLAG → DBU
ZERO → DBU
DPRMRST
WAIT FOR DPRMEN
$ 01 → A
WAIT FOR FIFO HSTRST
FIFO → DBU
WAIT FOR FIFO EMPTY
FIFO DBL
DPRMRST WAIT FOR SPA CYC
DECR. LOOP COUNT A - 1 → A
ENABLE AIR & ADMA
0 → LSTAT
52413
READ TRACK DESCR.
C
362944

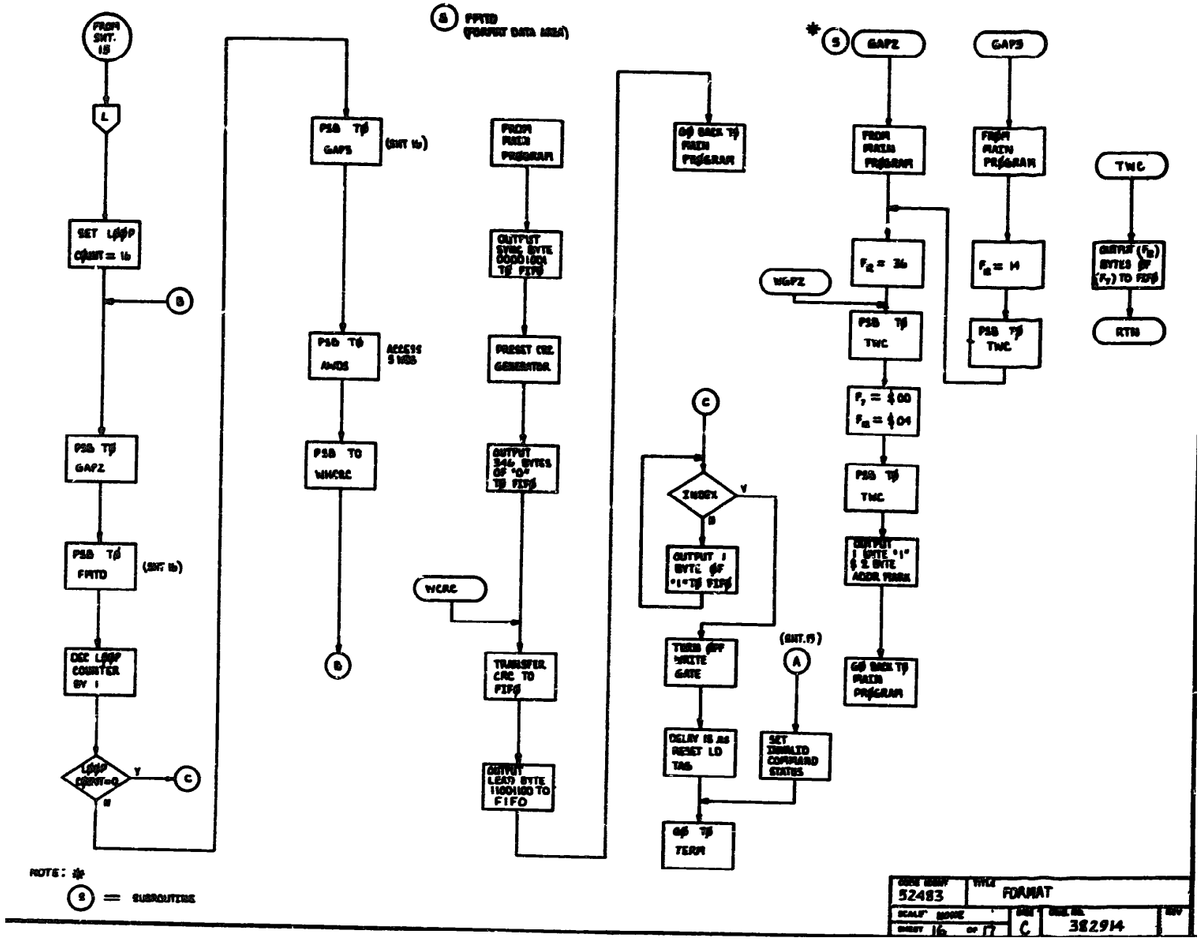


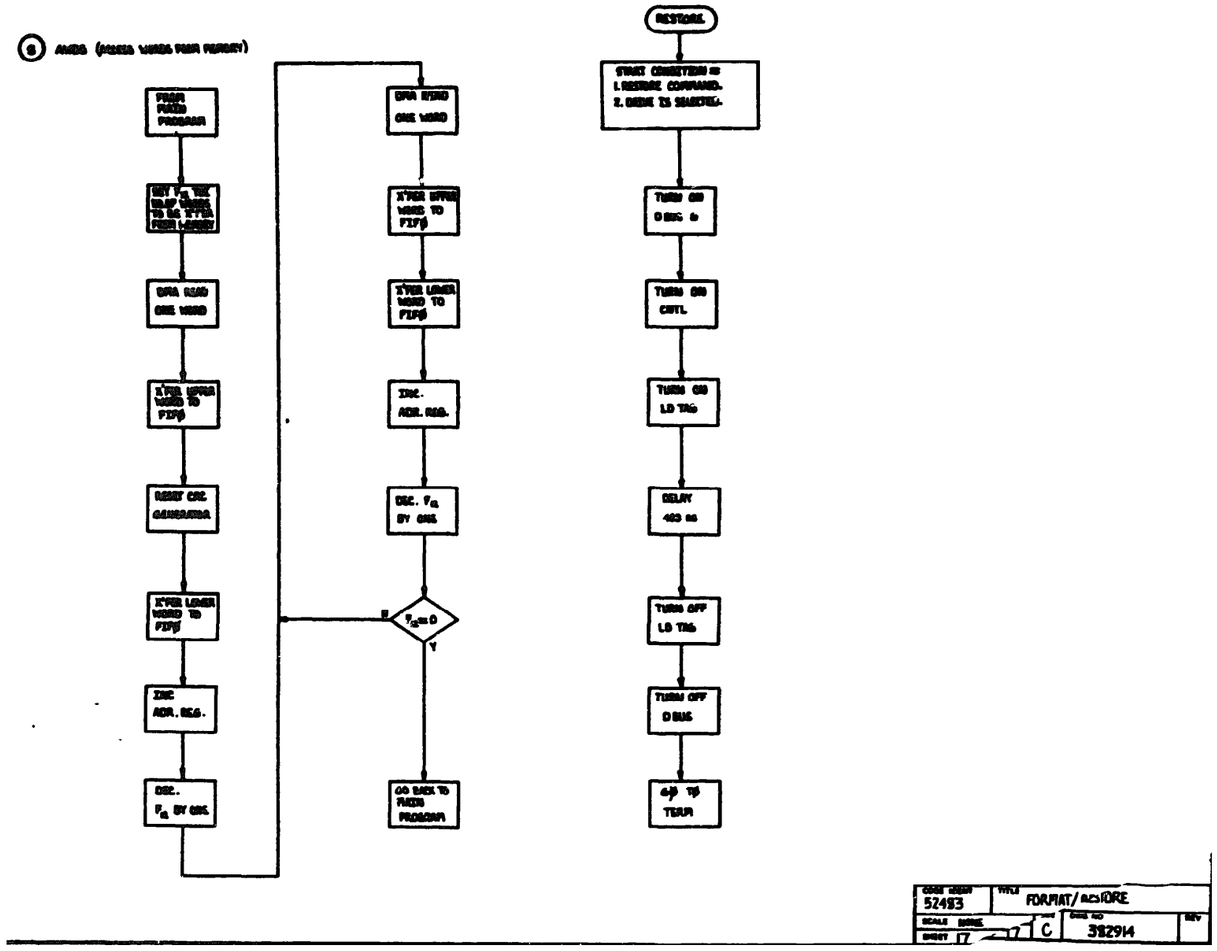
CODE IDENT	TITLE: CRC/RLK		
SCALE	SIZE	CODE NO. 382514	REV.
SHEET 15 OF 17			



62483	TITLE: DIAGNOSTIC		
SCALE: NONE	SHEET 16 OF 17	SIZE: C	DWG. NO. 362914


FORMAT
30L9H


FROM SNT. 18
L
SET LOOP COUNT = 16
B
PSB TO GAPZ
PSB TO FRTD
(SNT 16)
DEC LOOP COUNTER BY 1
LOOP COUNT=0
Y
N
C
PSB TO GAPS
(SNT 16)
PSB TO ANDS
ACCESS S MSB
PSB TO WHCRC
B
A FRTD (FORMAT DATA AREA)
FROM MAIN PROGRAM
OUTPUT SYNC BYTE CODE/ADR TO FIFO
PRESET CRC GENERATOR
OUTPUT 346 BYTES OF "0" TO FIFO
WCRC
TRANSFER CRC TO FIFO
OUTPUT LAST BYTE (ADR) TO FIFO
GO BACK TO MAIN PROGRAM
INDEX
Y
N
OUTPUT 1 BYTE OF "1" TO FIFO
TURN OFF WRITE GATE
DELAY 15 µs RESET LD TAB
GO TO TERM
(SNT.15)
A
SET TRIGATID COMMAND STATES
* S GAPZ
FROM MAIN PROGRAM
WGPZ
PSB TO TWC
$F_y = 100$
$F_{IR} = 104$
PSB TO TWC
OUTPUT 1 BYTE "1" & 2 BYTE ADDR PARM
GO BACK TO MAIN PROGRAM
GAPS
FROM MAIN PROGRAM
$F_{IR} = 14$
PSB TO TWC
TWC
OUTPUT (F_{IR}) BYTES OF (F_y) TO FIFO
RTN
NOTE: *
S = SUBROUTINE
52483
FORMAT
SCALE: NONE
SHEET 16 OF 17
SIZE C
DWG NO. 382914
REV

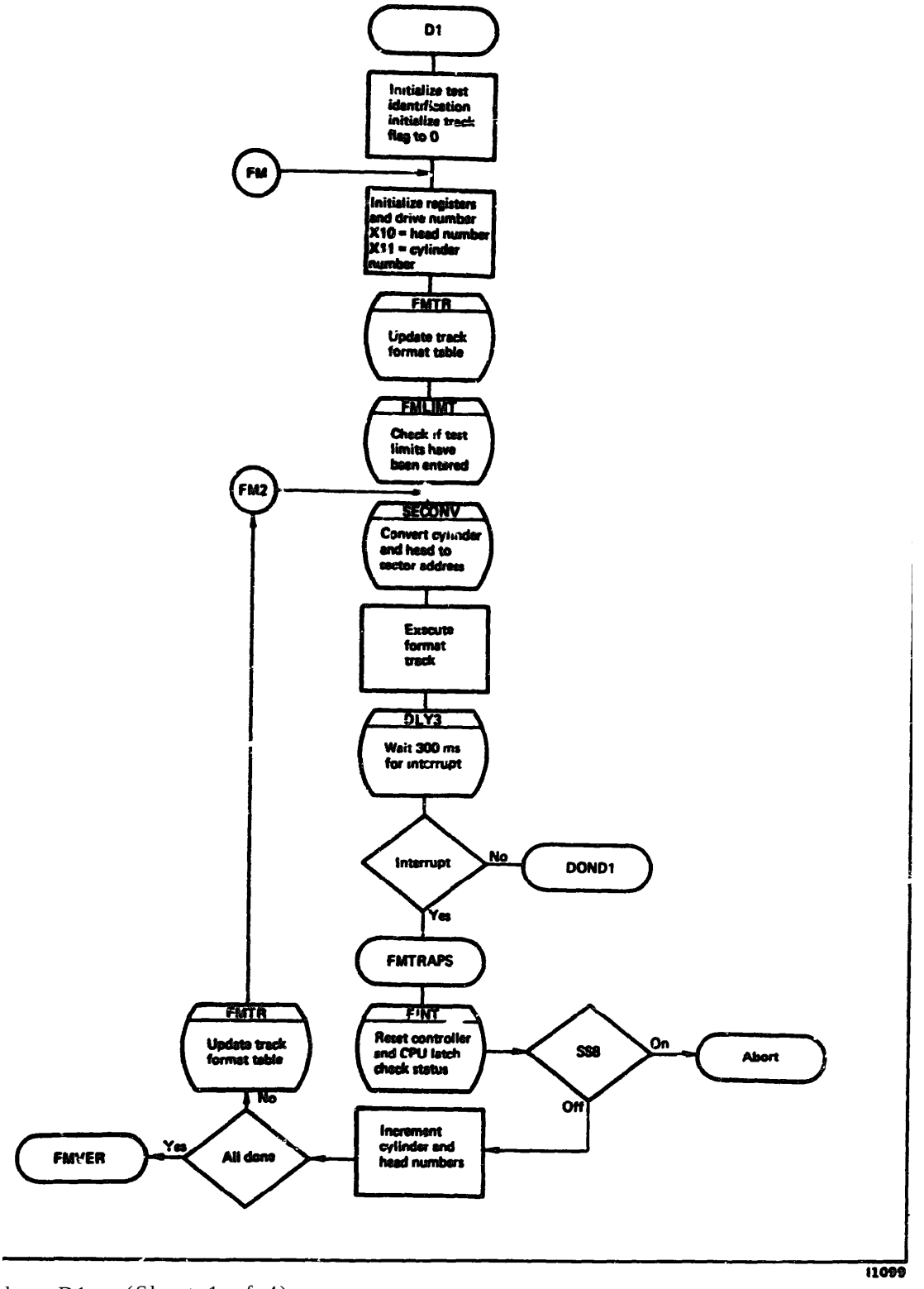

RESTORE
FORMAT
DMA READ
ONE WORD
DMA WRITE
ONE WORD
DEC.
DEC.
GO BACK TO
FORMAT
PROGRAM
TURN ON
TURN ON
CNTL
TURN ON
LD TAG
DELAY
TURN OFF
LD TAG
TURN OFF
D BUS
GO TO
TEST
52483
FORMAT/RESTORE
C
382914

APPENDIX B
DISC UNIT TEST FLOWCHARTS

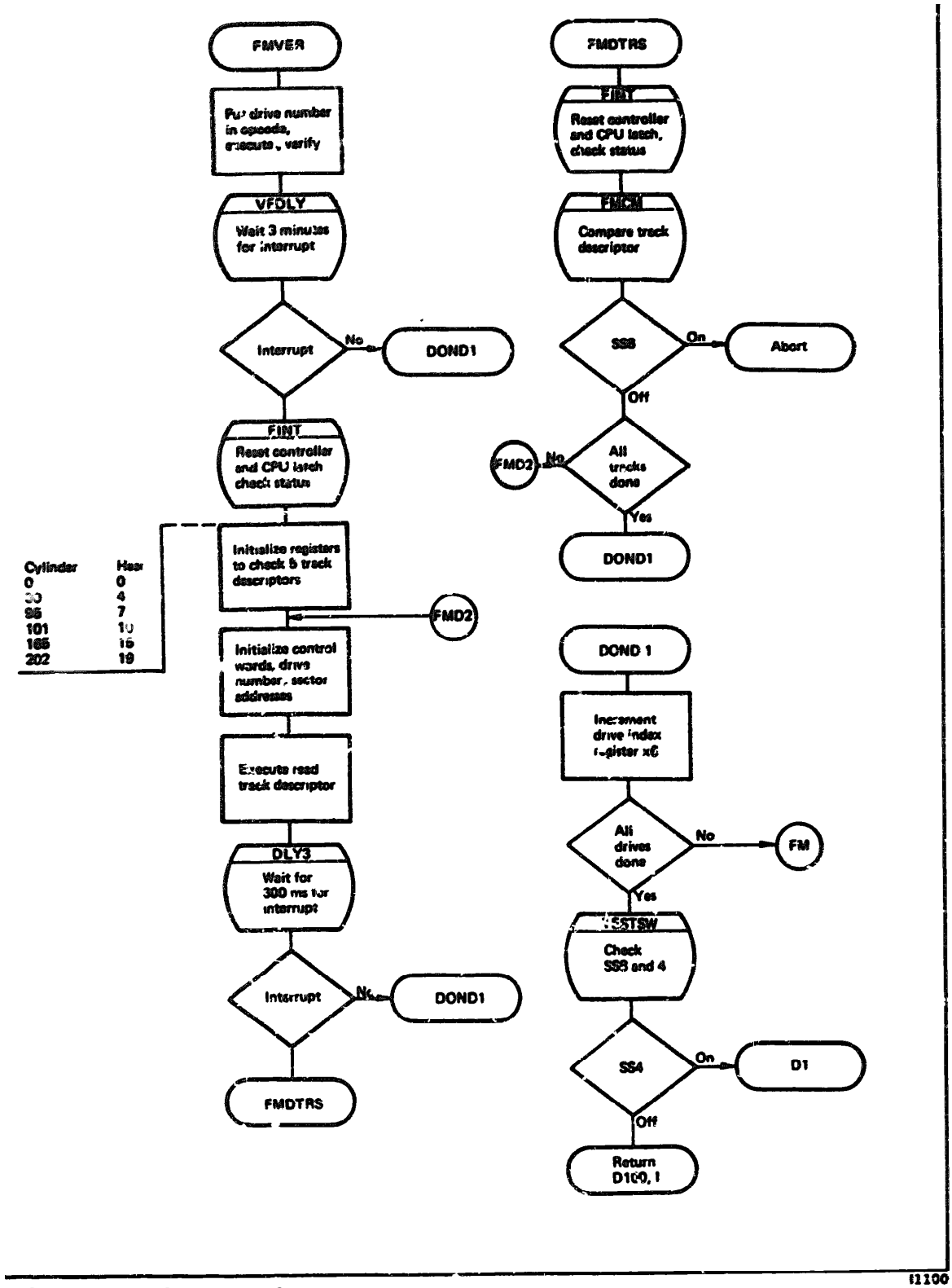
B.1 GENERAL

This appendix contains the flowcharts for the Disk Subsystem Reliability tests subset of the DISC UNIT TEST program. The following is a listing of the test flowcharts.

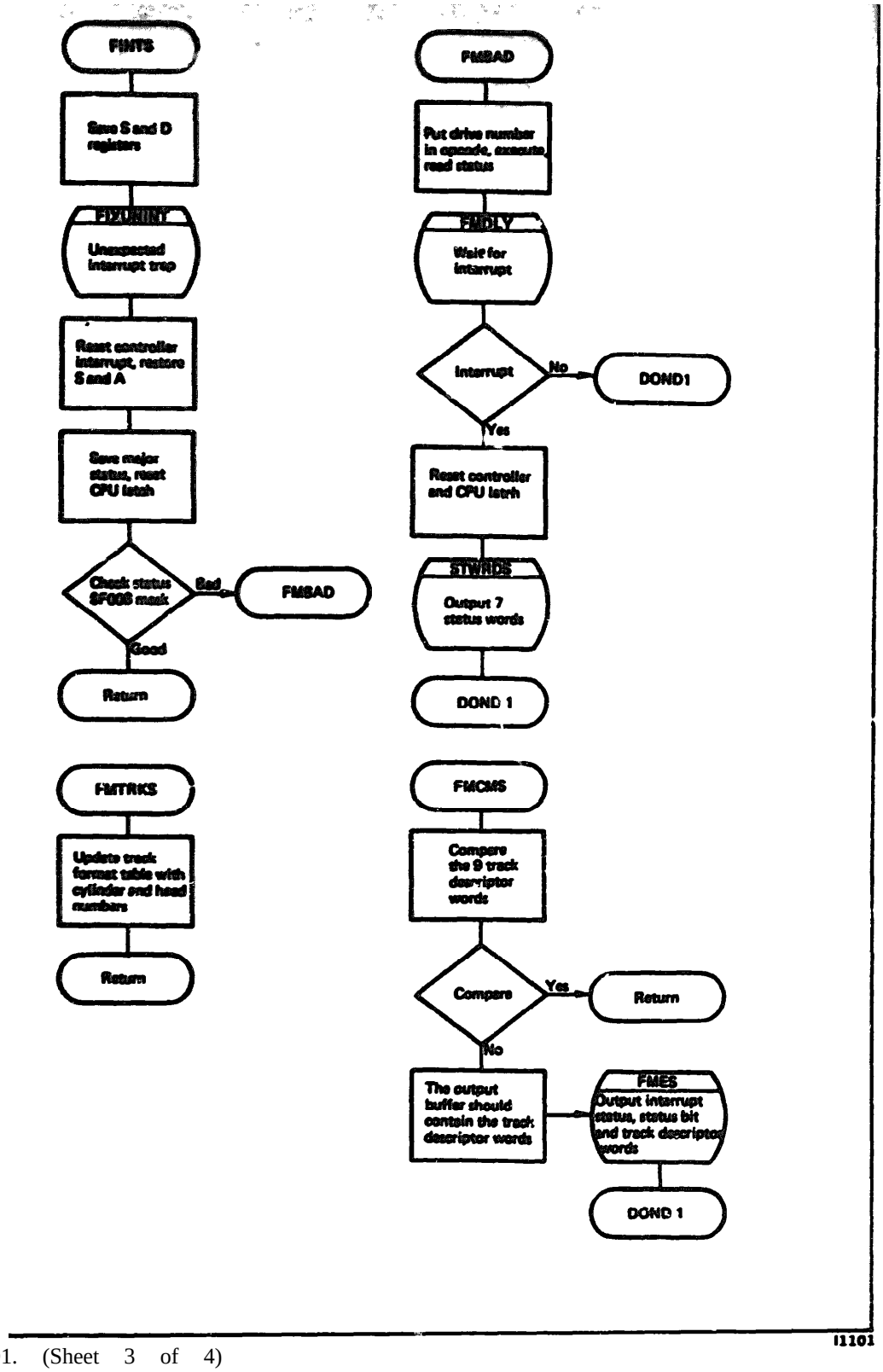
- D1 - Format Track Test.
- D2 - Write Command Chaining Test.
- D3 - Verify Test.
- D4 - Read Command Chaining Test.
- D5 - Write/Read Data Chaining Test.
- D6 - Sequential Seek Test.
- D7 - Incremental/Decremental Seek Test.
- D8 - Random Write/Read Test.



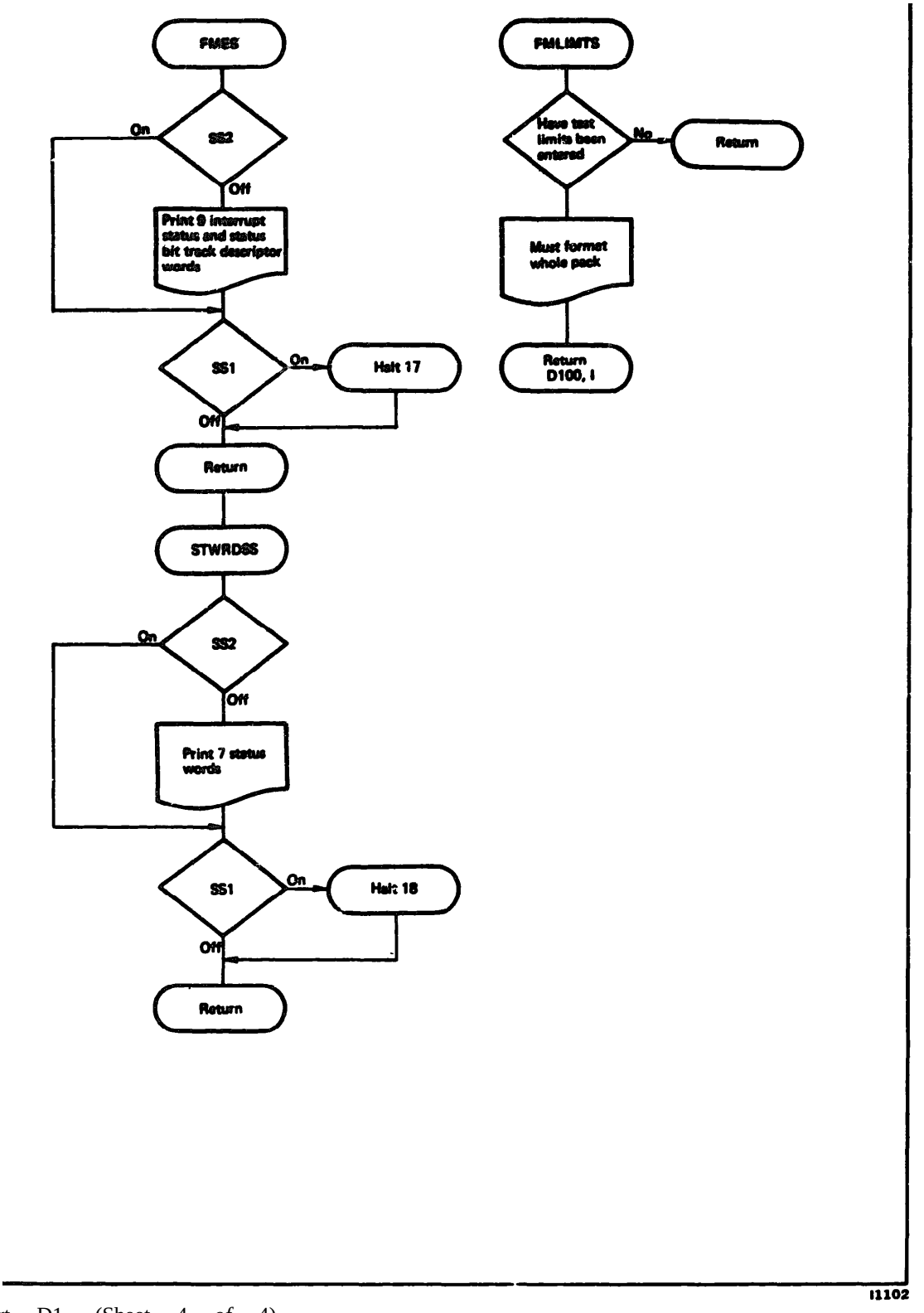
Flowchart D1. (Sheet 1 of 4)



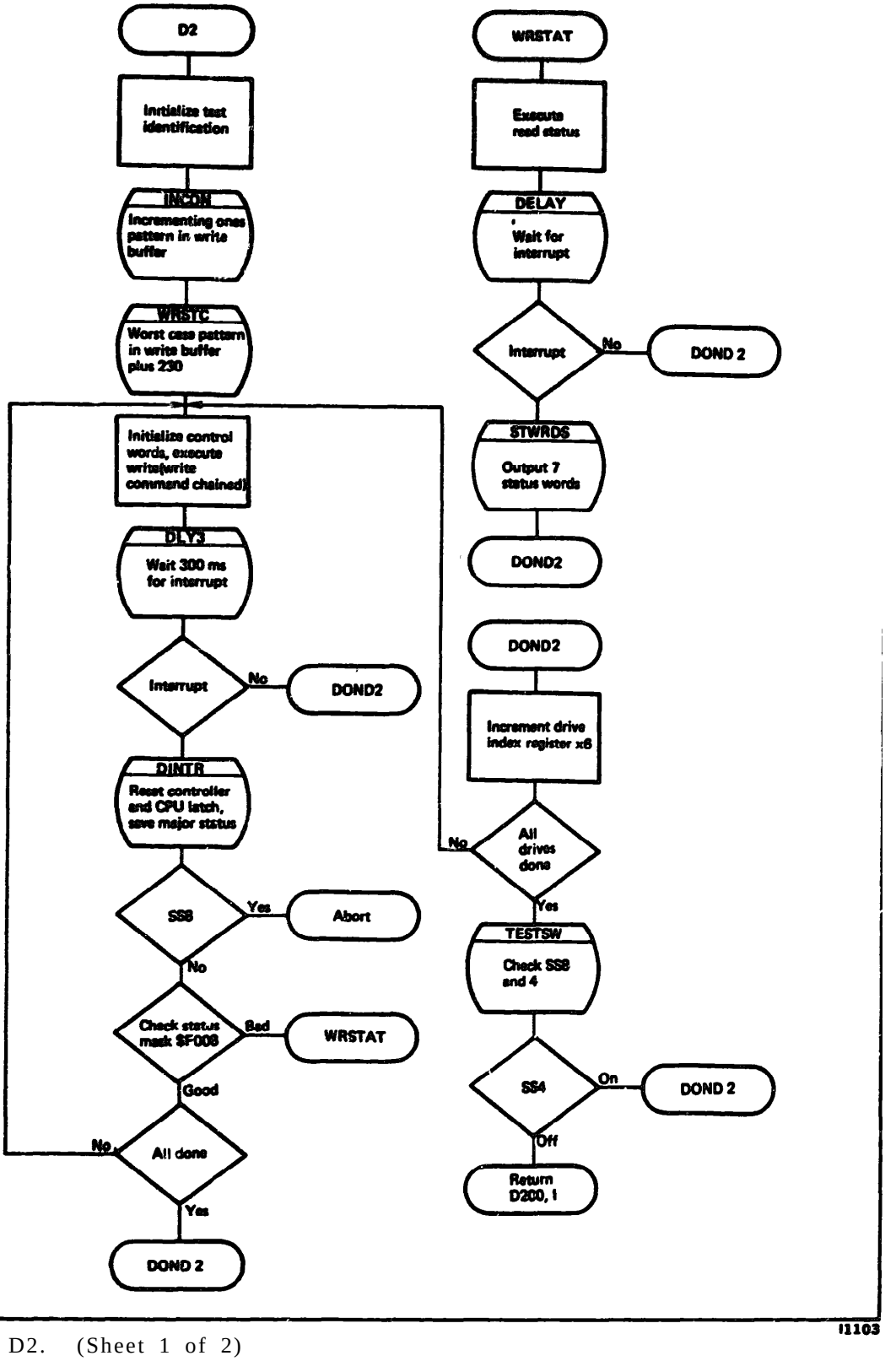
Flowchart D1. (Sheet 2 **of** 4)



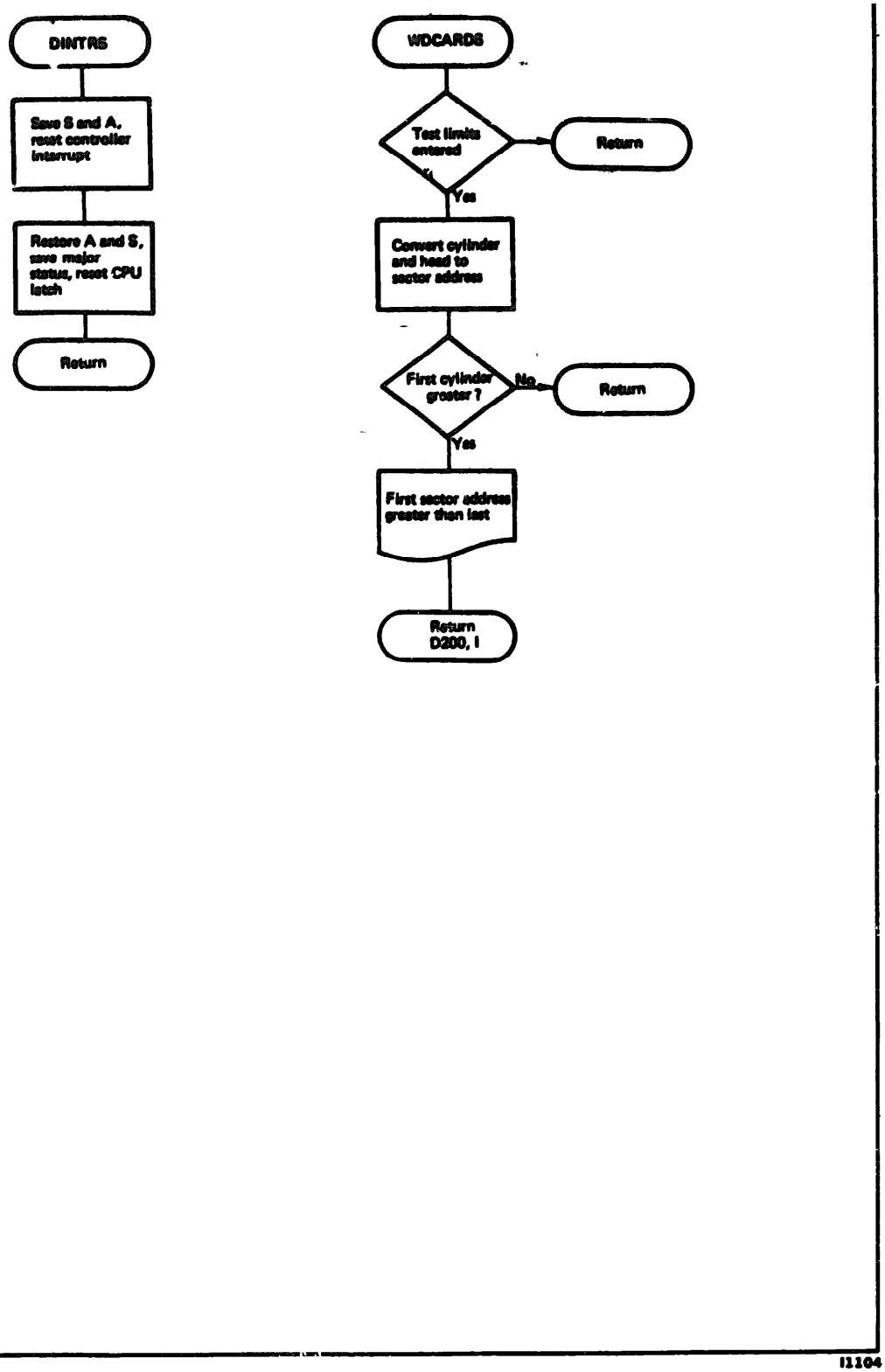
Flowchart D1. (Sheet 3 of 4)



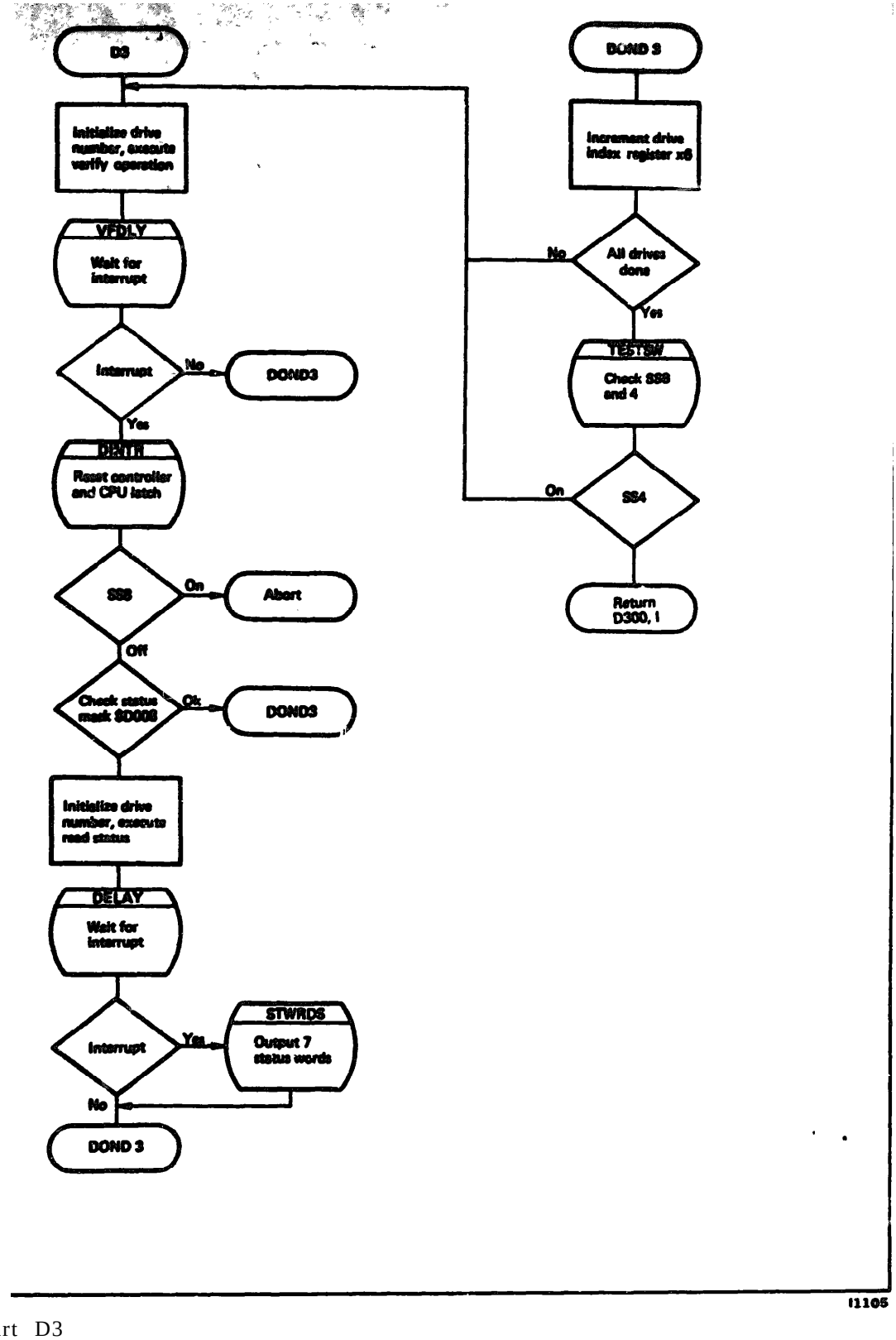
Flowchart D1. (Sheet 4 *of* 4)



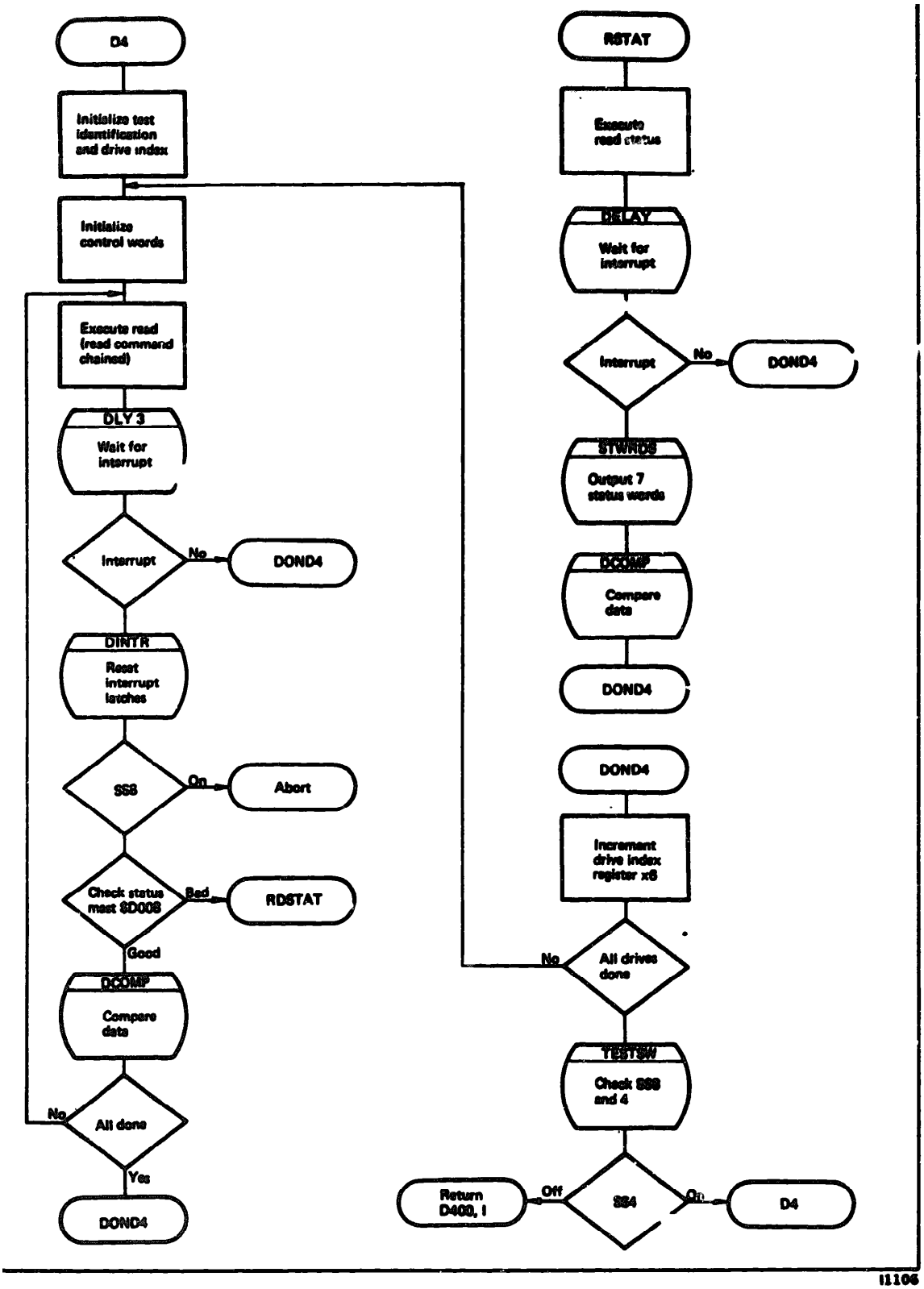
Flowchart D2. (Sheet 1 of 2)



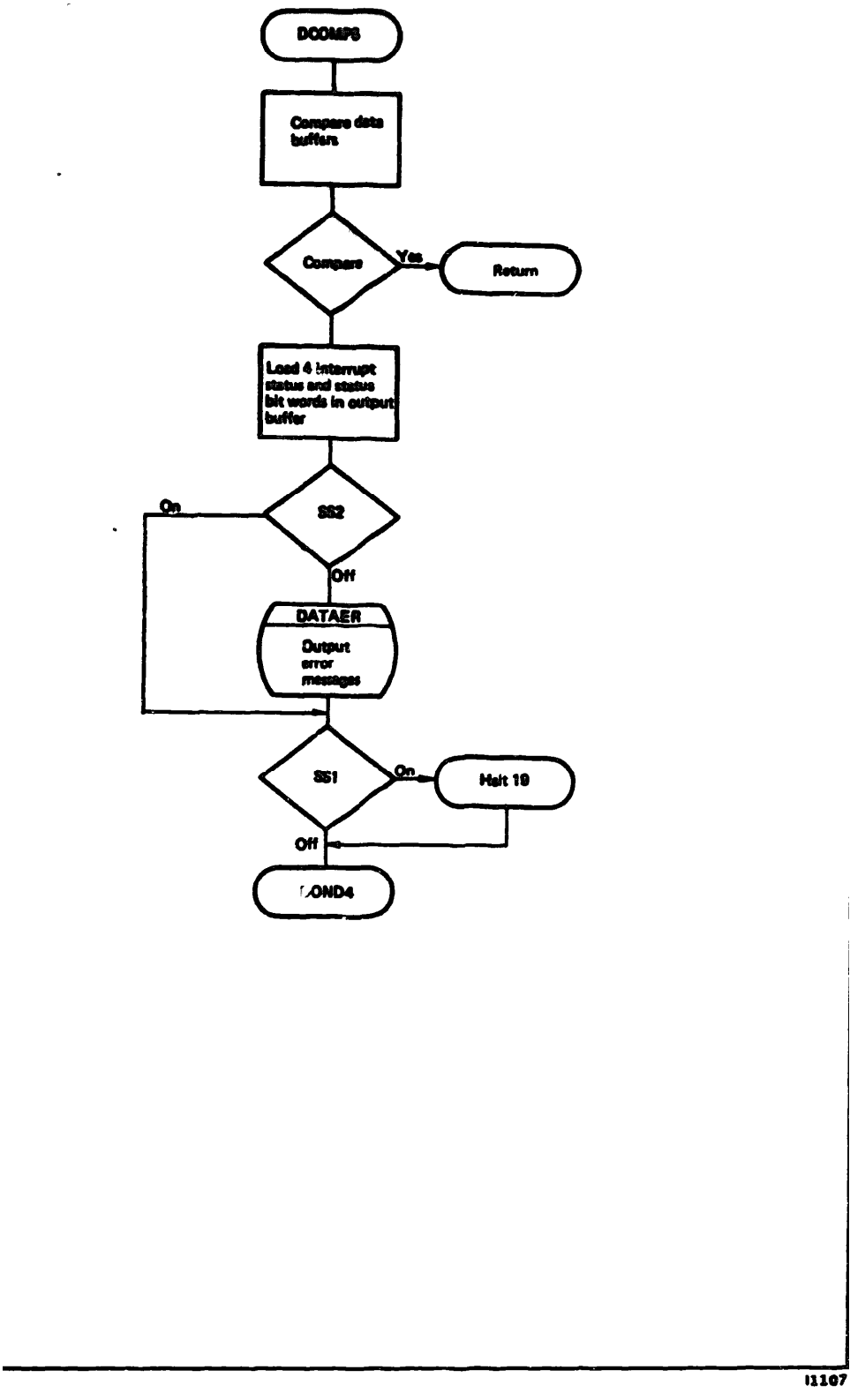
Flowchart D2. (Sheet 2 of 2)



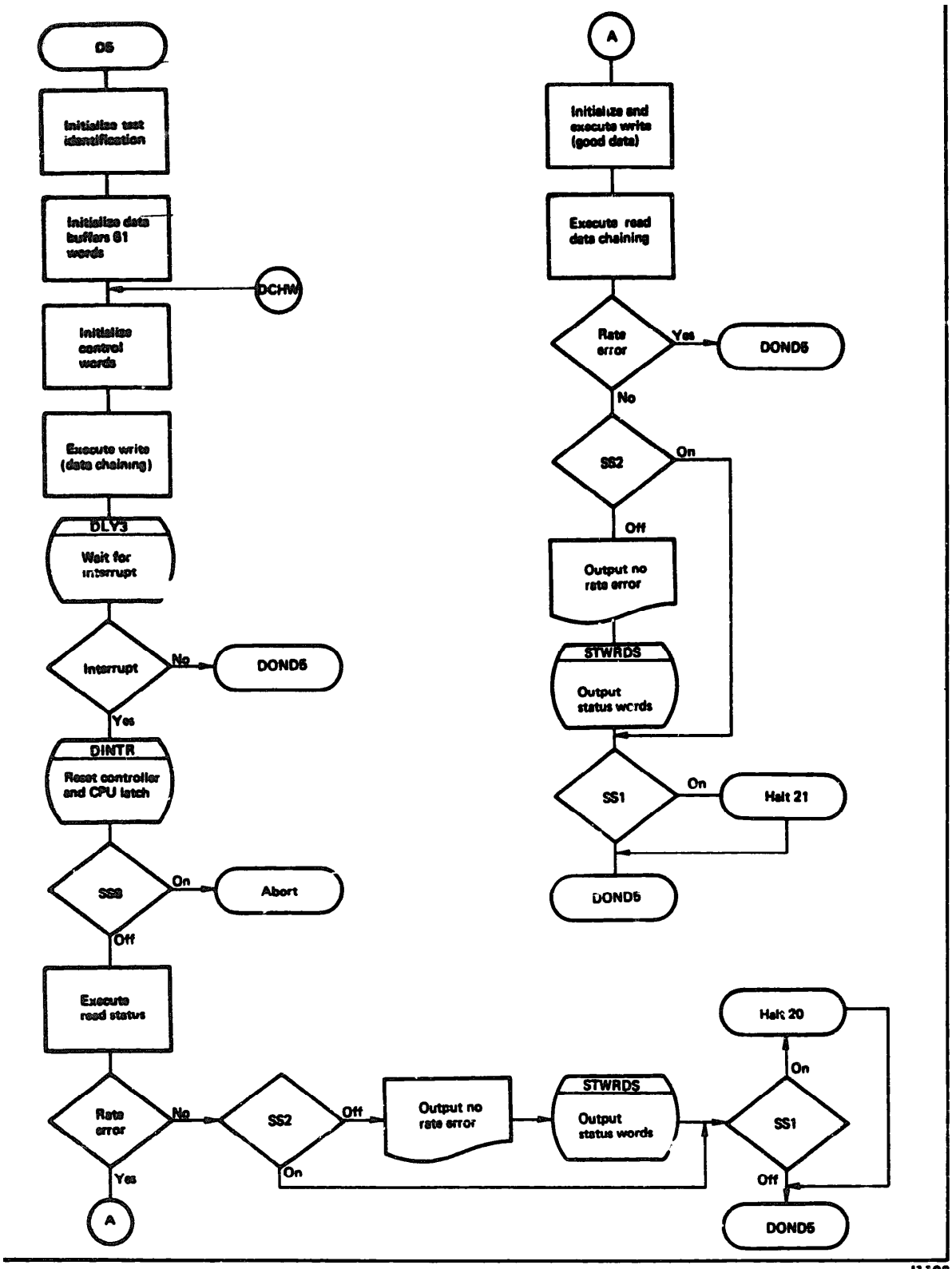
Flowchart D3



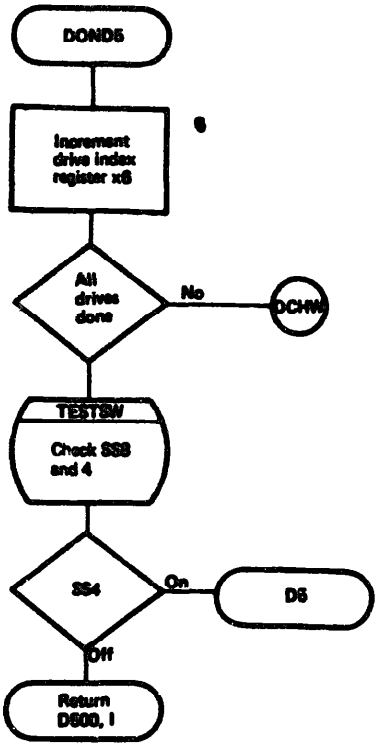
Flowchart D4. (Sheet 1 of 2)



Flowchart D4. (Sheet 2 **of 2)**

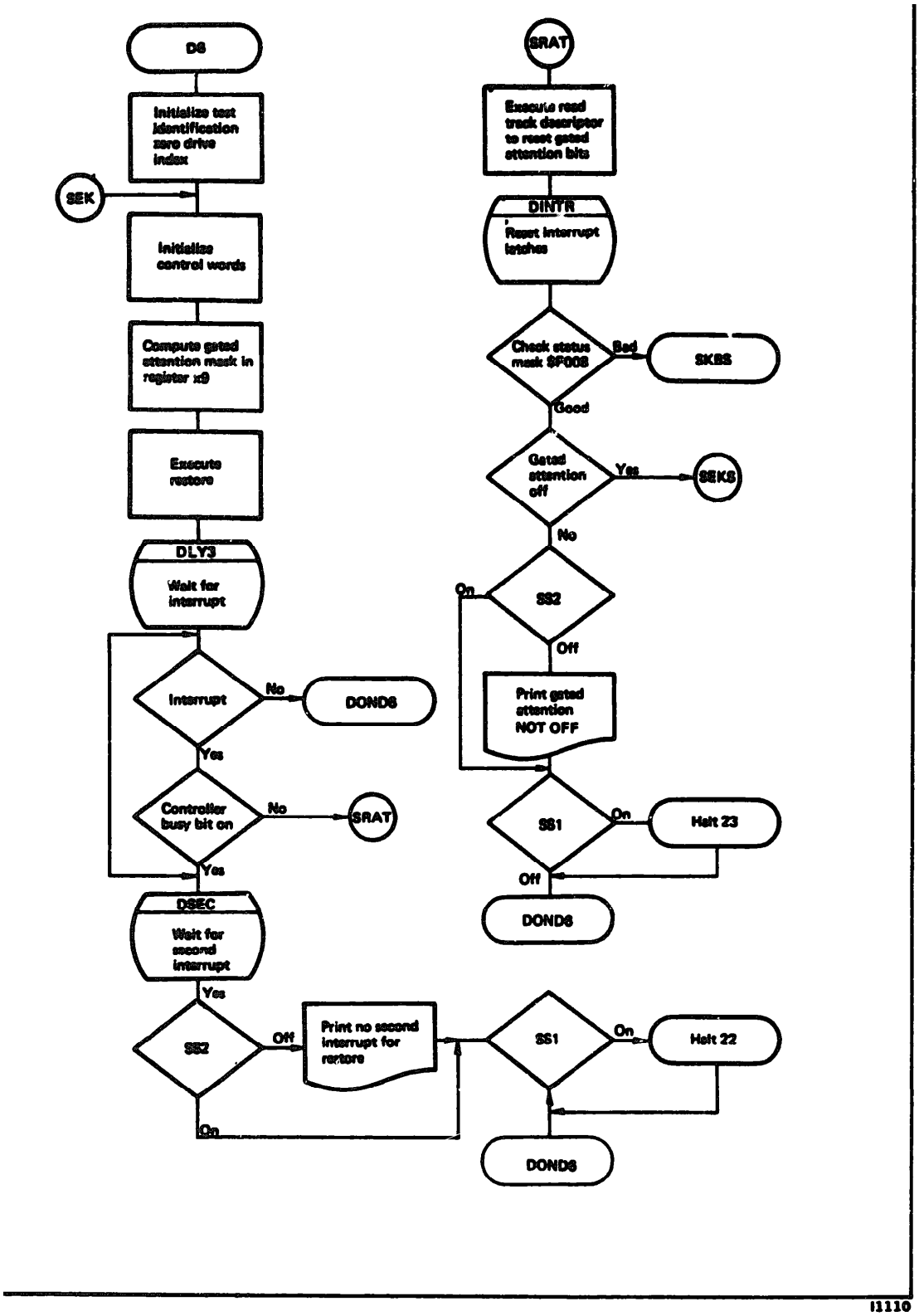


Flowchart D5. (Sheet 1 of 2)

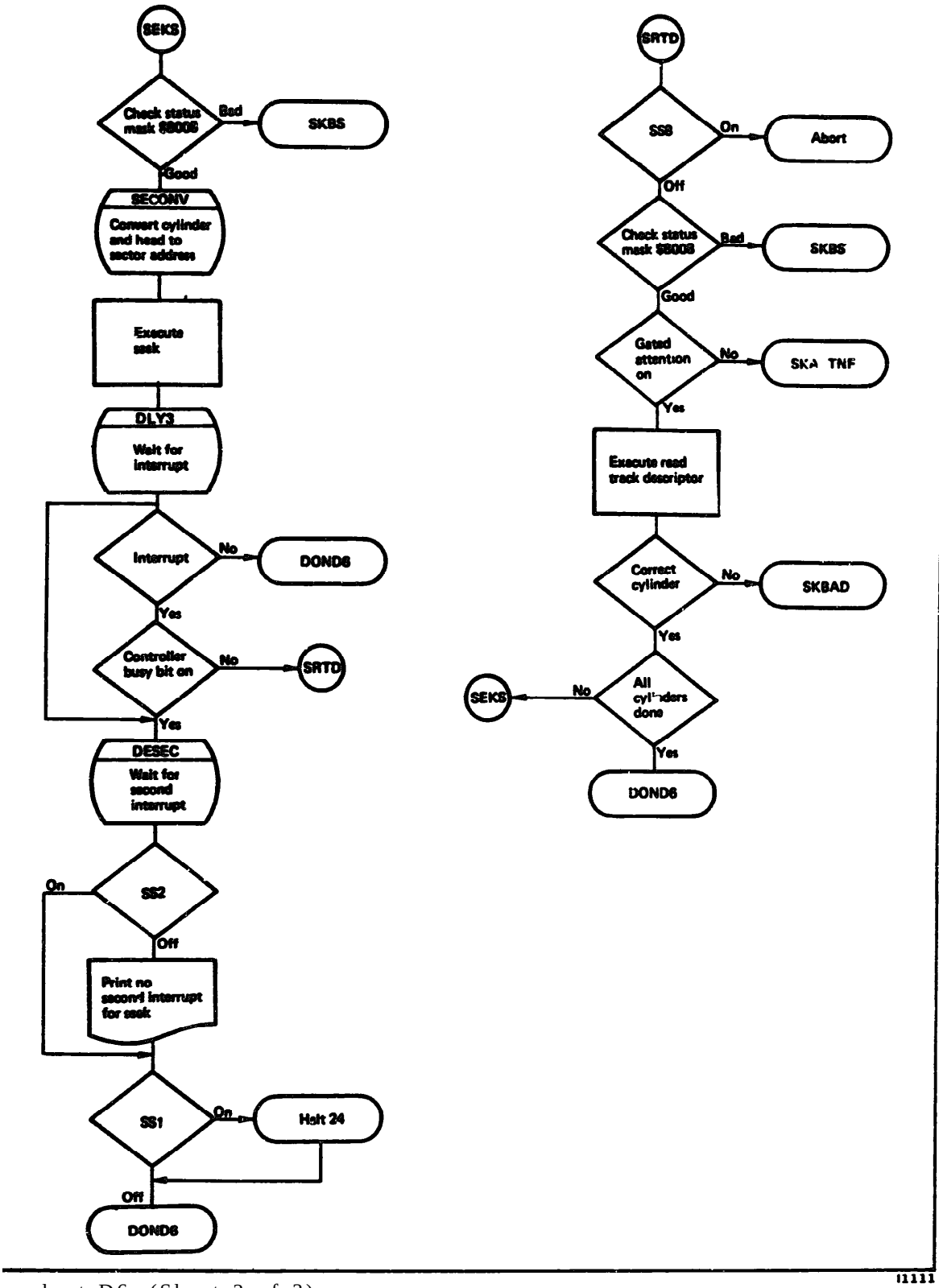


11109

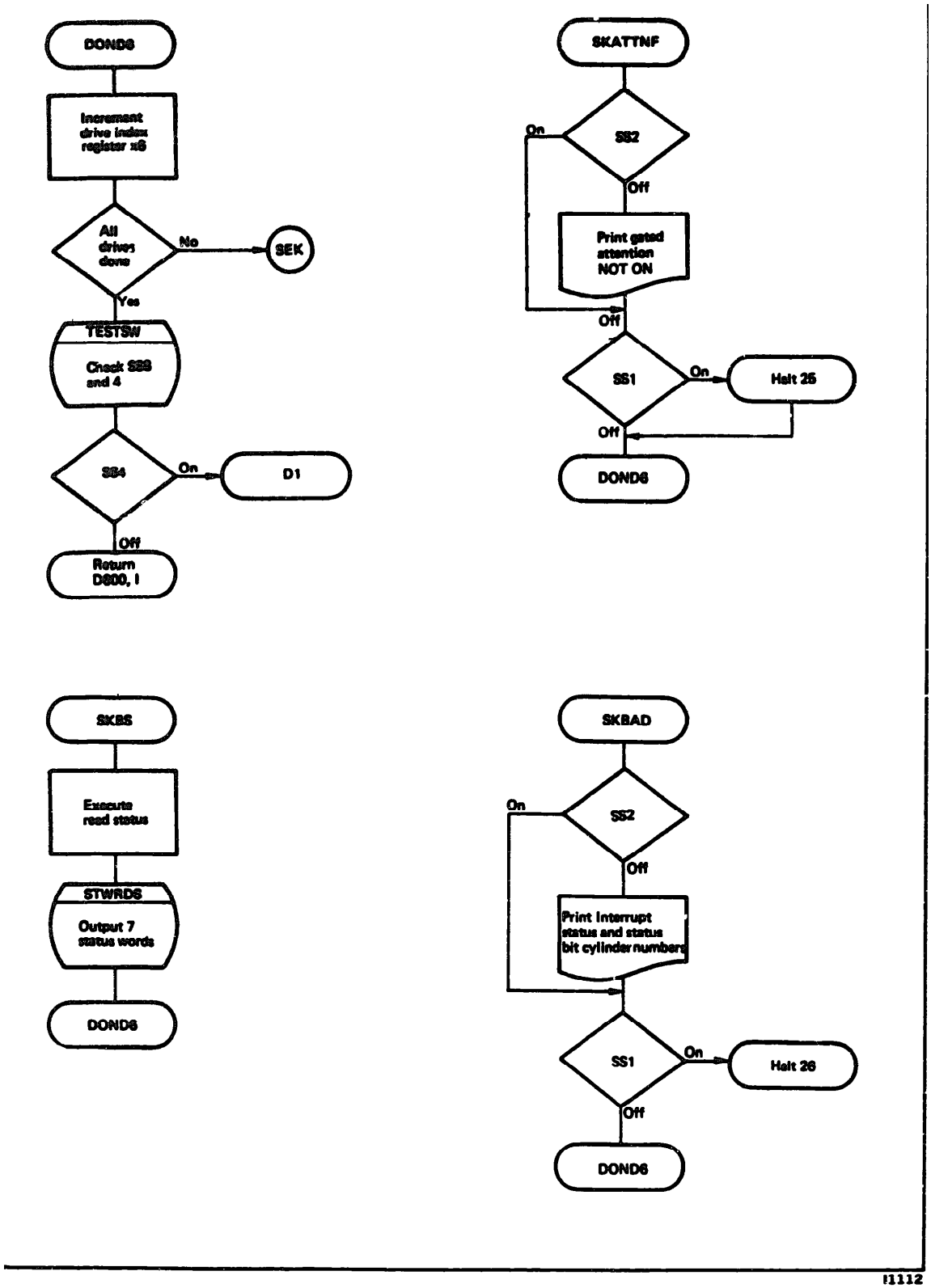
Flowchart D5. (Sheet 2 of 2)



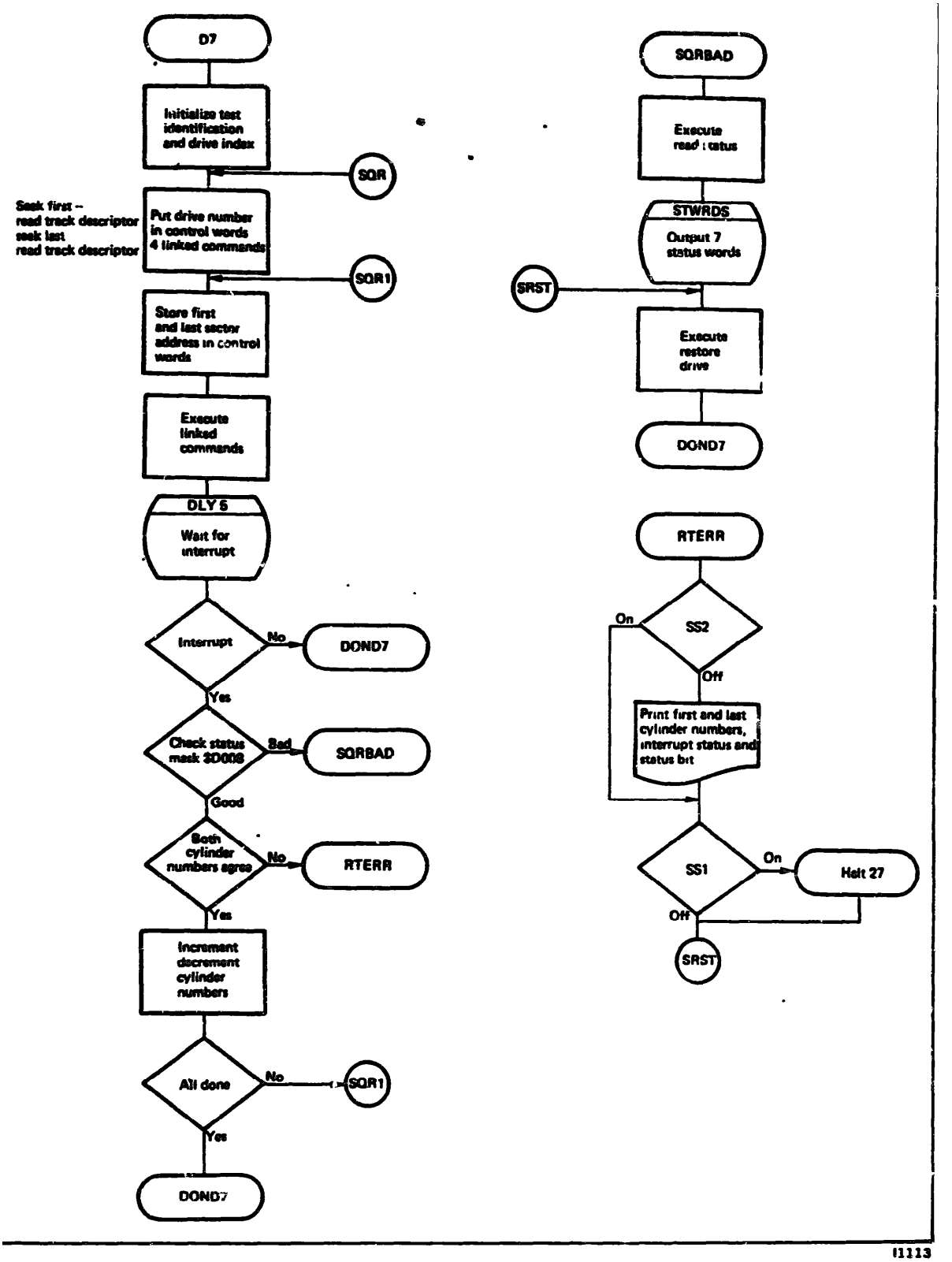
Flowchart D6. (Sheet 1 of 3)



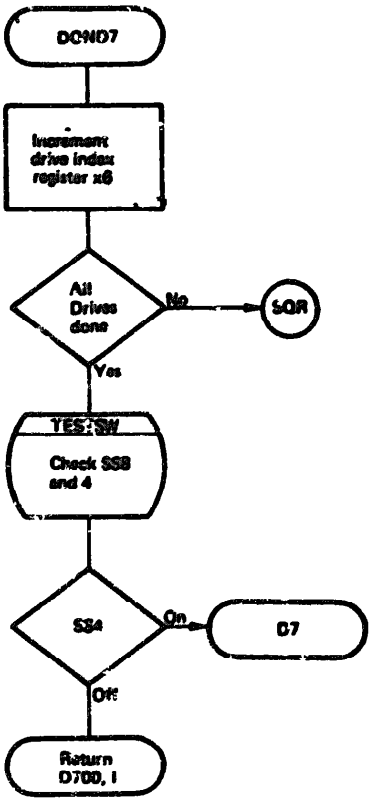
Flowchart D6. (Sheet 2 of 3)



Flowchart D6. (Sheet 3 of 3)

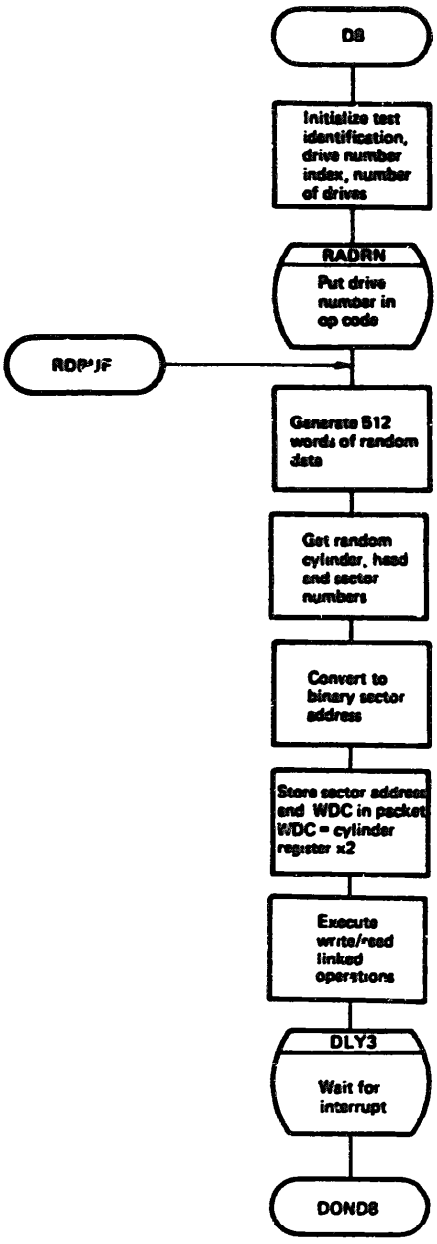


Flowchart D7. **(Sheet 1** of 2)



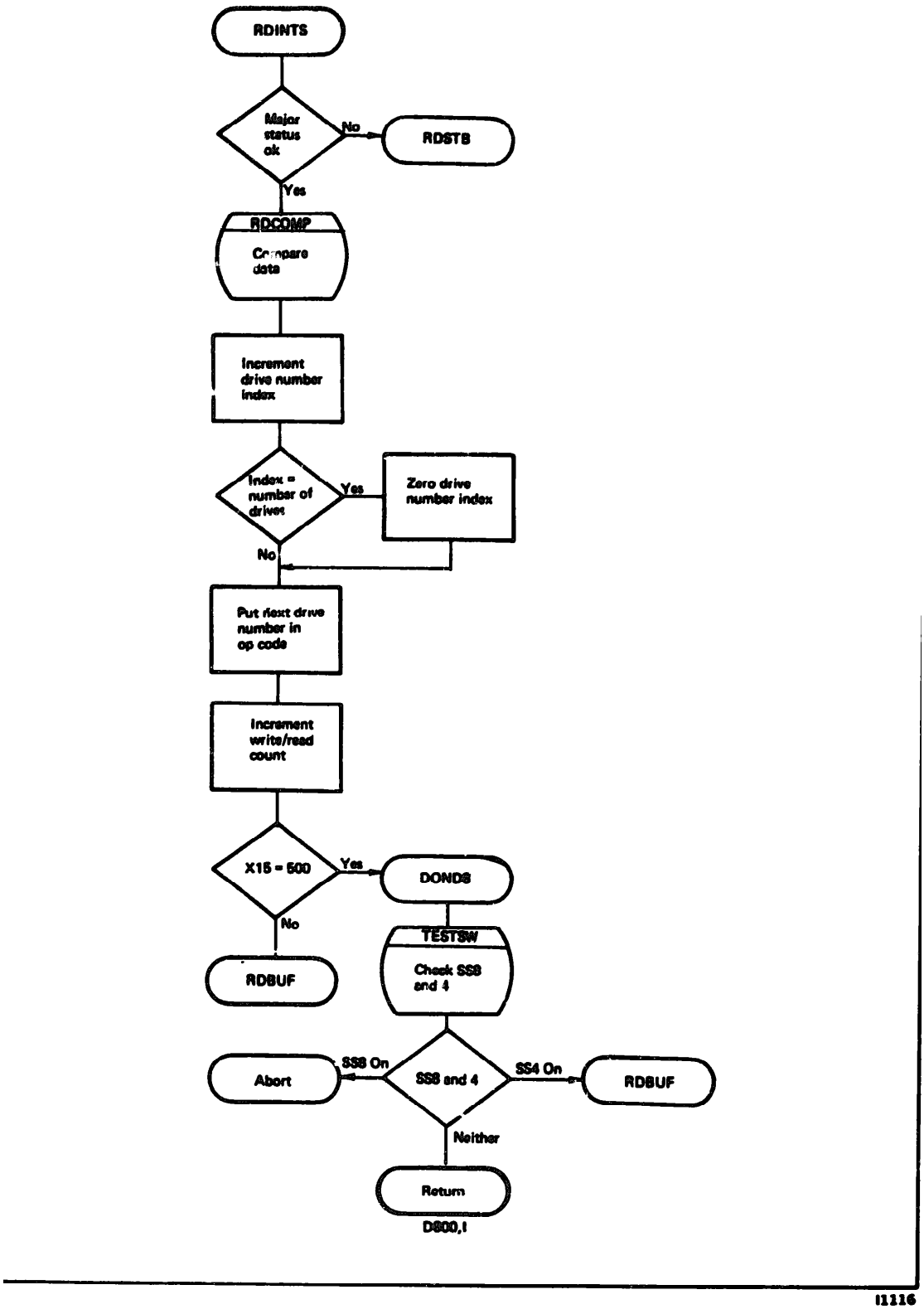
12124

Flowchart D7. (Sheet 2 of 2)

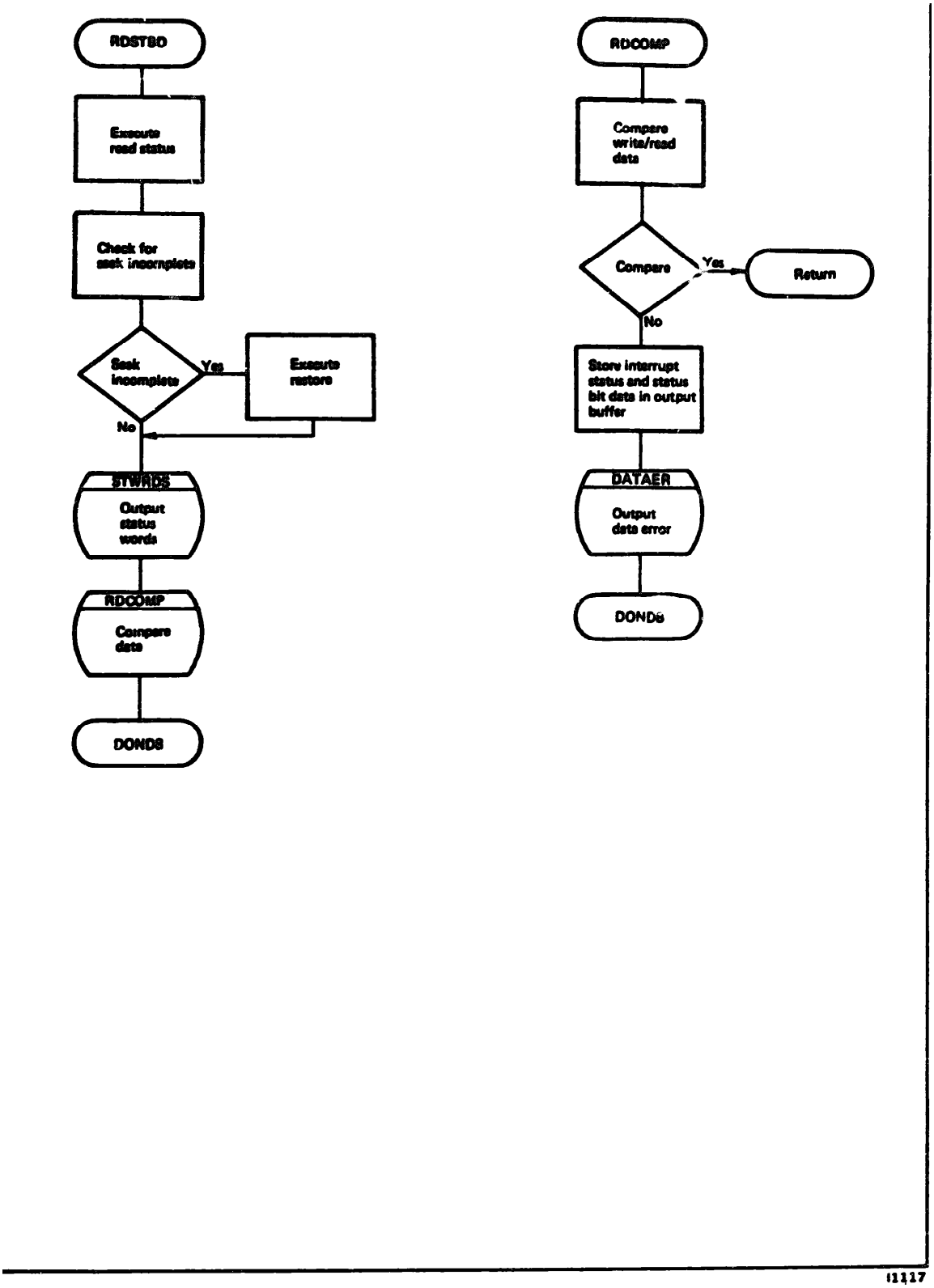


11115

Flowchart D8. (Sheet 1 of 3)



Flowchart **D8. (Sheet** 2 of 3)



Flowchart D8. (Sheet 3 of 3)

APPENDIX C
LOGICS/SCHEMATICS

C.1 GENERAL

This appendix provides the logic diagrams for the PDC and DCI boards, the IOL, PLO, SMX, MUX and PSQ logic cards, and schematics for the Disk Interface Power Supply.

The diagrams are preceded by Figure C-1 and Table C-1. Figure C-1 catalogs the logic symbols used in the LD's and gives their truth tables. Table C-1 provides a listing of the logical function(s) implemented by each IC module.

PDC Board - GTE/IS engineering drawing 300337.

Sheet 1.	Revision page.
Sheet 2.	IC map.
Sheet 2.1.	Board Layout.
Sheet 3.	Mnemonic glossary.
Sheet 4.	Connector pin assignments.
Sheet 5.	Waveshape and timing diagram.
Sheet 5.1.	Microprocessor decode ROM.
Sheet 6.	Main data loop logic.
Sheet 7.	Main data loop (continued).
Sheet 8.	ALU-Code decoding and carry flag.
Sheet 9.	Program counter and control logic.
Sheet 10.	Instruction register and OP-code decode ROMs.
Sheet 11.	I/O data drivers/receivers.
Sheet 12.	I/O bus drivers.
Sheet 13.	File and push down stack.
Sheet 14.	Clock generator, I/O controls and stack counter.
Sheet 15.	Branch condition logic.
Sheet 16.	Branch and I/O Control logic.
Sheet 17.	Interrupt logic.
Sheet 18.	Control memory.
Sheet 19.	Interrupt sync and strobe generator.
Sheet 20.	DOB receivers and DMA data registers.
Sheet 21.	Address, interrupt and ICI patches.
Sheet 22.	CPU command decoding.
Sheet 23.	Command EKO logic.
Sheet 24.	CPU interface control logic.
Sheet 25.	DMA data/address selection and DIB drivers.

Sheet 26. DMA address register and microprocessor data bus gating.

Sheet 27. DMA Sequence logic.

Sheet 28. DMA sequence logic (continued).

DCI Board - GTE/IS engineering drawing 300352.

Sheet 1. Revision page.

Sheet 2. IC map.

Sheet 3. Mnemonic glossary.

Sheet 4. Connector pin assignments.

Sheet 5. J11, J12, J13 receiver/driver logic.

Sheet 6. J3 receiver logic and signal decode.

Sheet 7. J3 receiver logic and signal decode (continued).

Sheet 8. Bit Counter.

Sheet 9. Address Mark detection.

Sheet 10. FIFO register logic.

Sheet 11. Read/write multiplex logic.

Sheet 12. Track format logic.

Sheet 13. Track format logic.

Sheet 14. Sync logic.

Sheet 15. Index/sector detection.

Sheet 16. CRC read/write multiplex logic.

Sheet 17. CRC register.

PSQ Card. GTE/IS engineering drawing 300112.

Sheet 1. Revision page.

Sheet 2. Schematic diagram.

IOL Card. GTE/IS engineering drawing 300332.

Sheet 1. Revision page.

Sheet 2. IC map.

Sheet 3. Mnemonic glossary

Sheet 4. Connector pin assignments.

Sheet 5. Serdes logic.

Sheet 6. Write logic.

Sheet 7. Write logic (continued)

Sheet 8. Write clock generation.

MUX Card. GTE/IS engineering drawing 300333

- **Sheet 1. Revision page.**
- **Sheet 2. IC map and mnemonic glossary.**
- **Sheet 3. Multiplex logic.**
- **Sheet 4. Multiplex logic (continued)**

SMX Card. GTE/IS engineering drawing 300334.

- **Sheet 1. Revision page.**
- **Sheet 2. IC map, mnemonic glossary and connector pin assignments.**
- **Sheet 3. Driver/receiver logic.**

PLO Card. GTE/IS engineering drawing 300364.

- **Sheet 1. Revision page.**
- **Sheet 2. Schematic HC PLO board.**
- **Sheet 3. Schematic HC PLO board (continued).**

Disk Interface Card File Power Supply, PN 350045.

- **Power Supply Schematic, drawing 101701.**
- **Remote Sense Power Supply Schematic, drawing 12-101550.**
- **Overvoltage Protection Device Schematic, drawing 101017.**

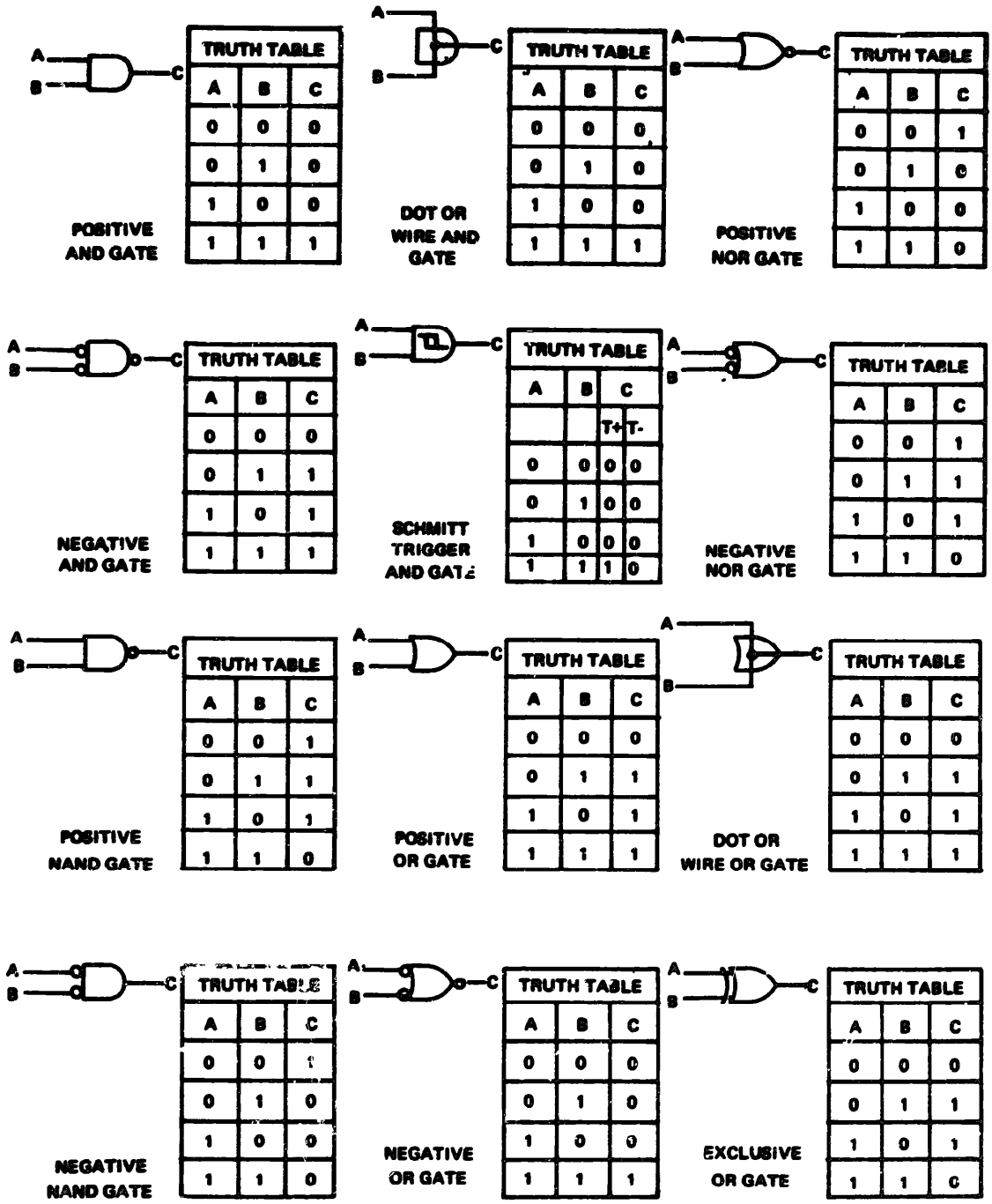


Figure C-1. Logic Symbols used in the Logic Diagrams (Sheet 1 of 3)

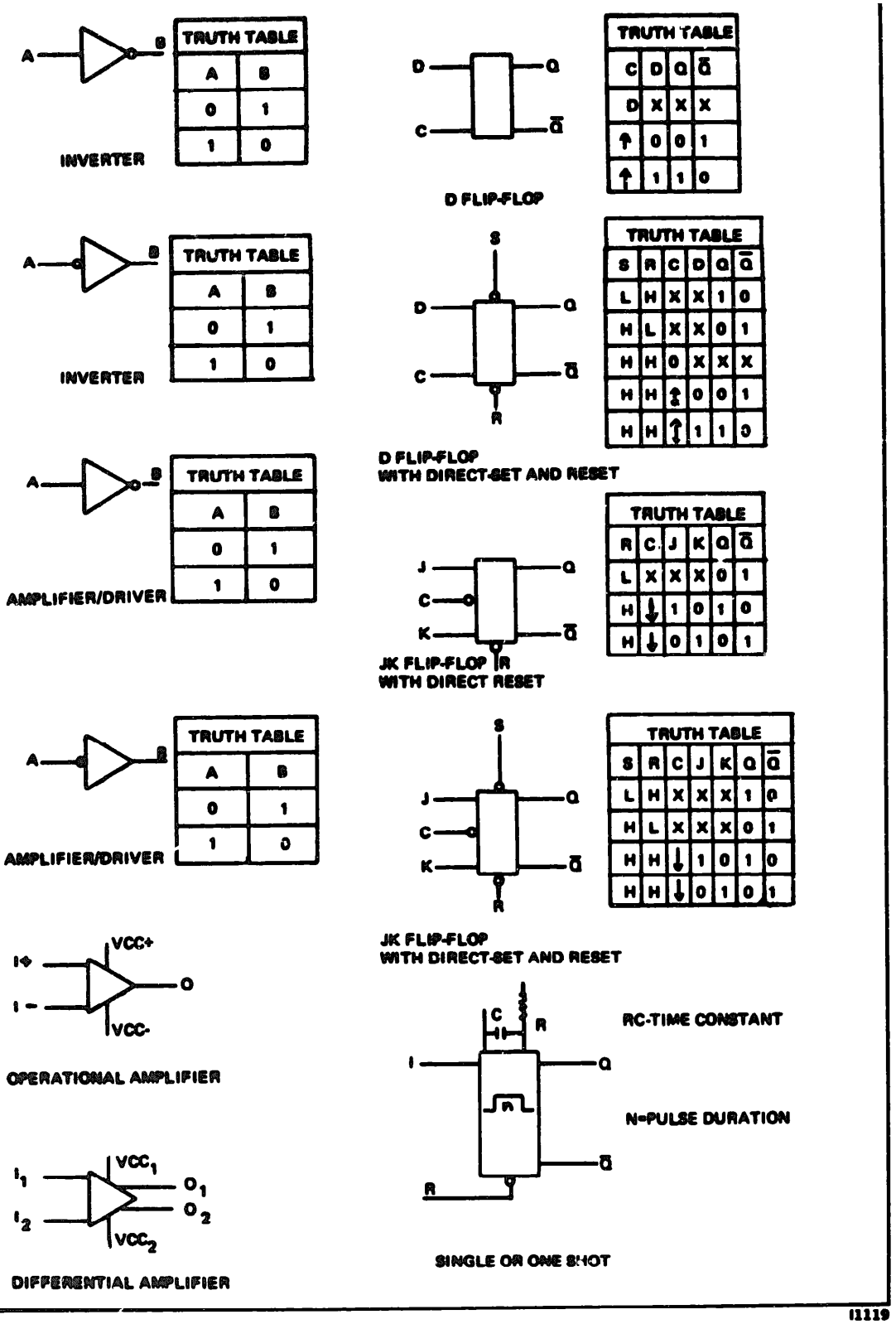
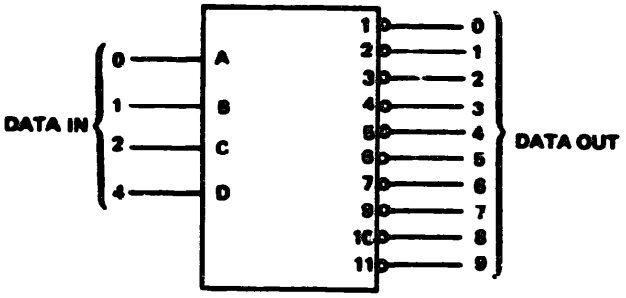


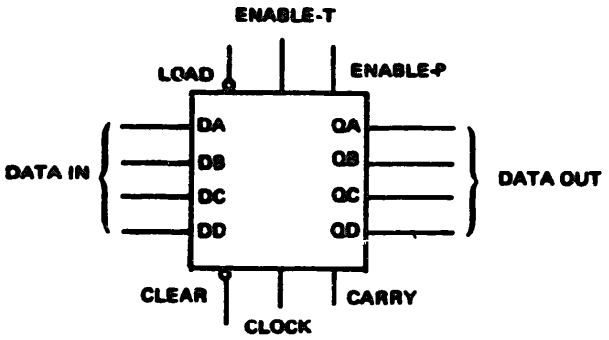
Figure C-1. Logic **Symbols** used in **the Logic** Diagrams (Sheet 2 of 3)



BCD-TO-DECIMAL CONVERTER

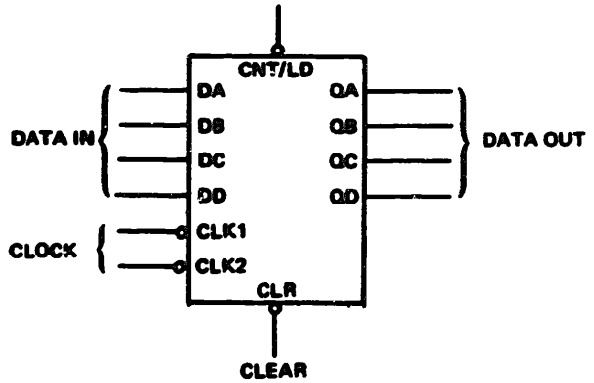
TRUTH TABLE													
D	B	C	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

ALL OTHER COMBINATIONS ARE INVALID



SYNCHRONOUS 4-BIT
BINARY COUNTER

TRUTH TABLE					
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A	CARRY OUT
0	L	L	L	L	L
1	L	L	L	H	L
2	L	L	H	L	L
3	L	L	H	H	L
4	L	H	L	L	L
5	L	H	L	H	L
6	L	H	H	L	L
7	L	H	H	H	L
8	H	L	L	L	L
9	H	L	L	H	L
10	H	L	H	L	L
11	H	L	H	H	L
12	H	H	L	L	L
13	H	H	L	H	L
14	H	H	H	L	L
15	H	H	H	H	H



PRESETTABLE 4-BIT
BINARY COUNTER

EN-P AND EN-T MUST BOTH BE HIGH TO ENABLE THE COUNTER. EN-T HAS THE ADDITIONAL FUNCTION OF ENABLING CARRY OUT.

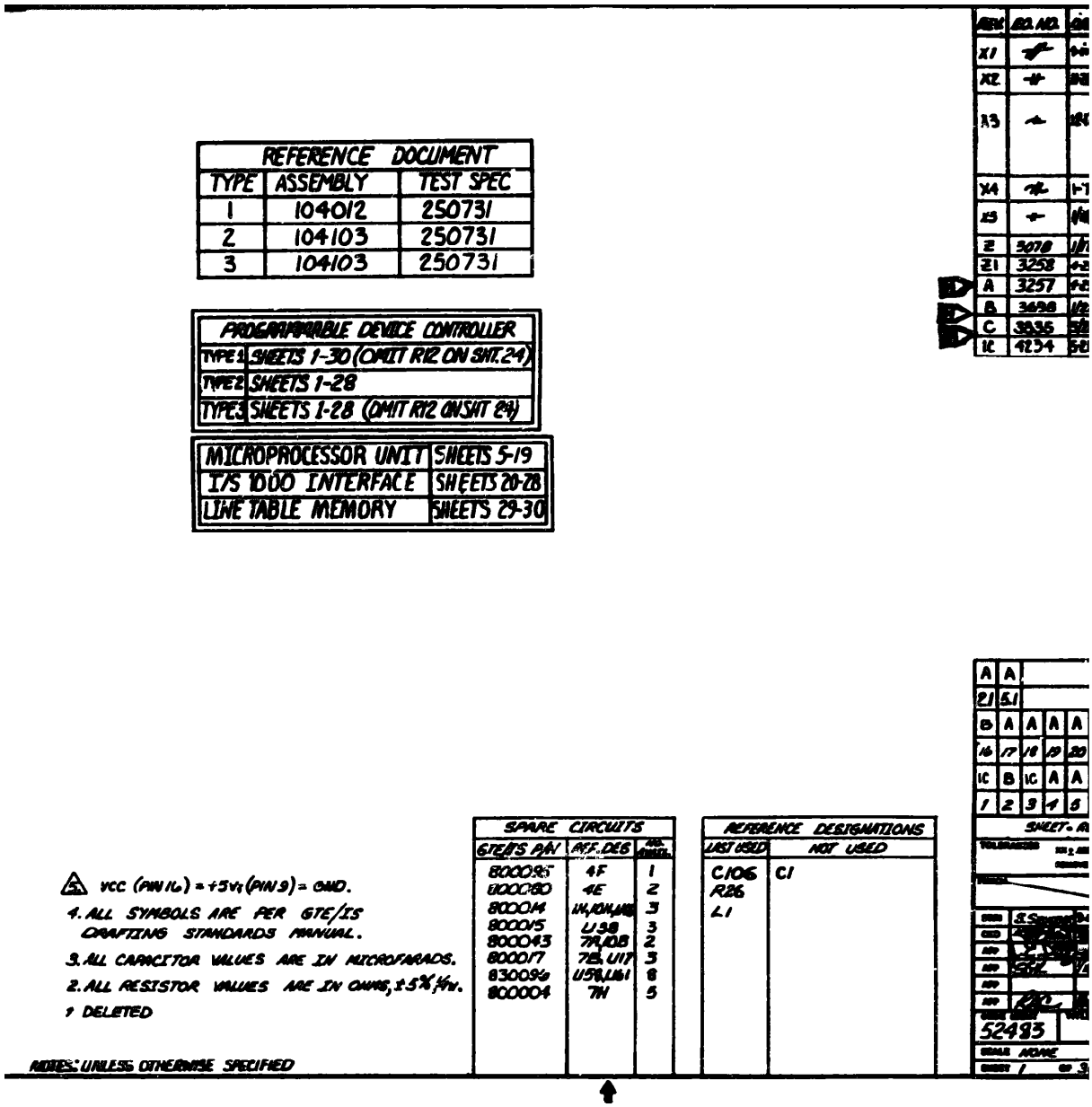
Figure C-1. Logic **Symbols used in the** Logic Diagrams (Sheet 3 of 3)

Table C-1. IC **Module Functional Description (Sheet** 1 of 2)

Module	Description
IC, 93415	1,024-bit RAM, 1k x 1 bit
IC, SN7400	Positive NAND gates
IC, SN7402	Positive NOR gates
IC, SN7404	Positive NAND gates/with open collectors
IC, SN7408	Postive AND gates
IC, SN7410	Hex Inverters
IC, SN7413	Schmitt-trigger Pos NAND gates/inverters
IC, SN7414	Schmitt-trigger Hex inverters
IC, SN7420	Positive NAND gates/inverters
IC, SN7425	Positive NOR gates
IC, SN7430	Positive NAND gates
IC, SN7438	Interface buffer gates
ID, SN7442	BCD-Decimal decoder
IC, SN7462	Expanders
IC, SN7474	Flip-flops, D Type
IC, SN7485	4-bit magnitude comparators
IC, SN7486	Exclusive OR gates
IC, SN7489	64-bit read/write memory
IC, SN74107	JK Flip-flops
IC, SN74108	JK Flip-flops, edge triggered
IC, SN74121N	Monostable Multivibrator
IC, SN74122	Retriggerable monostable multivibrators
IC, SN74151	Multiplexer/data selector
IC, SN74153	4-to-1 Multiplexer/data-selectors
IC, SN74154	4-to-16 demultiplexers/decoders
IC, SN74157	2-to-1 Multiplexer/data selector
IC, SN74161	Synchronous 4-bit counter
IC, SN74175	D-type Flip-flops
IC, SN74181	Arithmetic logic unit
IC, SN74191	Synchronous up/down counter
IC, SN74197	50/30 MHz Presettable Decode/binary counters/latches
IC, SN74198	8-bit shift register

Table C-1. IC **Module Functional Description** (Sheet **2 of 2)**

Module	Description
IC, SN74221	Monostable multivibrator/Schmitt triggered input
IC, SN74298	2-input multiplexers with storage
IC, SN74H00	Positive NAND gates
IC, SN74H01	Hex inverters
IC, SN74H04(A)	Hex inverters with open collectors
IC, SN74H05(A)	Positive NAND gates/inverters
IC, SN74H10	Positive NAND gates/inverters
IC, SN74H11	Positive AND gates
IC, SN74H20	Positive NAND gates
IC, SN74H30	Positive NAND gates
IC, SN74H40	Buffers/Clock Drivers
IC, SN74H53	Expandable gates
IC, SN74H74	D-Type Flip-flop
IC, SN74S00	Positive NAND gate inverter
IC, SN74S37	Interface buffer gates
IC, SN74S38	Interface buffer gates
IC, SN74S124	Voltage controlled oscillator
IC, SN74S138	Decoders/demultiplexers
IC, SN74S153	4-to-1 multiplexers



REFERENCE DOCUMENT		
TYPE	ASSEMBLY	TEST SPEC
1	104012	250731
2	104103	250731
3	104103	250731

PROGRAMMABLE DEVICE CONTROLLER	
TYPE 1	SHEETS 1-30 (OMIT R12 ON SHT. 24)
TYPE 2	SHEETS 1-28
TYPE 3	SHEETS 1-28 (OMIT R12 ON SHT 24)

MICROPROCESSOR UNIT	SHEETS 5-19
I/S 1000 INTERFACE	SHEETS 20-28
LINE TABLE MEMORY	SHEETS 29-30

X1		
X2		
X3		
X4		
X5		
Z	3078	
Z1	3258	
A	3257	
B	3698	
C	3936	
IC	4254	

A	A				
21	5.1				
B	A	A	A	A	
16	17	18	19	20	
IC	B	IC	A	A	
1	2	3	4	5	

SHEET- A

52493

SCALE NONE

⚠5 VCC (PIN 16) = +5V; (PIN 9) = GND.

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.

3. ALL CAPACITOR VALUES ARE IN MICROFARADS.

2. ALL RESISTOR VALUES ARE IN OHMS, ±5% ¼w.

1 DELETED

NOTES: UNLESS OTHERWISE SPECIFIED

SPARE CIRCUITS		
GTE/IS P/N	REF. DES	NO. CKTS.
8000185	4F	1
8000180	4E	2
8000114	U4,U14,U15	3
8000115	U38	3
8000143	7A,10B	2
8000117	7B, U17	3
8300916	U58,U61	8
8000104	7H	5

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C106	C1
R26	
L1	

REV.	E.O. NO.	DATE	DESCRIPTION			
X1	—	[illegible]	INITIAL RELEASE	[illegible]	[illegible]	[illegible]
X2	—	[illegible]	REVISED & REDRAWN	[illegible]	[illegible]	[illegible]
X3	—	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
X4	—	1-7-7[illegible]	CHANGED [illegible]	[illegible]	[illegible]	[illegible]
X5	—	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Z	3078	[illegible]	SPECIAL PILOT REL.	[illegible]	[illegible]	[illegible]
Z1	3258	4-29-75	[illegible]	S.B	[illegible]	[illegible]
A	3257	4-29-75	PRODUCTION REL	S.B	[illegible]	[illegible]
B	3698	[illegible]	SEE E.O.	[illegible]	[illegible]	[illegible]
C	3835	[illegible]	SEE E.O.	[illegible]	[illegible]	[illegible]
1C	4234	6-21-77	SEE E.O.	R.B	[illegible]	[illegible]

REFERENCE DOCUMENT		
TYPE	ASSEMBLY	TEST SPEC
1	104012	250731
2	104103	250731
3	104103	250731

PROGRAMMABLE DEVICE CONTROLLER	
TYPE 1	SHEETS 1-30 (OMIT R12 ON SHT. 24)
TYPE 2	SHEETS 1-28
TYPE 3	SHEETS 1-28 (OMIT R12 ON SHT 24)

MICROPROCESSOR UNIT	SHEETS 5-19
I/S 1000 INTERFACE	SHEETS 20-28
LINE TABLE MEMORY	SHEETS 29-30

REV	A	A													
SH	21	51													
REV	B	A	A	A	A	A	B	A	A	A	B	B	C	A	A
SH	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
REV	1C	B	1C	A	A	A	A	A	C	A	A	A	A	C	A
SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SHEET REVISION STATUS

5. VCC (PIN 16) = +5V; (PIN 8) = GND.

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.

3. ALL CAPACITOR VALUES ARE IN MICROFARADS.

2. ALL RESISTOR VALUES ARE IN OHMS, ±5% 1/4W.

1. DELETED

NOTES: UNLESS OTHERWISE SPECIFIED

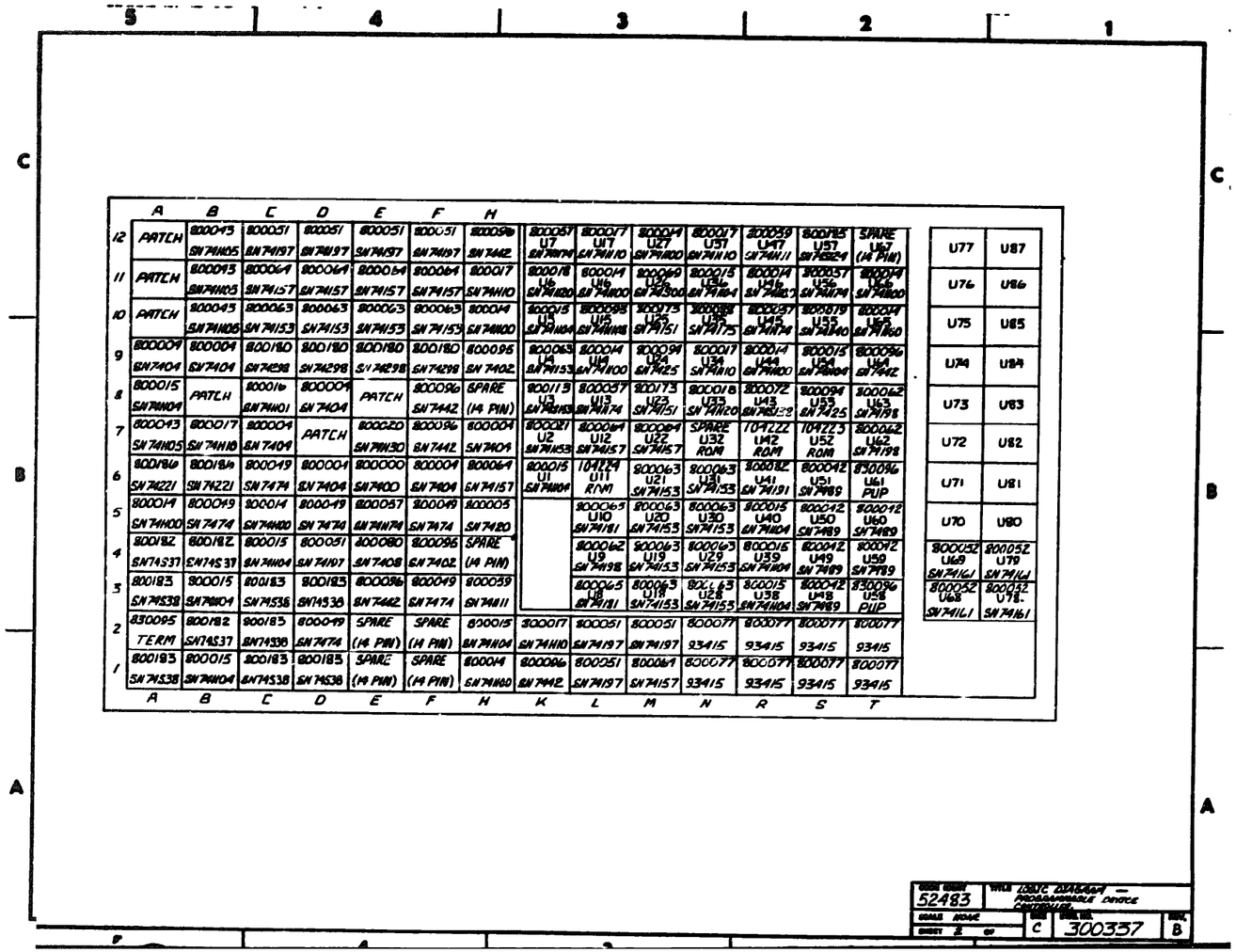
SPARE CIRCUITS		
GTE/IS P/N	REF. DES.	NO. SPARE
800095	4F	1
800080	4E	2
800014	1H,10H,U[illegible]	3
800015	U38	3
800043	7A,10B	2
800017	7B,U17	3
830096	U58,U61	8
800004	7H	5

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C106	C1
R26	
L1	

PROPRIETARY INFORMATION

GTE INFORMATION SYSTEMS

DRN	S. S[illegible]
CODE IDENT	52483
TITLE	LOGIC DIAGRAM PROGRAMMABLE DEVICE CONTROLLER
SCALE	NONE
SHEET	1 OF 30
SIZE	C
DWG NO.	300337
REV	1C


5
4
3
2
1
C
B
A
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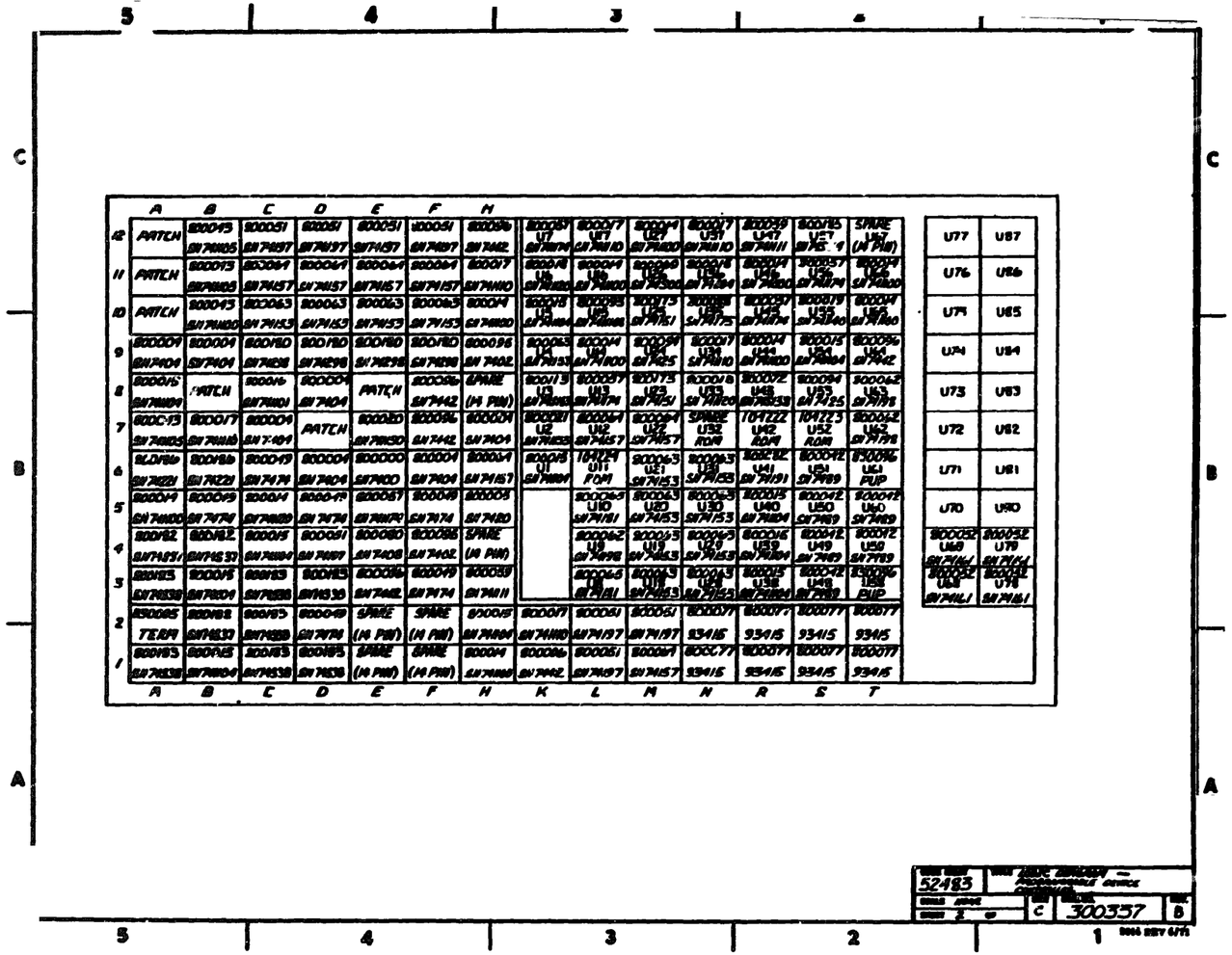
11 PATCH 800043 SN74H05 | 800069 SN74157 | 800069 SN74157 | 800064 SN74157 | 800017 SN74H10
10 PATCH 800043 SN74H05 | 800063 SN74153 | 800063 SN74153 | 800063 SN74153 | 800049 SN7453 | 800049 SN74H00
9 800009 SN7404 | 800004 SN7404 | 800180 SN74298 | 800180 SN74298 | 800180 SN74298 | 800095 SN7402
8 800015 SN74H04 | PATCH 800016 SN74H01 | 800009 SN7404 | PATCH | 800096 SPARE (14 PIN) SN7442
7 800043 SN74H05 | 800017 SN74H10 | 800009 SN7404 | PATCH | 800020 SN74H30 | 800096 SN7442 | 800009 SN7404
6 800180 SN74221 | 800184 SN74221 | 800049 SN7474 | 800004 SN7404 | 800000 SN7400 | 800004 SN7404 | 800064 SN74157
5 800014 SN74H00 | 800049 SN7474 | 800014 SN74H00 | 800049 SN7474 | 800057 SN74H74 | 800049 SN7474 | 800005 SN7420
4 800182 SN74S37 | 800182 SN74S37 | 800015 SN74H04 | 800051 SN7497 | 800080 SN7408 | 800096 SN7402 | SPARE (14 PIN)
3 800183 SN74S38 | 800015 SN74H04 | 800183 SN74S38 | 800183 SN74S38 | 800096 SN7442 | 800049 SN7474 | 800059 SN74H11
2 430095 TERM | 800182 SN74S37 | 800183 SN74S38 | 800049 SN7474 | SPARE (14 PIN) | SPARE (14 PIN) | 800015 SN74H04
1 800183 SN74S38 | 800015 SN74H04 | 800183 SN74S38 | 800183 SN74S38 | SPARE (14 PIN) | SPARE (14 PIN) | 800014 SN74H00
A B C D E F H K L M N R S T
800057 U7 SN74H74 | 800077 U17 SN74H10 | 800044 U27 SN74H20 | 800017 U31 SN74H10 | 800039 U47 SN74H11 | 800183 U57 SN74S24 | SPARE U67 (14 PIN)
800018 U6 SN74H20 | 800014 U16 SN74H00 | 800069 U26 SN74S00 | 800015 U36 SN74H04 | 800014 U46 SN74H00 | 800057 U56 SN74H74 | 800014 U66 SN74H00
800015 U5 SN74H04 | 800088 U15 SN74H08 | 800015 U25 SN74H51 | 800088 U35 SN74H75 | 800057 U45 SN74H74 | 800879 U55 SN74H40 | 800014 U65 SN74H60
800063 U4 SN74H53 | 800014 U14 SN74H00 | 800094 U24 SN7425 | 800017 U34 SN74H10 | 800014 U44 SN74H00 | 800015 U54 SN74H04 | 800096 U64 SN7442
800113 U3 SN74H53 | 800057 U13 SN74H74 | 800173 U23 SN74151 | 800018 U33 SN74H20 | 800072 U43 SN74S288 | 800094 U53 SN7425 | 800062 U63 SN7498
800221 U2 SN74H53 | 800069 U12 SN74S57 | 800069 U22 SN74S57 | SPARE U32 ROM | 104222 U42 ROM | 104223 U52 ROM | 800062 U62 SN7498
800015 U1 SN74H04 | 104224 U11 ROM | 800063 U21 SN74153 | 800063 U31 SN74153 | 800182 U41 SN74191 | 800042 U51 SN7489 | 890096 U61 PUP
800069 U10 SN74181 | 800063 U20 SN74153 | 800063 U30 SN74153 | 800015 U40 SN74H04 | 800042 U50 SN7489 | 800042 U60 SN7489
800062 U9 SN7498 | 800063 U19 SN74153 | 800063 U29 SN74153 | 800015 U39 SN74H04 | 800042 U49 SN7489 | 800042 U59 SN7489
800065 U8 SN74181 | 800063 U18 SN74153 | 820183 U28 SN74155 | 800015 U38 SN74H04 | 800042 U48 SN7489 | 890096 U58 PUP
800017 SN74H10 | 800051 SN7497 | 800051 SN7497 | 800077 93415 | 800077 93415 | 800077 93415 | 800077 93415
800096 SN7442 | 800051 SN7497 | 800069 SN74157 | 800077 93415 | 800077 93415 | 800077 93415 | 800077 93415
U77 U87
U76 U86
U75 U85
U74 U84
U73 U83
U72 U82
U71 U81
U70 U80
800052 U69 SN74161 | 800052 U79 SN74161
800052 U68 SN74161 | 800052 U78 SN74161
52483
TITLE LOGIC DIAGRAM — PROGRAMMABLE DEVICE CONTROLLER
SCALE NONE
SHEET 2 OF
DWG. NO. 300337
REV. C
REV. B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11 PATCH 800013 SN74LS05 800047 SN74S57 800047 SN74S57 800047 SN74S57 800017 SN74S10 800018 U6 SN74S00 800049 U16 SN74S00 800049 U26 SN74S00 800018 U36 SN74S04 800019 U46 SN74S11 800057 U56 SN74LS04 800019 U66 SN74S11
10 PATCH 800043 SN74LS00 800063 SN74LS53 800063 SN74LS53 800063 SN74LS53 800044 SN74S00 800018 U5 SN74S04 800018 U15 SN74S04 800073 U25 SN74S51 800018 U35 SN74S04 800057 U45 SN74LS04 800019 U55 SN74S40 800014 U65 SN7400
9 800004 SN7404 800004 SN7404 800180 SN74S18 800180 SN74S18 800180 SN74S18 800096 SN7402 800063 U4 SN74S53 800044 U14 SN74S00 800039 U24 SN74S51 800017 U34 SN74S10 800014 U44 SN74S00 800015 U54 SN74LS04 800096 U64 SN7402
8 800015 SN74LS04 PATCH 800046 SN74S04 PATCH 800096 SN7402 SPARE (14 PIN) 800073 U3 SN74S08 800087 U13 SN7474 800073 U23 SN74S51 800078 U33 SN74S20 800072 U43 SN74LS38 800094 U53 SN74S125 800062 U63 SN7486
7 800015 SN74LS04 800017 SN74S10 800004 SN7404 PATCH 800180 SN74S18 800096 SN7402 800004 SN7404 800087 U2 SN74LS32 800044 U12 SN74S00 800004 U22 SN7404 SPARE U32 ROM 1024222 U42 ROM 1024223 U52 ROM 800062 U62 SN7486
6 SLDR6V SN74221 800186 SN74221 800049 SN7474 800004 SN7404 800000 SN7400 800004 SN7404 800051 SN74S57 800018 U1 SN74S04 1024224 U11 PDM 800043 U21 SN74LS53 800053 U31 SN74S53 1024222 U41 SN74S91 800042 U51 SN7489 800096 U61 PUP
5 800049 SN7400 800049 SN7474 800044 SN7400 800049 SN7474 800067 SN74S10 800049 SN7474 800053 SN7420 800043 U10 SN74S51 800043 U20 SN74S53 800053 U30 SN74S53 800015 U40 SN74S04 800042 U50 SN7489 800042 U60 SN7489
4 800182 SN74LS32 800182 SN74LS32 800015 SN74S04 800091 SN7407 800180 SN74S18 800186 SN74221 SPARE (14 PIN) 800062 U9 SN74S86 800043 U19 SN74LS53 800043 U29 SN74LS53 800016 U39 SN74S04 800042 U49 SN7489 800042 U59 SN7489
3 800185 SN74LS38 800015 SN74S04 800183 SN74LS38 800180 SN74S18 800186 SN74221 800049 SN7474 800111 SN74S11 800045 U8 SN74S51 800043 U18 SN74LS53 800043 U28 SN74LS53 800015 U38 SN74S04 800042 U48 SN7489 800096 U58 PUP
2 850085 SN74LS32 800182 SN74LS32 800165 SN74S38 800049 SN7474 SPARE (14 PIN) SPARE (14 PIN) 800015 SN74S04 800077 SN74S10 800061 SN74S74 800061 SN74S74 800077 SN74S10 800077 SN74S10 800077 SN74S10
1 TE.DR SN74LS32 800185 SN74LS38 800185 SN74LS38 800185 SN74LS38 800185 SN74LS38 800185 SN74LS38 800185 SN74LS38 800049 SN7474 SPARE (14 PIN) SPARE (14 PIN) 800014 SN74S00 800086 SN7402 800061 SN74S74 800049 SN7474 800077 SN74S10 93415 93415 93415 93415
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U76 U86
U75 U85
U74 U84
U73 U83
U72 U82
U71 U81
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52483
C
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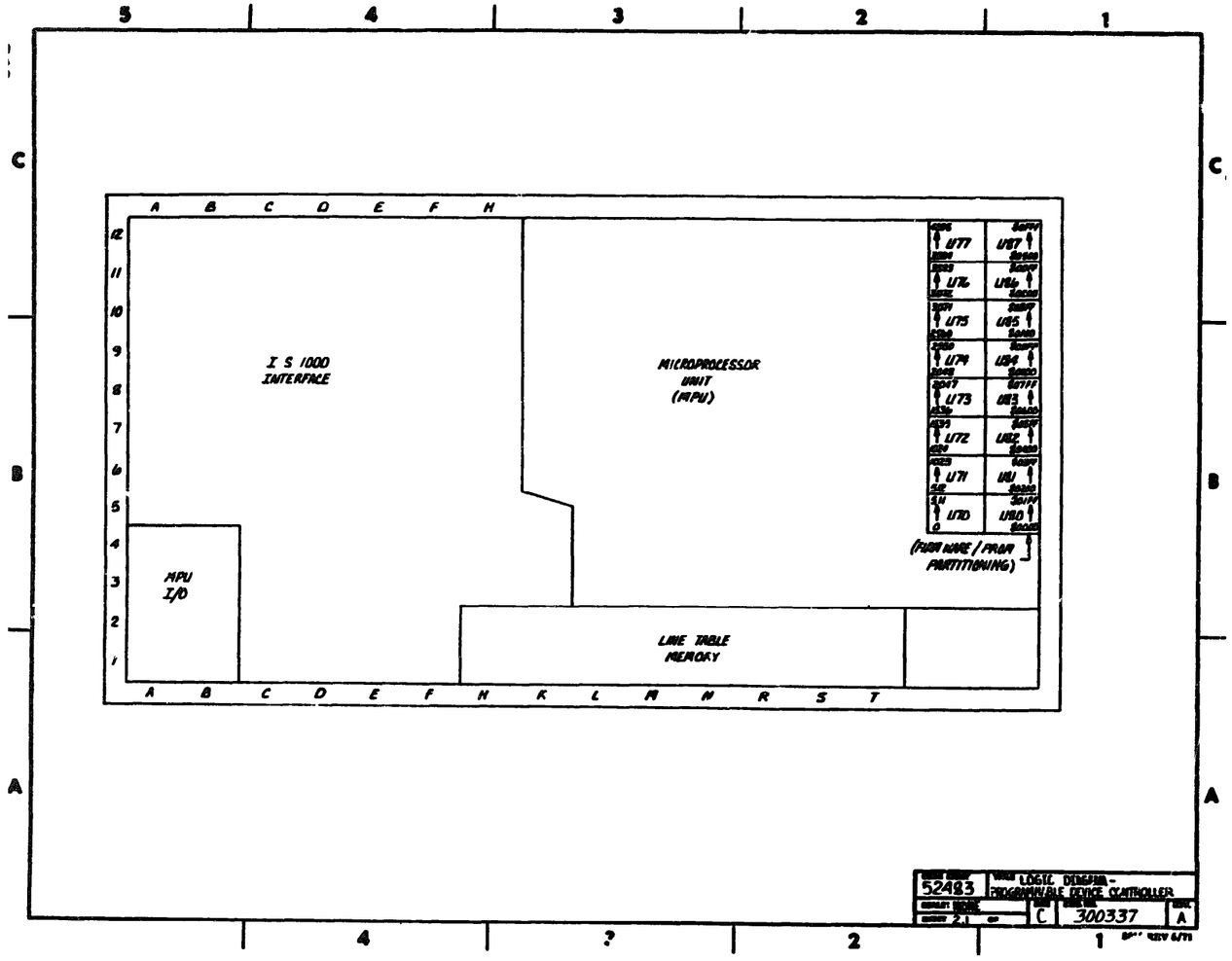
I S 1000
INTERFACE
MICROPROCESSOR
UNIT
(MPU)
MPU
I/O
LINE TABLE
MEMORY
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U75
U74
U73
U72
U71
U70
U67
U66
U65
U64
U63
U62
U61
U60
(FOR MORE / FROM
PARTITIONING)
52483
LOGIC DIAGRAM -
PROGRAMMABLE DEVICE CONTROLLER
C
300337
A

MNEMONIC GLOSSARY

MNEMONIC	SOURCE	DEFINITION
1(0-7)	7A1	ACCUMULATOR OUTPUT
ACC(0-1)	7A3	ACCUMULATOR CONTROL
AD(0-9)	29C1	MEMORY ADDRESS LINES (0-9)
ADA(0-5)	21B3	PATCH SELECTED DEVICE ADDRESS
ADR1X	22B5	DECODED ADDRESSES 16 THRU 31
ADR2X	22B8	DECODED ADDRESSES 32 THRU 47
ADR3X	22B5	[illegible]
ALU(0-5)	[illegible]	ACCUMULATOR D-RAM ADDRESS
ALU(0-7)	28B, 70A	ALU OUTPUT
ARINC	22C1	ADDRESS REGISTER INCREMENT
ARL(6-7)	26	ADDRESS REGISTER LOWER BITS (0-7)
ARLLD	22C1	ADDRESS REGISTER LOWER LOAD
ARUD(7)	26	ADDRESS REGISTER UPPER BITS (0-7)
ARUDD	22C1	ADDRESS REGISTER UPPER LOAD
AREQ	15B5	ACCUMULATOR IS ZERO
A2L	15C4	ACCUMULATOR LOWER FOUR BITS ARE ZERO
A2U	15C4	ACCUMULATOR UPPER FOUR BITS ARE ZERO
BFA	16B4	BRANCH FLIP-FLOP CONTROL INPUT
BFF	16B2	BRANCH (AND 2 CYCLE TIME INTERRUPT-FLIP
BRDY	14B1	BUS READY I/Ø.
BWRLD	30B4	BYTE NUMBER REGISTER LOAD
BUSYEN	27B3	BUSY ENABLE
CFF	8C1	CARRY FLAG FLIP-FLOP
CFTH	8C4	CARRY FLAG INPUT SELECTED
CIN3	7B4	CARRY INTO ALU BIT 3
CIN7	7C2	CARRY INTO ALU BIT 7
CLI	14C1	MASTER CLOCK PHASE 1
CL2	14C1	MASTER CLOCK PHASE 2
CMDFLG	24A4	COMMAND FLAG
COUT	7B5	CARRY OUT OF ALU
CPUISL	22B1	CPU INTERFACE SELECT
CRT(1-4)	15A9	CRITERIA SELECTED FOR CONDITIONS
CUP	8B4	CARRY FLAG UPDATE
CUPCK	8B3	CARRY FLAG UPDATE CLOCK
DA(0-7)	12	DEVICE ADDRESS LINES
DACC	10A1	DECODE ACCUMULATOR COMMAND
DAB0-DA05	21C5	DEVICE ADDRESS BUS, LINES 00-05, CPU BUS
DAI(5-7)	22C3	DEVICE ADDRESS FOR INTERRUPTS, BITS 5-7
DALSD-3	8A1	DECODE ALU FUNCTION CONTROL
DCIN7	8B2	CARRY IN TO BIT 7
DALM	8B2	DECODE ALU MODE
DDDL	10B1	DECODE DATA DIRECTION LINE
DDL	14A1	DIR. DIRECTION LINE I/Ø.
DDIBC	10B1	DECODE DIO CONDITIONAL INSTRUCTION
DEPADR	21B3	DECODED ADDRESS
DFWE	10B1	DECODE FILE WRITE ENABLE

MNEMONIC GLOSSARY

MNEMONIC	SOURCE	DEFINITION
DIB(0-15)	26	DEVICE TO CPU BUS, LINES 00-15, CPU BUS
DIBOUT	25C4	DEVICE INPUT BUS OUTPUT ENABLE
DINI	14C3	DECODE INI INSTRUCTION
DIØ	10B1	DECODE I/Ø INSTRUCTION
DIOI	14C4	DECODE I ØI INSTRUCTION
DIWE	10A2	DECODE INPUT/OUTPUT REGISTER WRITE ENABLE
DMAADØ	27B3	DMA ADDRESS GATE
DMADTØ	27A3	DMA DATA GATE
DMACW1	26A3	DMA CLEAR-WRITE RIGHT BYTE
DMALD	27A3	DMA LOAD
DMACW0	28A3	DMA CLEAR-WRITE LEFT BYTE
DMAP(0-3)	28B	DMA PRIORITY LINES 1 THRU 3
DMASEQ	28B4	DMA SEQUENCE
DMAST	28A3	DMA STROBE
DMCW93	27A1	DMA CLEAR-WRITE ONE-SHOT OUTPUT
DMAMS	28B3	DMA MEMORY START
DMAMS6	27A4	DMA MEMORY START
DMØS	28C5	READ DATA ALMOST READY
DMØSDL	28C4	DMØS DELAYED
DMPIN	29B2	DMA PRIORITY INPUT
DMPOUT	29B2	DMA PRIORITY OUTPUT
DMRQ	27C3	DMA REQUEST
DMRQ93	27B3	DMA REQUEST ONE-SHOT OUTPUT
DMRS	27B2	DMA RESPONSE
DMRSEN	27B3	DMA RESPONSE ENABLE
DMRS93	27B4	DMA RESPONSE ONE-SHOT OUTPUT
DMUX(0-1)	10A1	DECODE MUX A LINE SELECT
DMUB(0-1)	10A1	DECODE MUX B LINE SELECT
DOB(00-15)	20	DATA OUTPUT BUS, LINES 00-15 (CPU BUS)
DPCE	10B1	DECODE PROGRAM COUNTER ENABLE
DPLWE	10B1	DECODE PROGRAM COUNTER LOWER WRITE ENABLE
DPØP	14C3	DECODE P&P INSTRUCTION
DPUWE	10B1	DECODE PROGRAM COUNTER UPPER WRITE ENABLE
DRDI-IN	24B3	DMA CLEAR-WRITE DELAYED
DRIDSL	24B1	DATA REGISTER INPUT DATA SELECT
DRLLD	22C1	DATA REGISTER LOWER LOAD
DRULD	22C1	DATA REGISTER UPPER LOAD
DUNCD	10B1	DECODE UNCONDITIONAL TEST CONDITION DECODED
DWAIT	14C3	DECODE WAIT INSTRUCTION
EDF	22A3	EXECUTE DEVICE FUNCTION
EDFINI	22A2	EDF INITIALIZE CPU I/Ø COMMAND
EDFRST	22A2	EDF RESET
EDFSTR	22A2	EDF START
EKØ	23B1	ECHØ
ENFF	17C2	INTERRUPT ENABLE FLIP-FLOP
ENI	17C3	ENABLE INTERRUPT
EXTINT	12B4	EXTERNAL INTERRUPT MICROPROCESSOR

MNEMONIC GLOSSARY

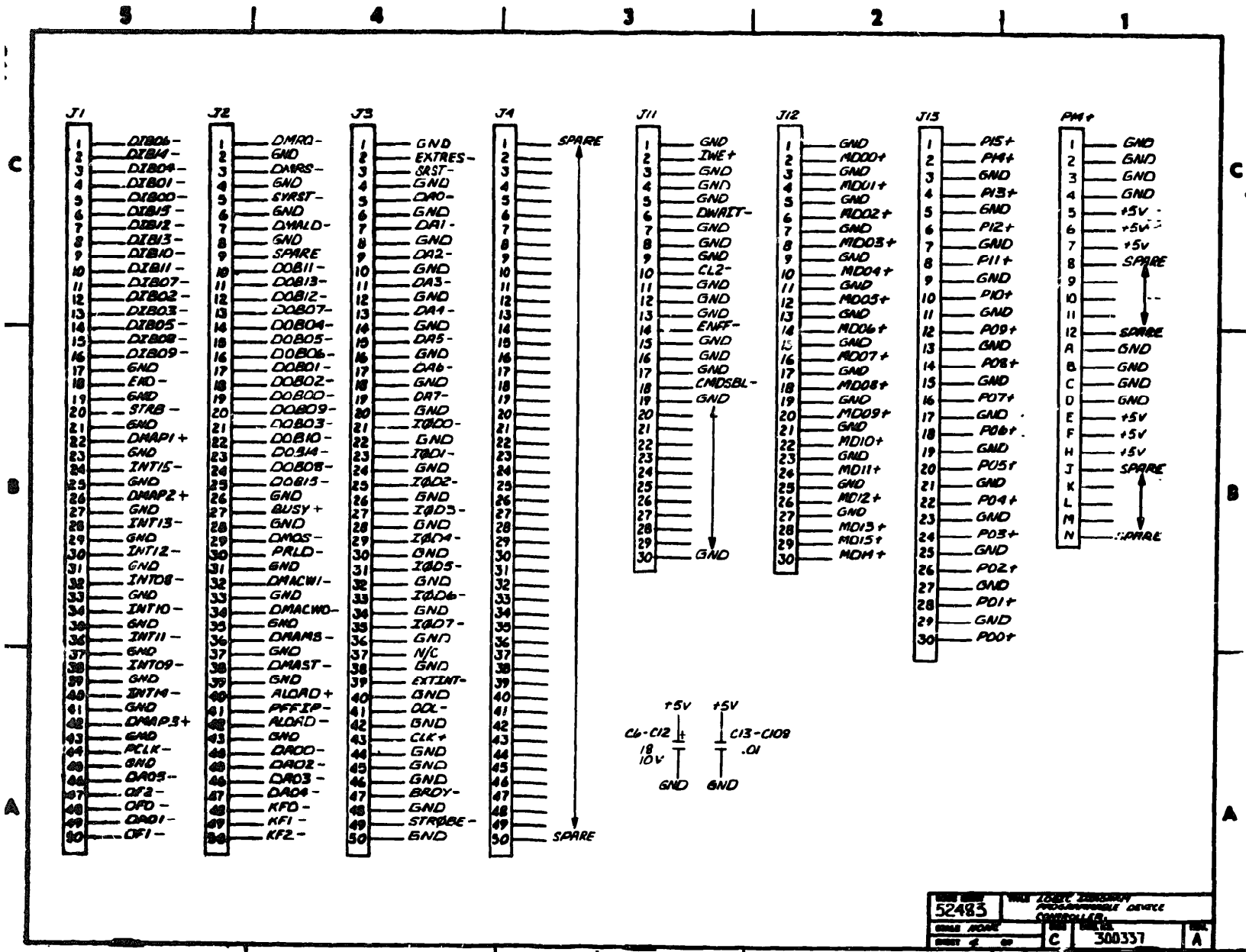
MNEMONICS	SOURCE	DEFINITION
EXTRES	24B3	EXTERNAL MICROPROCESSOR RESET
F(0-7)	13	FILE OUTPUT
FME	14A4	FILE MEMORY ENABLE
FSTCLK	14B1	FAST CLOCK
FWE	13C3	FILE WRITE ENABLE
GØ2A	16C4	WAIT OR INI INSTRUCTION
I(0-15)	10	INSTRUCTION REGISTER OUTPUT
ICI	22B2	INTERRUPT CHAIN INTERRUPTS
ICIDAT	25B2	ICI DATA
ICIEN	21B3	ICI ENABLE
ICIECH	23B3	ICI COMMAND ECHO
ILAC	7A4	INSTRUCTION LOADS ACCUMULATOR
INFF	16C2	INI INSTRUCTION FLIP-FLOP [illegible]
INIECH	23B2	[illegible] COMMAND ECHO
INT	19C2	INTERRUPT - [illegible]
INT(6-15)	21C2	[illegible]
IØD(0-7)	11	I/Ø DATA
IØFF	16A2	I/Ø FLIP-FLOP
IØLCK	15B4	I/Ø DATA LATCH CLOCK
IØL2	15B4	I/Ø DATA LATCH ZERO
ISTRB	22C4	INTERNAL STROBE
IWE	10A3	INSTRUCTION REGISTER WRITE ENABLE
IWEA	10A4	INSTRUCTION REGISTER WRITE ENABLE A
KFØ-KF2	22B5	K- FIELD, CPU BUS
LFBYTE	28A4	WRITE LEFT BYTE
LMRLD	30B4	LINE NUMBER REGISTER LOAD
LWE(0-1)	9B4	PROGRAM COUNTER LOAD ENABLE
MARINC	30B4	MEMORY ADDRESS INCREMENT
MD(0-15)	18	MEMORY DATA
MDIEN	30B4	MEMORY OUTPUT DATA ENABLE
MEMWE	30B1	MEMORY WRITE ENABLE
MEMWRT	30B4	WRITE INTO MEMORY
MT	15C1	MET TEST CONDITION (TEST TRUE)
MUA(0-7)	6a	MULTIPLEXED A BUS
MUB(0-7)	6a	MULTIPLEXED B BUS
ØFØ-ØF2	22A4	O- FIELD, CPU BUS
ØSC	17A5	OSCILLATOR
PC(01-05)	9	PROGRAM COUNTER CARRY
PCE	9C3	PROGRAM COUNTER ENABLE
PCE(1,2)	9C4	PROGRAM COUNTER ENABLE
PCIE-1	24A2	PERIPHERAL CODE (CPU BUS SIGNAL)
PFFIP	27C5	POWER FAILURE IN PROGRESS
PID	17C3	INTERRUPT INSTRUCTION DECODE
P(00-15)	9	PROGRAM COUNTER BITS
PLWE	9B5	PROGRAM COUNTER LOWER WRITE ENABLE
PUSH	P&PA, P&PM	PUSH INSTRUCTION DECODE

MNEMONIC GLOSSARY

MNEMONICS	SOURCE	DEFINITION
PUWE	9A2	PROGRAM COUNTER UPPER WRITE ENABLE
R+	11C2	PULL-UP
RDS	22B2	REQUEST DEVICE STATUS
RDSEN	22B4	RDS COMMAND ENABLE FLAG
RDSECH	23C2	RDS COMMAND ECHO
READ	21C3	DMA READ CYCLE
RENF	17B2	RESET THROUGH ENABLE FLIP-FLOP
RENI	17B3	RESET INTERRUPT ENABLE FLIP-FLOP
RSAD(0-9)	14B5	READ STACK ADDRESS
RTBYTE	29A4	WRITE RIGHT BYTE
R/W	22C2	READ / WRITE
SCEN	14B3	STACK CLOCK ENABLE
SCK	14B5	STACK CLOCK
SETINT	22C1	SET INTERRUPT
SGZF	16C3	SHIFT IN 0 FOR ARITHMETIC SHIFT RIGHT
SHIN	7B1	SHIFT IN (ACCUMULATOR)
SIFF	17B3	SET INTERRUPT FLIP-FLOP
SIOF	16A5	SET I/Ø FLIP-FLOP
SREG	24C4	SYSTEM RESET
SRST-1	12A4	SYSTEM RESET
STRB	24A5	STROBE (CPU I/Ø BUS SIGNAL)
STRENB	22B4	EDF STR ENABLE FLAG
STRECH	23B2	EDF STR COMMAND ECHO
STRABE	19B2	I/Ø DATA STROBE
SU(0-7)	15	STACK UPPER
SWE	13B5	STACK WRITE ENABLE
SYRST	22A2	SYSTEM RESET (CPU BUS SIGNAL)
TFF	14C2	TIMING FLIP FLOP OUTPUTS
ULWB-ULWC	9A4	UPPER PROGRAM COUNTER LOAD
XINK	17B2	INTERRUPT ACTIVITY CONTROL
INTR	24B3	INTERRUPT - T-11
PIN 14	9C3	PROG COUNTER INPUT BIT 14
CMT	15C2	CONTROL "MET TEST"
CMDSBL	18B1	CONTROL MEMORY DISABLE
DRL0-7	20A2 & B2	DATA REGISTER LOWER
DRU0-7	20B2 & C2	DATA REGISTER UPPER
DISK	24B3	DISK CONTROLLER USE
SBFA	16B3	SET BFF SIGNAL
CMT	15C1	CONDITION MET
DRL(0-7)	2D	DATA REGISTER LOWER-DMA
DRU(0-7)	2D	DATA REGISTER UPPER-DMA
DALM	8A1	DECODE ALU MODE CONTROL
SBFA	16B4	SET BFF FLIP-FLOP
SELECT 0-7	18C4	CONTROL MEMORY BMP SELECT
STRB+A	14B1	STROBE ENABLE

CODE IDENT 52483	WHITE LOGIC DIAGRAMS - PROGRAMMABLE DEVICE CONTROLLER		
SCALE NONE	SIZE C	DRAWING NO. 300337	REV. 1C
SHEET 3 OF			

5016 REV 6/71


5
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J1
1 DIB06-
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8 DIB13-
9 DIB10-
10 DIB11-
11 DIB07-
12 DIB02-
13 DIB03-
14 DIB05-
15 DIB08-
16 DIB09-
17 GND
18 END-
19 GND
20 STRB-
21 GND
22 DMAP1+
23 GND
24 INT15-
25 GND
26 DMAP2+
27 GND
28 INT13-
29 GND
30 INT12-
31 GND
32 INT08-
33 GND
34 INT10-
35 GND
36 INT11-
37 GND
38 INT09-
39 GND
40 INTM-
41 GND
42 DMAP3+
43 GND
44 PCLK-
45 GND
46 DA03-
47 CF2-
48 CFD-
49 DA01-
50 CF1-
J2
1 DMRQ-
2 GND
3 DAIRS-
4 GND
5 SYRST-
6 GND
7 DMALD-
8 GND
9 SPARE
10 DOB11-
11 DOB13-
12 DOB12-
13 DOB07-
14 DOB04-
15 DOB05-
16 DOB06-
17 DOB01-
18 DOB02-
19 DOB00-
20 DOB09-
21 DOB03-
22 DOB10-
23 DOB14-
24 DOB08-
25 DOB15-
26 GND
27 BUSY+
28 GND
29 DMOS-
30 PRLD-
31 GND
32 DMACWI-
33 GND
34 DMACWO-
35 GND
36 DMAMB-
37 GND
38 DMAST-
39 GND
40 ALOAD+
41 PFFIP-
42 ALOAD-
43 GND
44 DA00-
45 DA02-
46 DA03-
47 DA04-
48 KF0-
49 KF1-
50 KF2-
J3
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2 EXTRES-
3 SRST-
4 GND
5 DA0-
6 GND
7 DA1-
8 GND
9 DA2-
10 GND
11 DA3-
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13 DA4-
14 GND
15 DA5-
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17 DA6-
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19 DA7-
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23 I@D1-
24 GND
25 I@D2-
26 GND
27 I@D3-
28 GND
29 I@D4-
30 GND
31 I@D5-
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33 I@D6-
34 GND
35 I@D7-
36 GND
37 N/C
38 GND
39 EXTINT-
40 GND
41 DDL-
42 GND
43 CLK+
44 GND
45 GND
46 GND
47 BRDY-
48 GND
49 STRBBE-
50 GND
J4
1 SPARE
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49
50 SPARE
J11
1 GND
2 IWE+
3 GND
4 GND
5 GND
6 DWAIT-
7 GND
8 GND
9 GND
10 CL2-
11 GND
12 GND
13 GND
14 ENFF-
15 GND
16 GND
17 GND
18 CMDSBL-
19 GND
20
21
22
23
24
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27
28
29
30 GND
J12
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2 MD00+
3 GND
4 MD01+
5 GND
6 MD02+
7 GND
8 MD03+
9 GND
10 MD04+
11 GND
12 MD05+
13 GND
14 MD06+
15 GND
16 MD07+
17 GND
18 MD08+
19 GND
20 MD09+
21 GND
22 MD10+
23 GND
24 MD11+
25 GND
26 MD12+
27 GND
28 MD13+
29 MD15+
30 MDM+
J13
1 P15+
2 PM+
3 GND
4 P13+
5 GND
6 P12+
7 GND
8 P11+
9 GND
10 P10+
11 GND
12 P09+
13 GND
14 P08+
15 GND
16 P07+
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20 P05+
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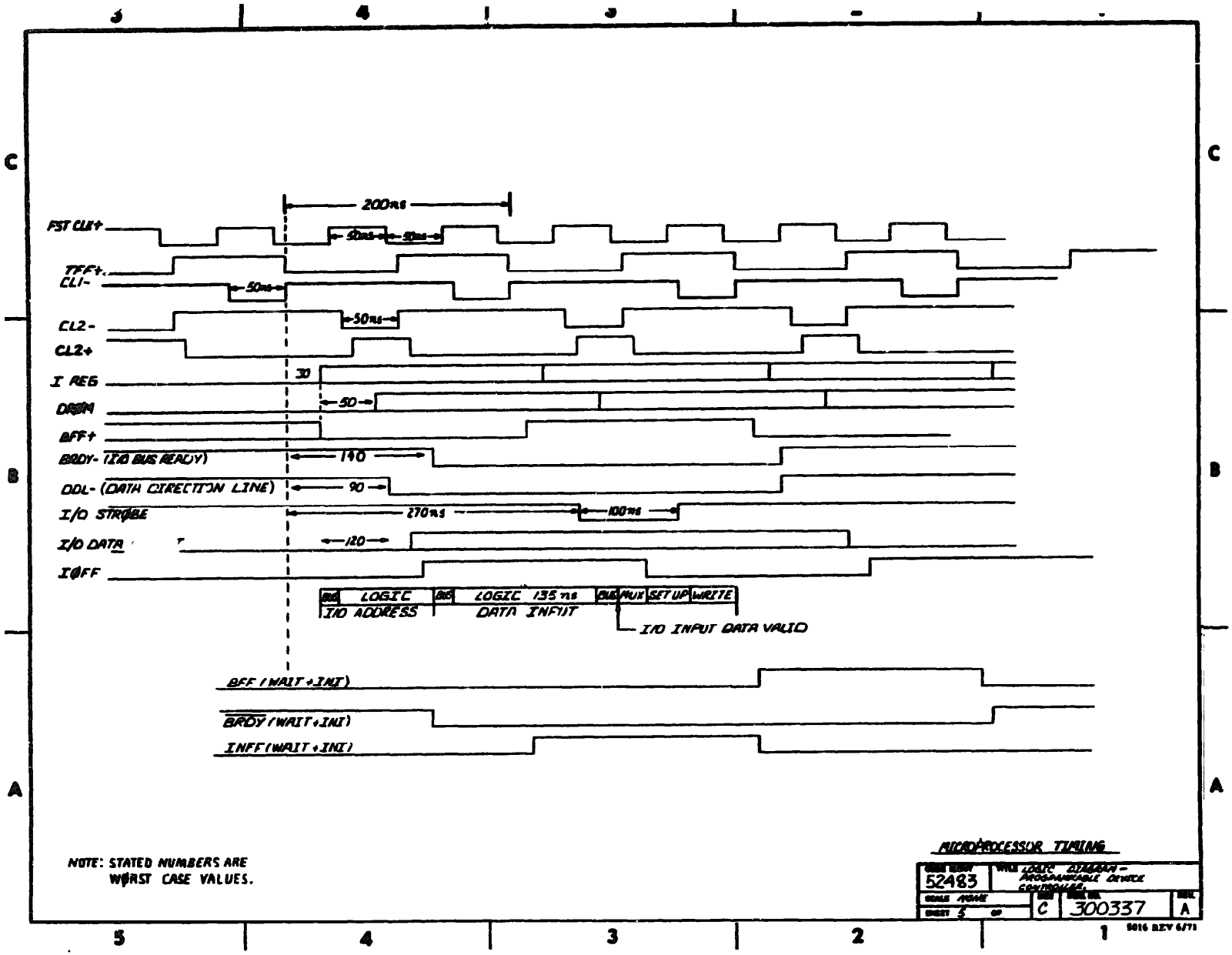
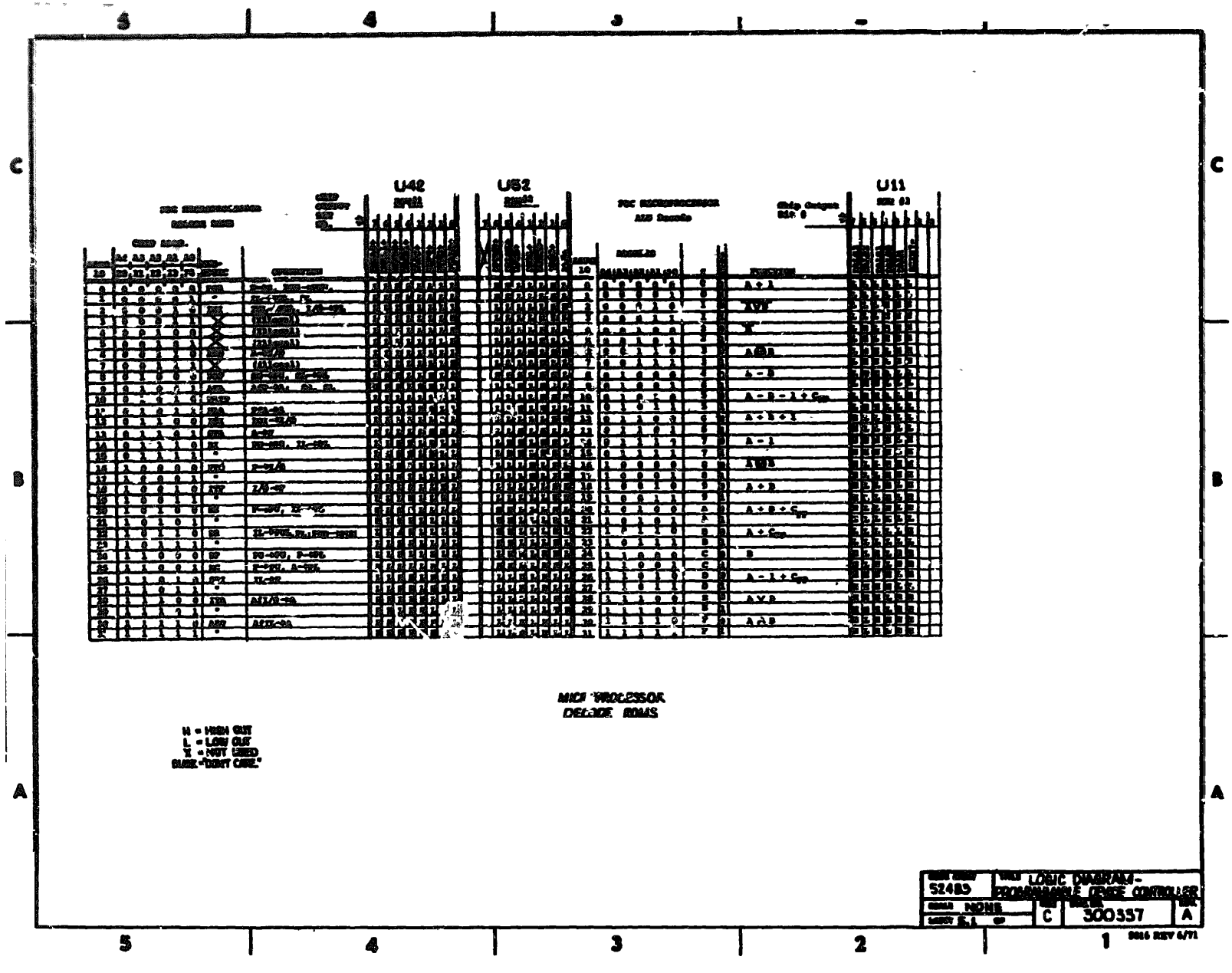
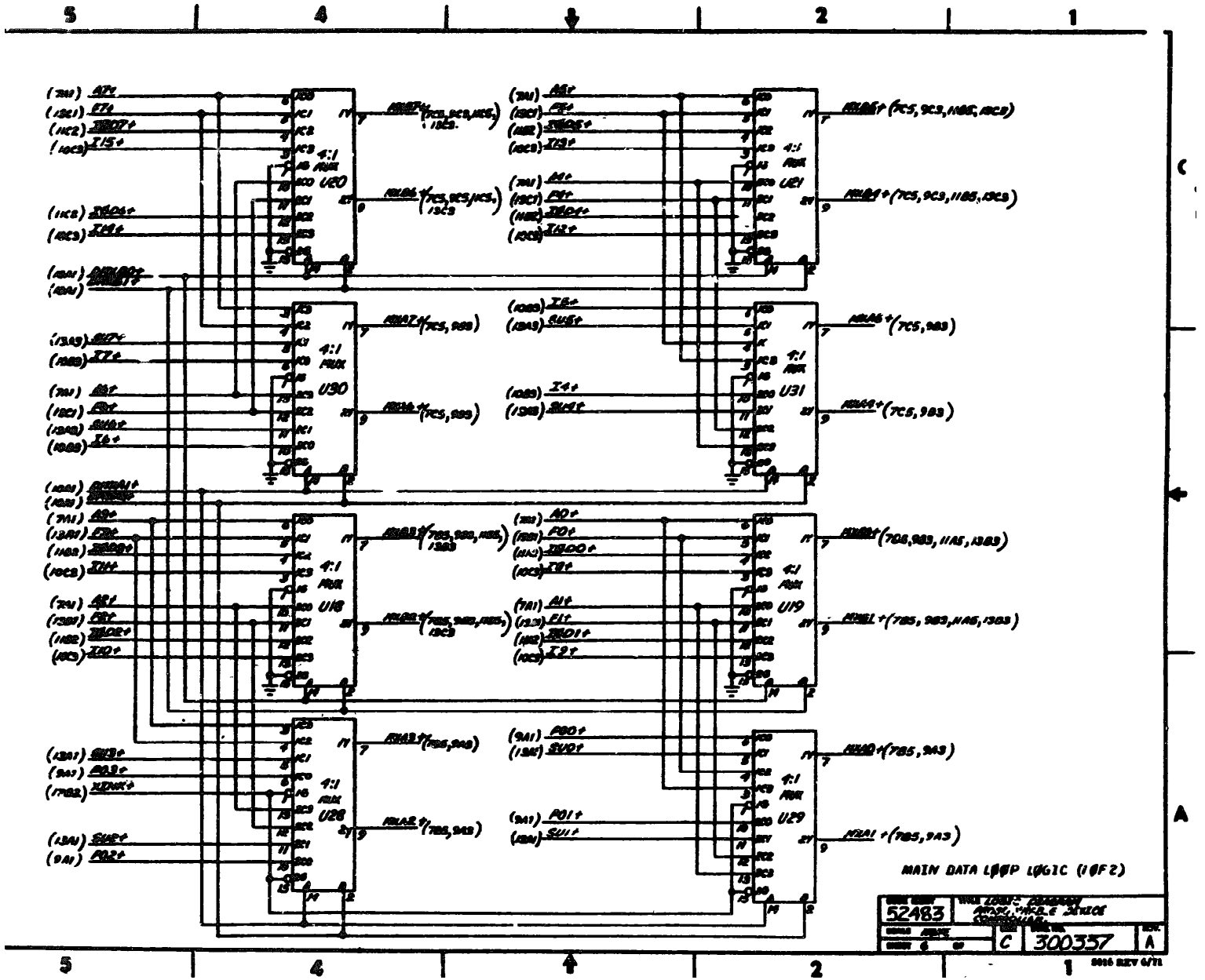
25 GND
26 P02+
27 GND
28 P01+
29 GND
30 P00+
PM+
1 GND
2 GND
3 GND
4 GND
5 +5V
6 +5V
7 +5V
8 SPARE
9
10
11
12 SPARE
A GND
B GND
C GND
D GND
E +5V
F +5V
H +5V
J SPARE
K
L
M
N SPARE
+5V
C6-C12
18
10V
GND
+5V
C13-C109
.01
GND
52483
C
300357
A


200ns
FST CLK+
50ns
50ns
TFF+
CLI-
50ns
CL2-
50ns
CL2+
I REG
30
ORIM
50
BFF+
BRDY- (I/O BUS READY)
140
DDL- (DATA DIRECTION LINE)
90
I/O STROBE
270ns
100ns
I/O DATA
120
IØFF
LOGIC
I/O ADDRESS
LOGIC 135 ns
DATA INFUT
MUX
SET UP
WRITE
I/O INPUT DATA VALID
BFF (WAIT+INI)
BRDY (WAIT+INI)
INFF (WAIT+INI)
NOTE: STATED NUMBERS ARE
WORST CASE VALUES.
MICROPROCESSOR TIMING
52483
C
300337
A


U42
U52
U11
MICROPROCESSOR
DECODE ROMS
H = HIGH OUT
L = LOW OUT
X = NOT USED
BLANK = "DON'T CARE"
52483
LOGIC DIAGRAM - PROGRAMMABLE DEVICE CONTROLLER
NONE
C
300337
A


5
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C
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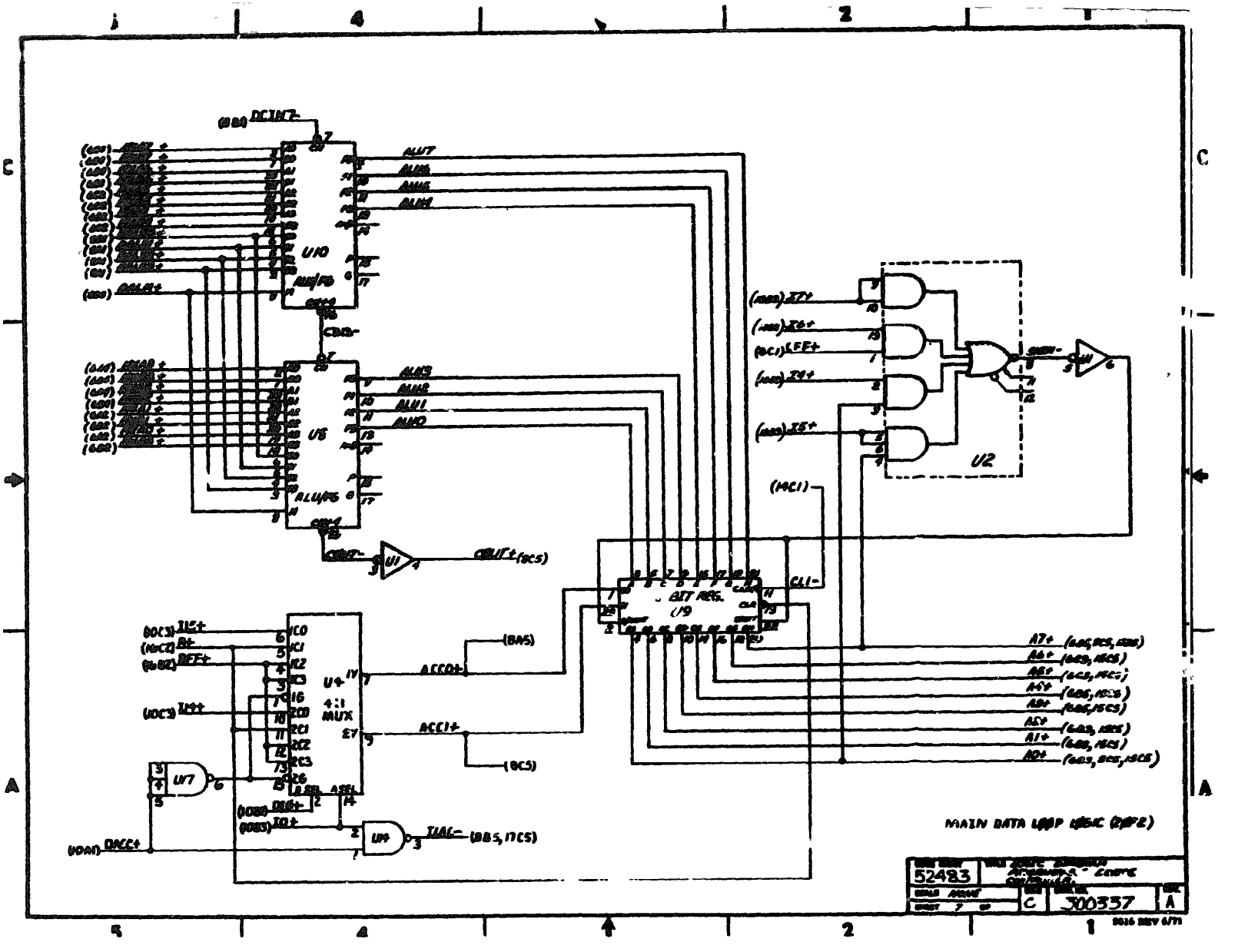
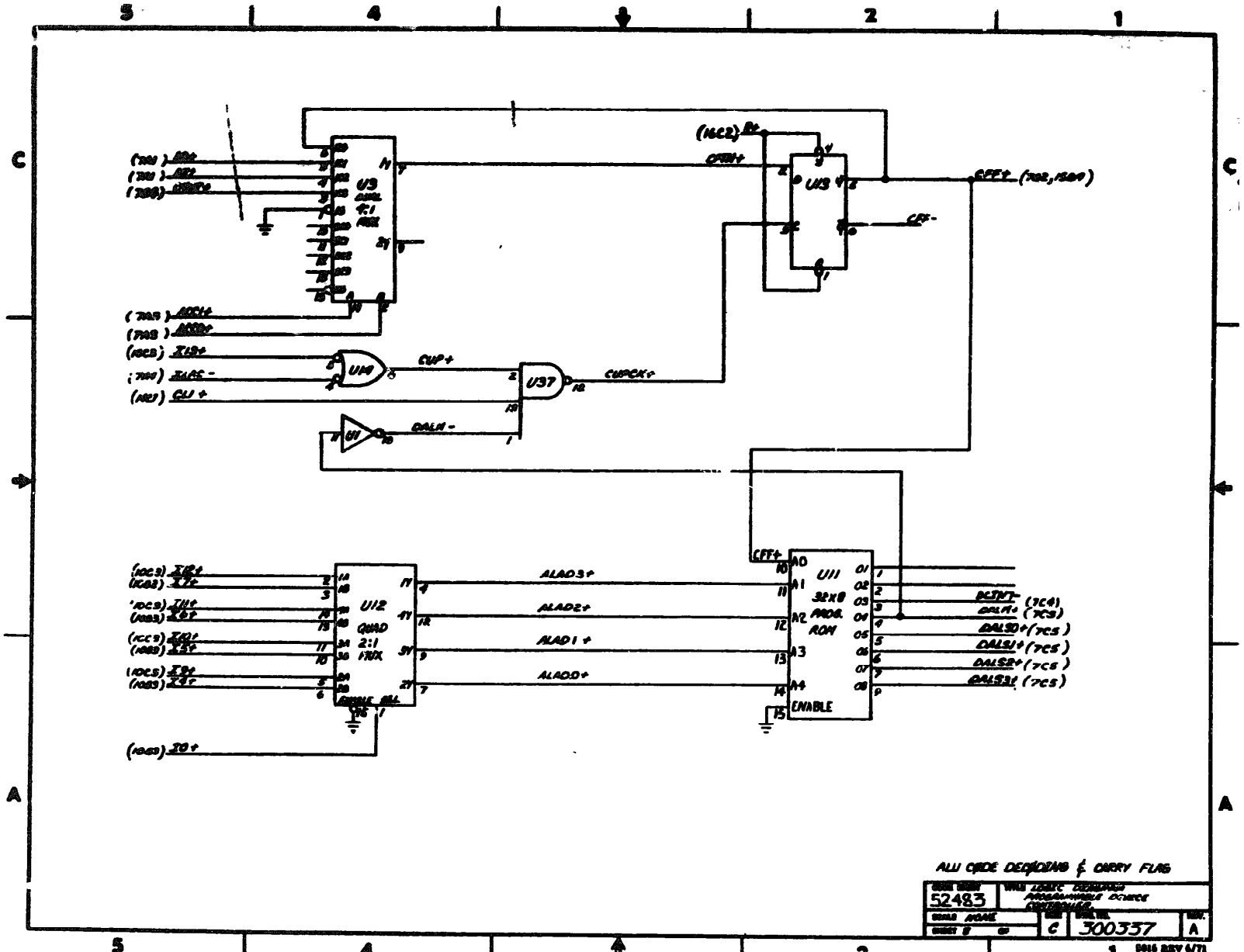
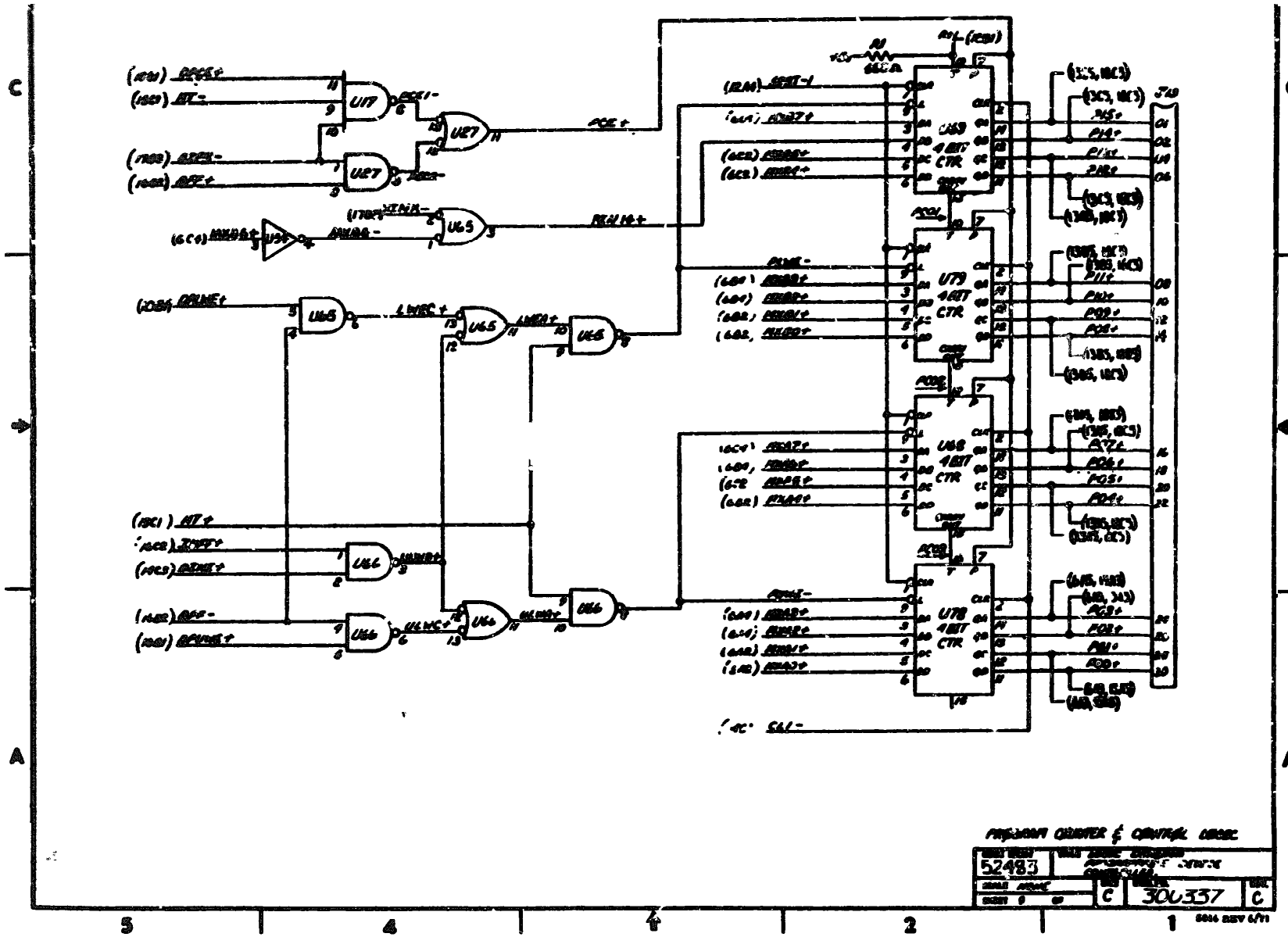
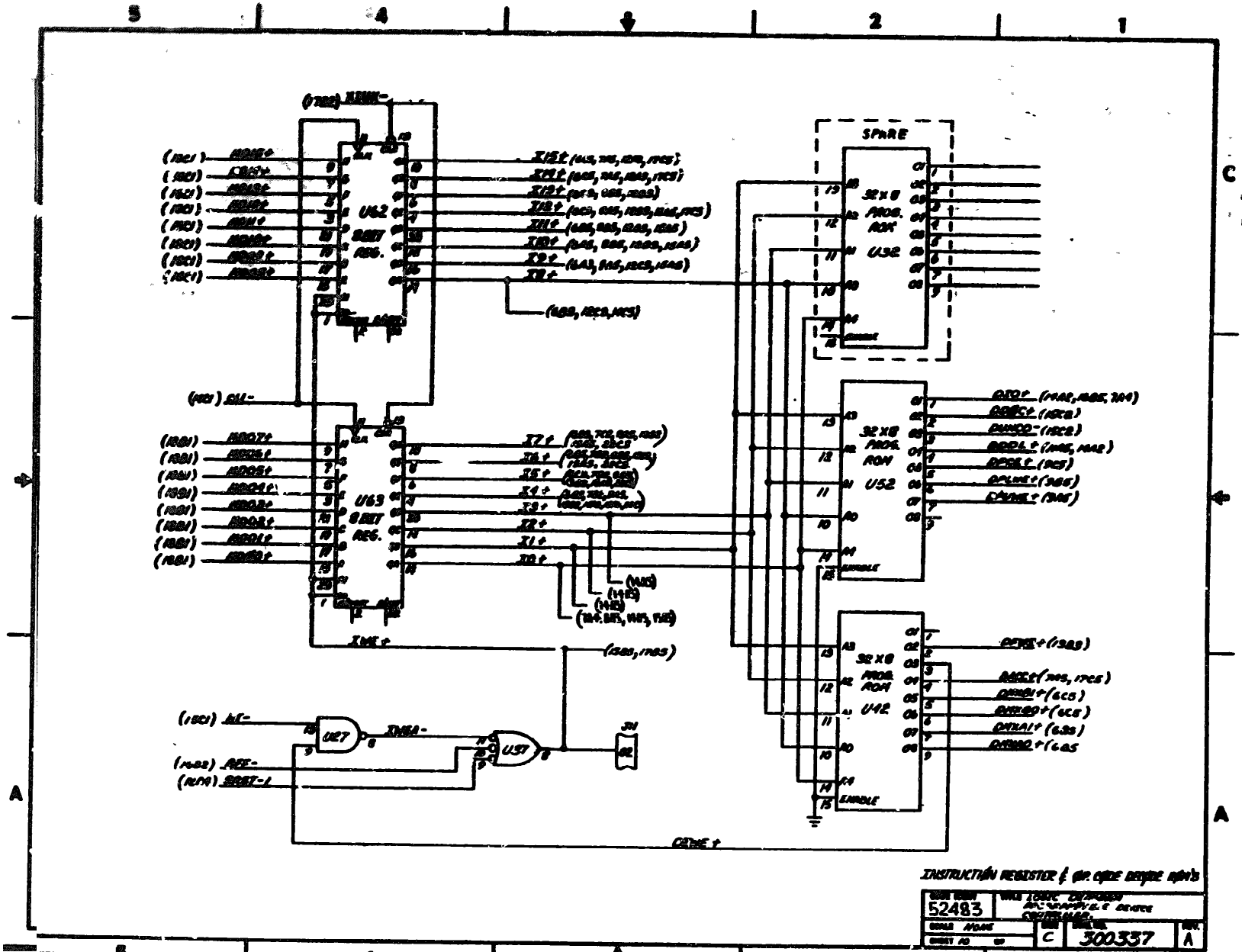
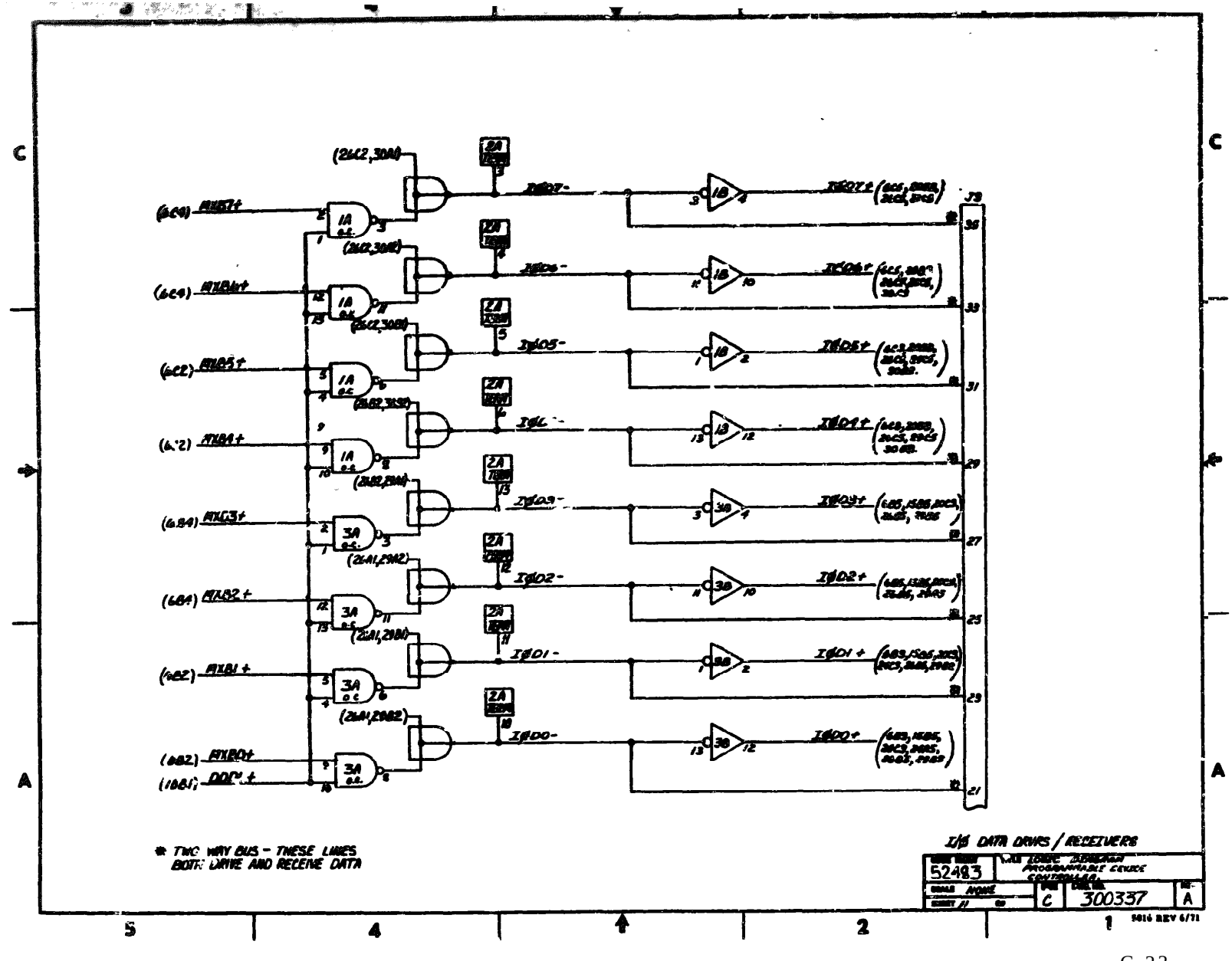
U20
U30
U18
U28
U21
U31
U19
U29
4:1 MUX
MAIN DATA LOOP LOGIC (1 OF 2)
52483
C
300357
A

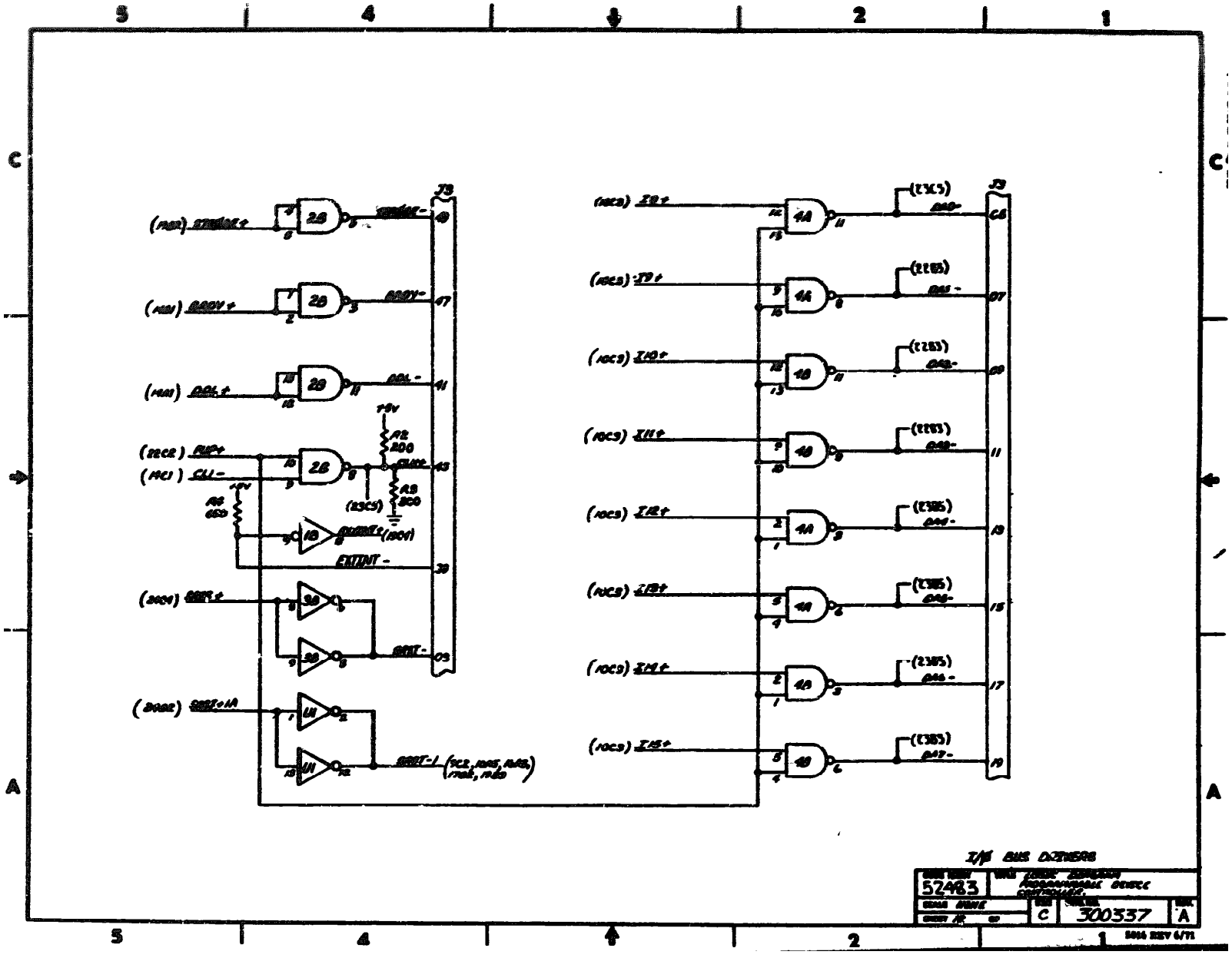

U10
U8
U2
U19
U4
4:1 MUX
U7
U9
U11
ALU7
ALU6
ALU5
ALU4
ALU3
ALU2
ALU1
ALU0
ACC0+
ACC1+
(BA5)
(BC5)
(BBS,ITCS)
MAIN DATA LOOP LOGIC (TYPE)
52483
C
300337
A

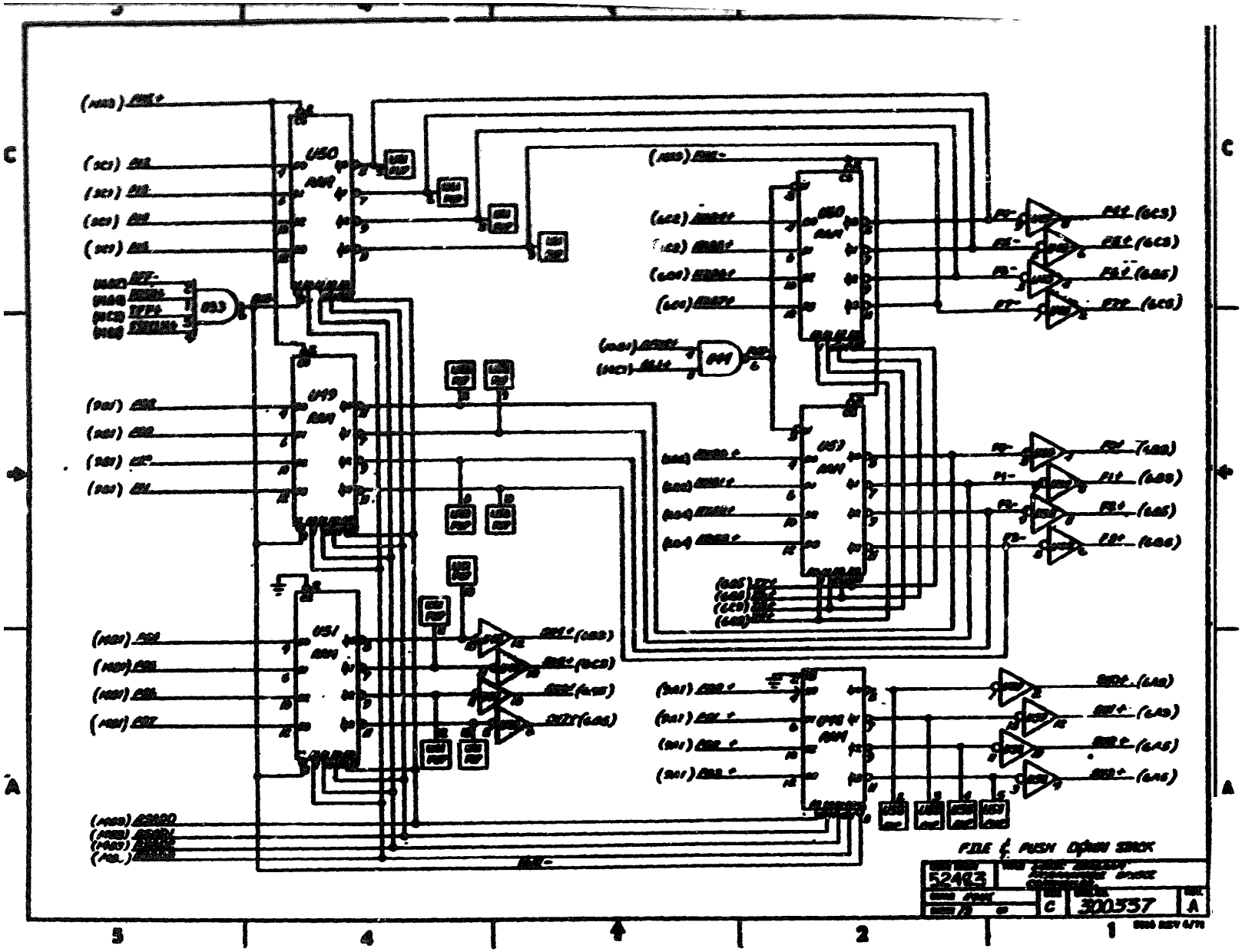

U3
U13
U10
U37
U11
U12
QUAD 2:1 MUX
32X8 PROM
ENABLE
CUP+
CUPCK+
CFF+
CFF-
ALAD3+
ALAD2+
ALAD1+
ALAD0+
ALU CODE DECODING & CARRY FLAG
52483
C
300337
A

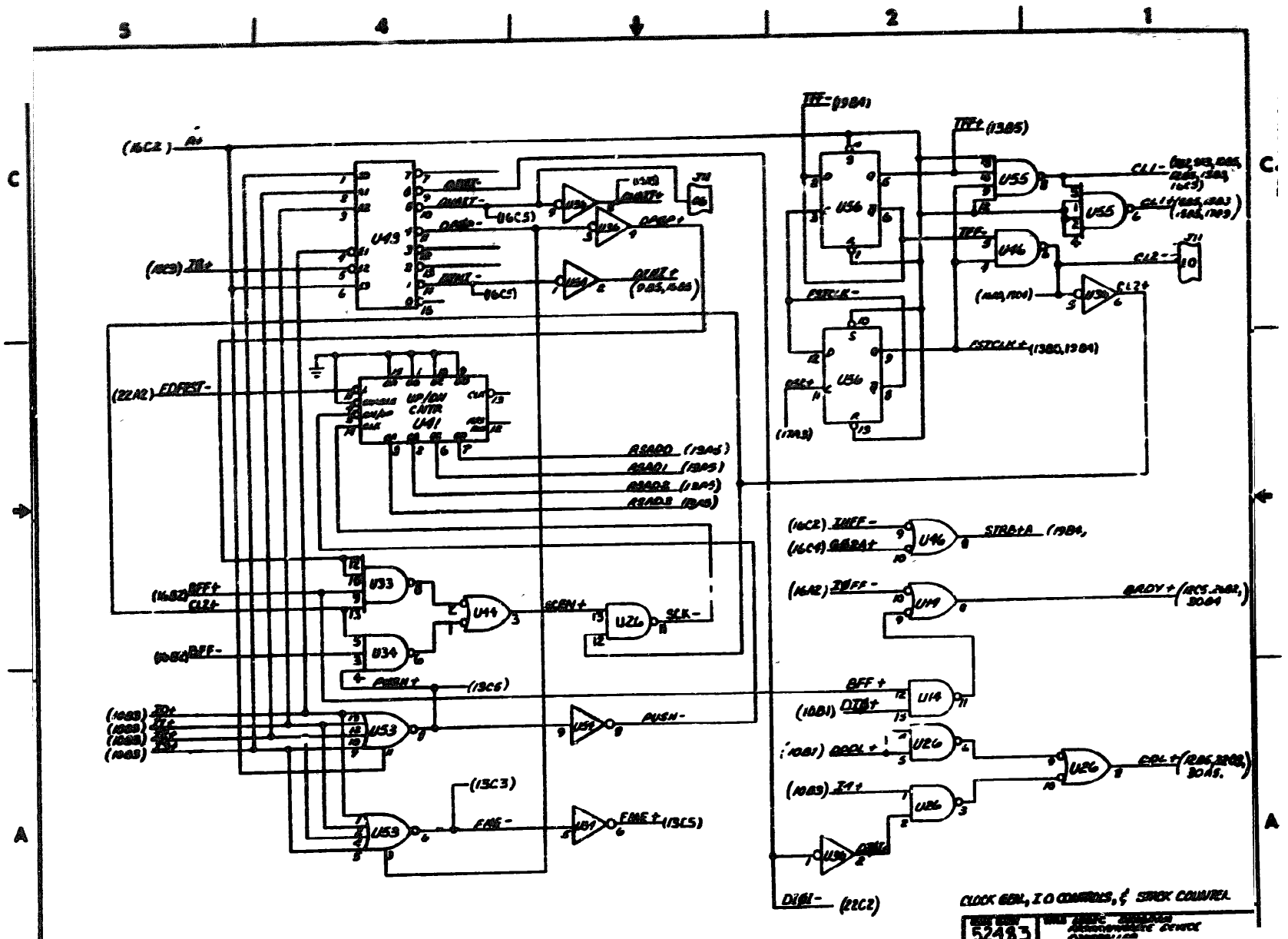

PRESCALER DIVIDER & CONTROL LOGIC
52483
C
300337
C
5
4
3
2
1
A
C

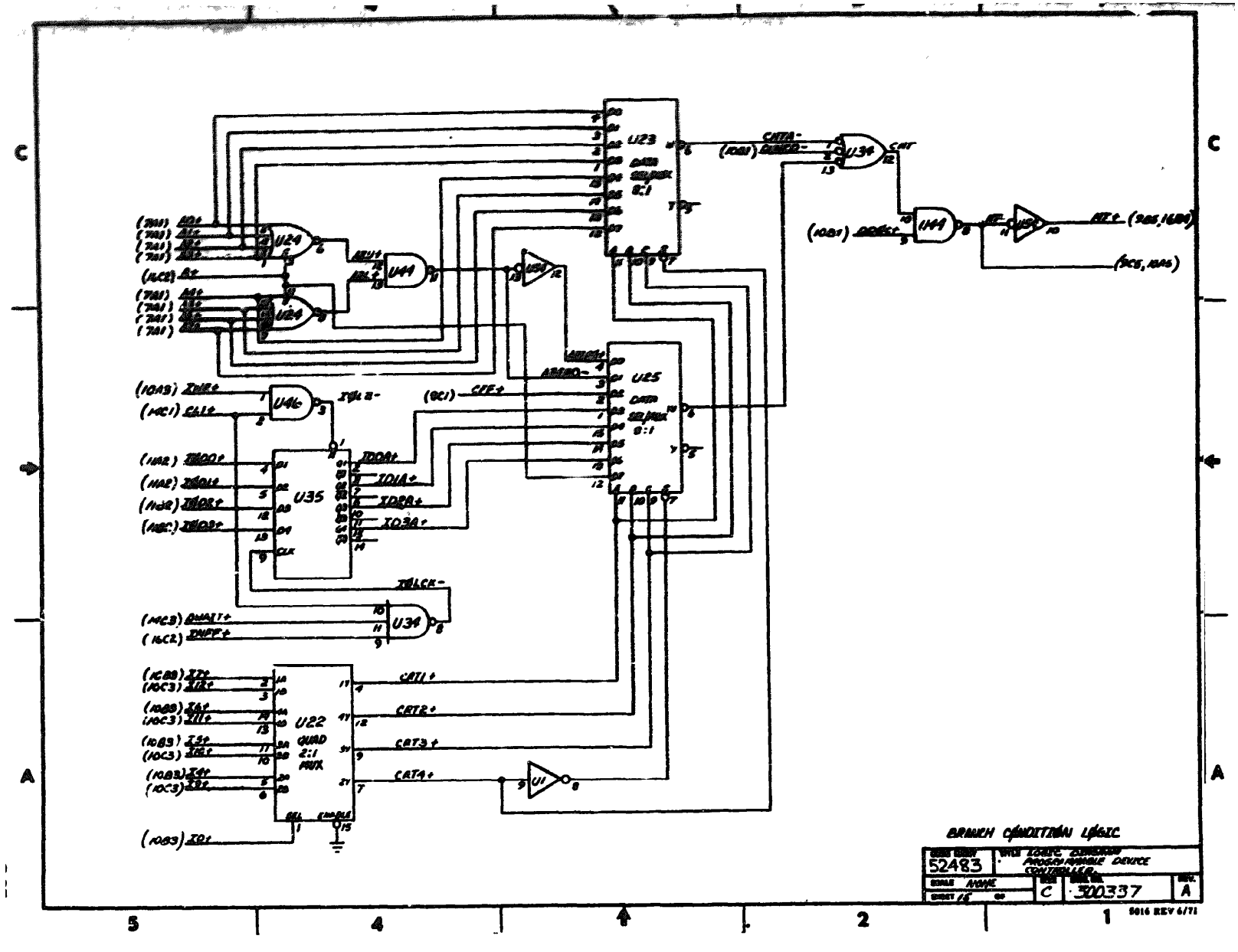

SPARE
U62
U63
U57
U52
U32
U42
INSTRUCTION REGISTER & MISC. CONTROL DECODE PWB'S
52483
300337
C
A

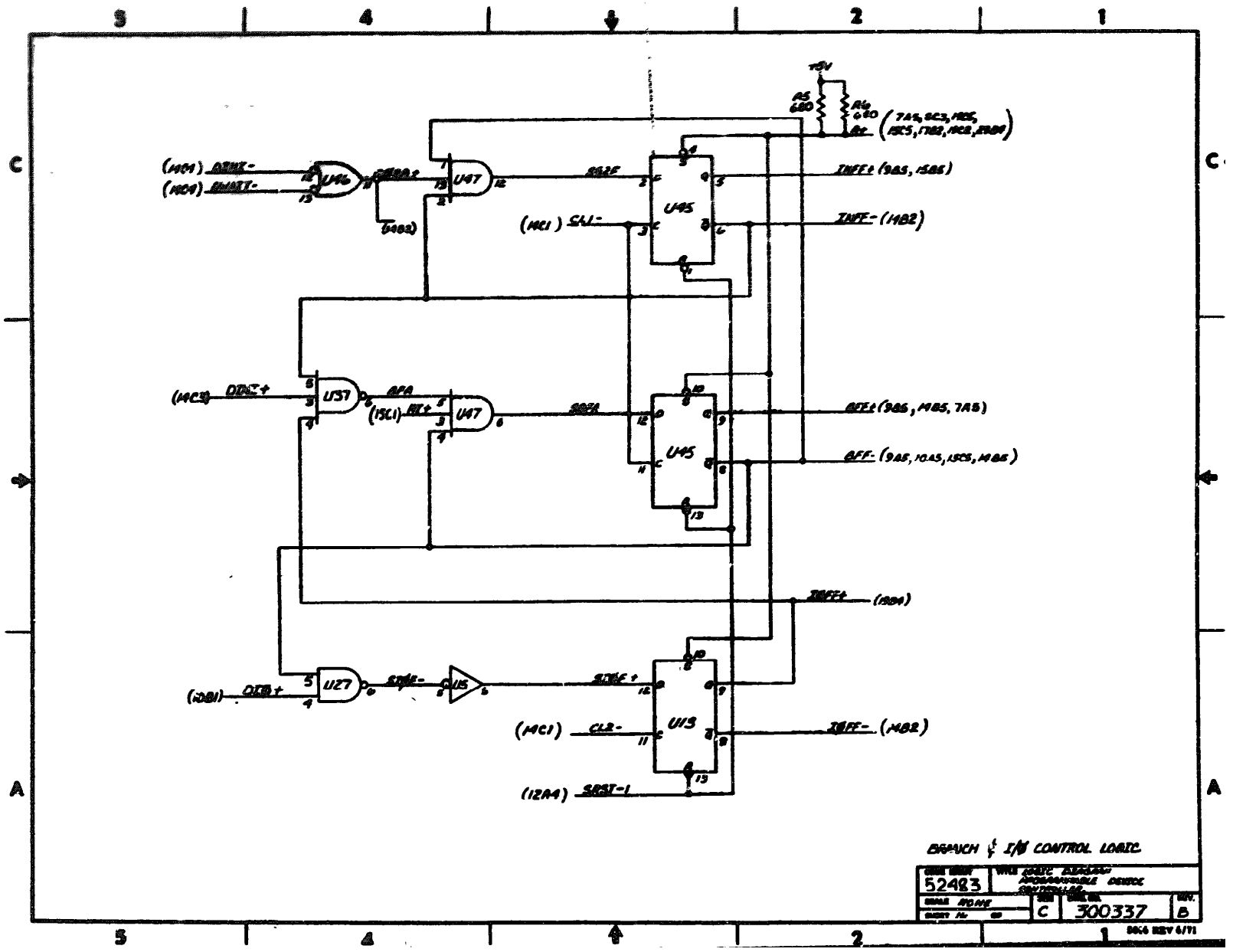

I/Ø DATA DRVRS / RECEIVERS
* TWO WAY BUS - THESE LINES BOTH DRIVE AND RECEIVE DATA
52483
MOUE
C
300337
A
5016 REV 6/71

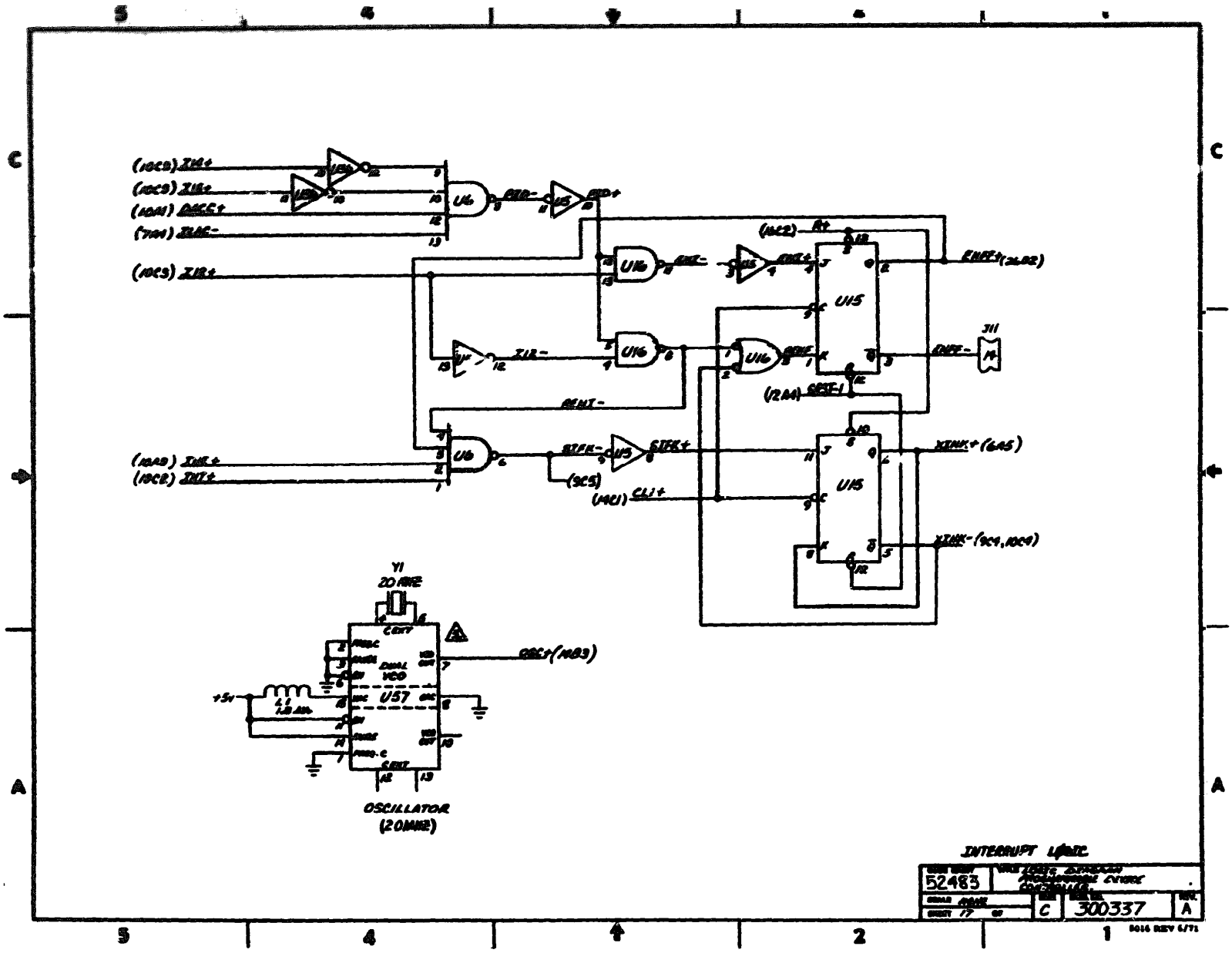

J3
2B
2B
2B
2B
1B
9B
9B
1H
1H
1A
1A
1B
4B
1A
1A
1A
1A
4B
EXTINT -
+5V
R2
200
R3
200
R4
650
R5
650
I/O BUS DRIVERS
52483
C
300537
A

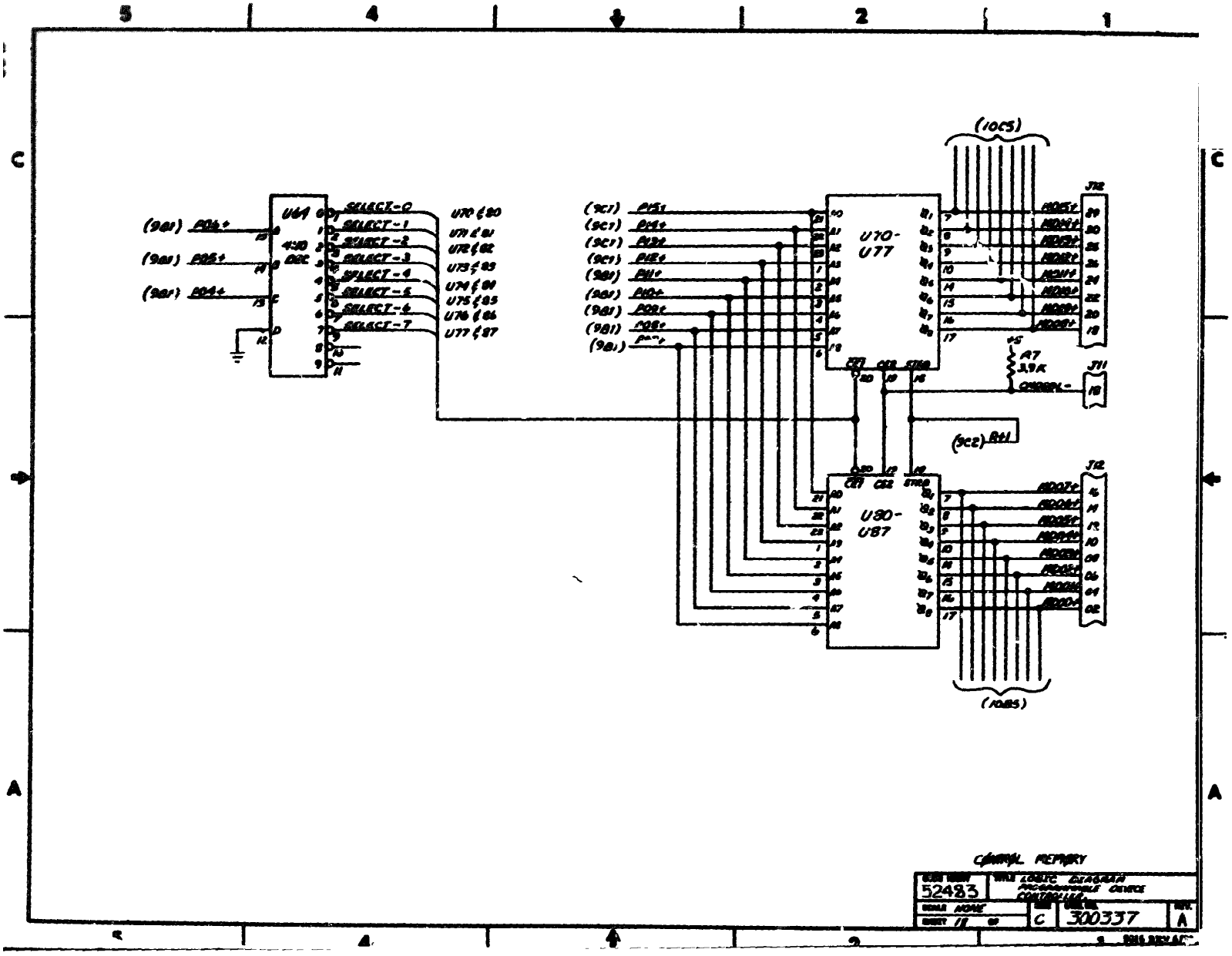

FILE & PUSH Option STACK
52483
300537
C
A

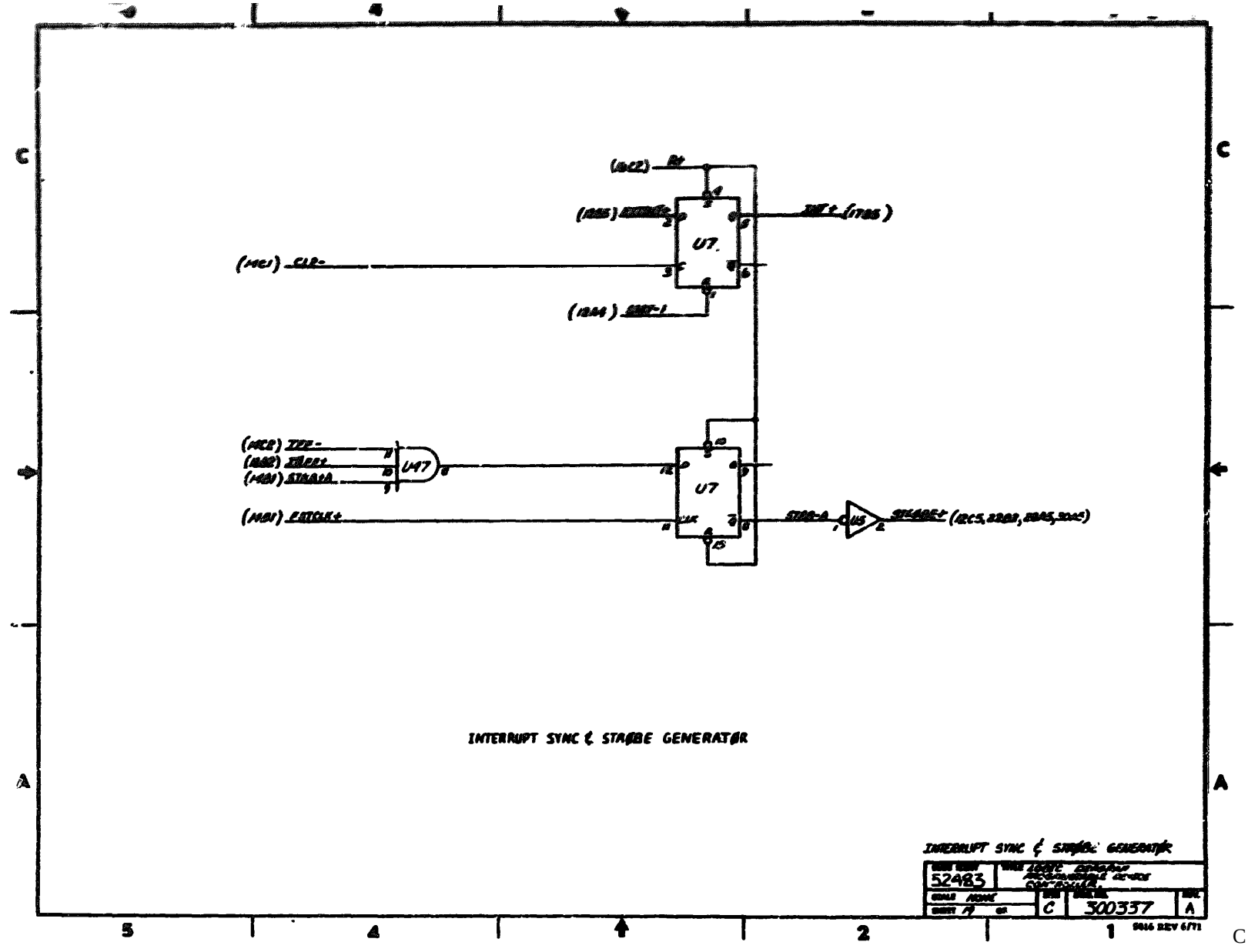

5
4
2
1
C
A
U49
U41
U33
U34
U44
U53
U59
U56
U55
U46
U14
U19
U26
U54
U24
U25
U31
U36
CLOCK GEN, I O CONTROLS, & STROK COUNTER
52483

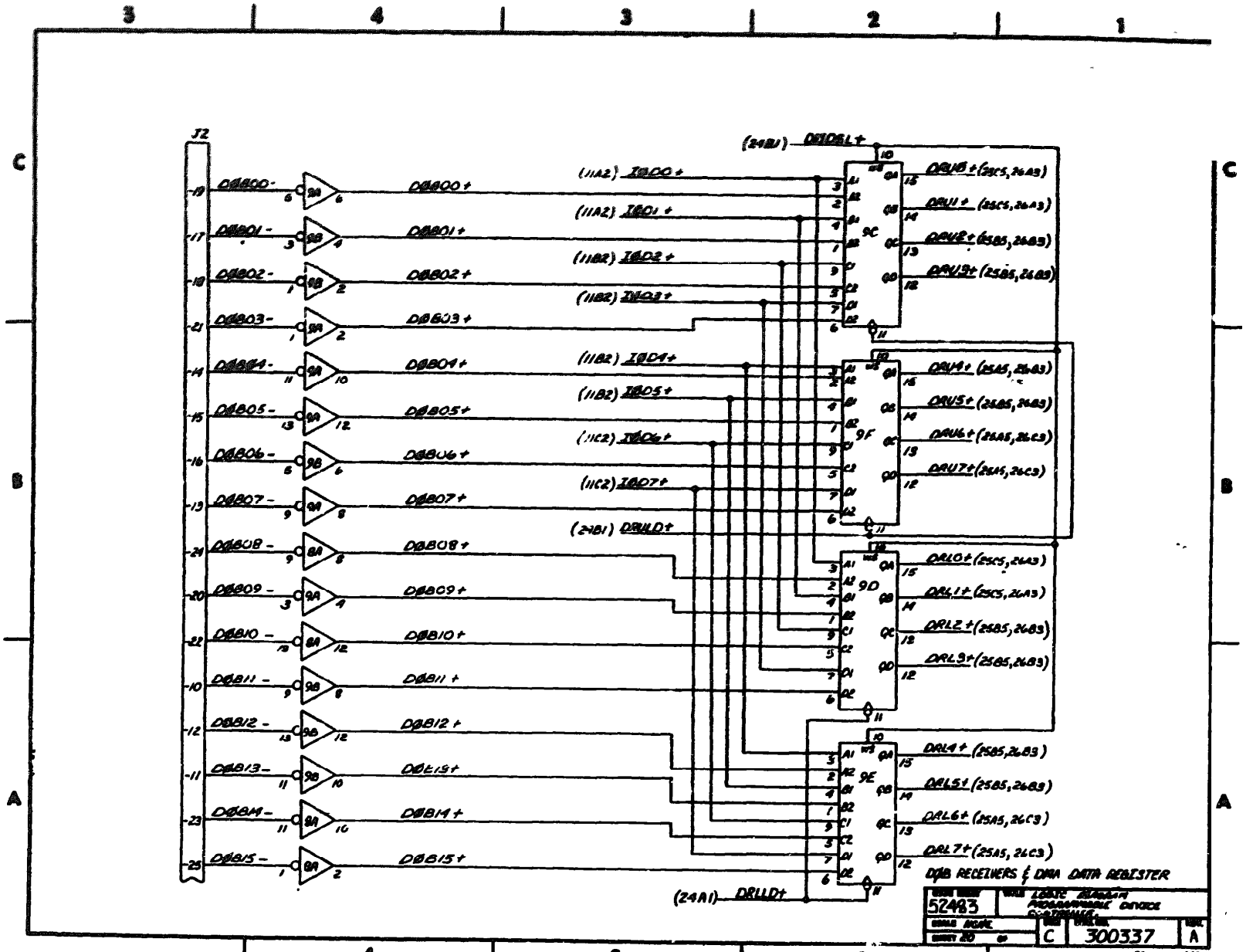

U23
U24
U44
U25
U46
U34
U35
U22
U1
U49
QUAD 2:1 MUX
BRANCH CONDITION LOGIC
52483
C
300337
A

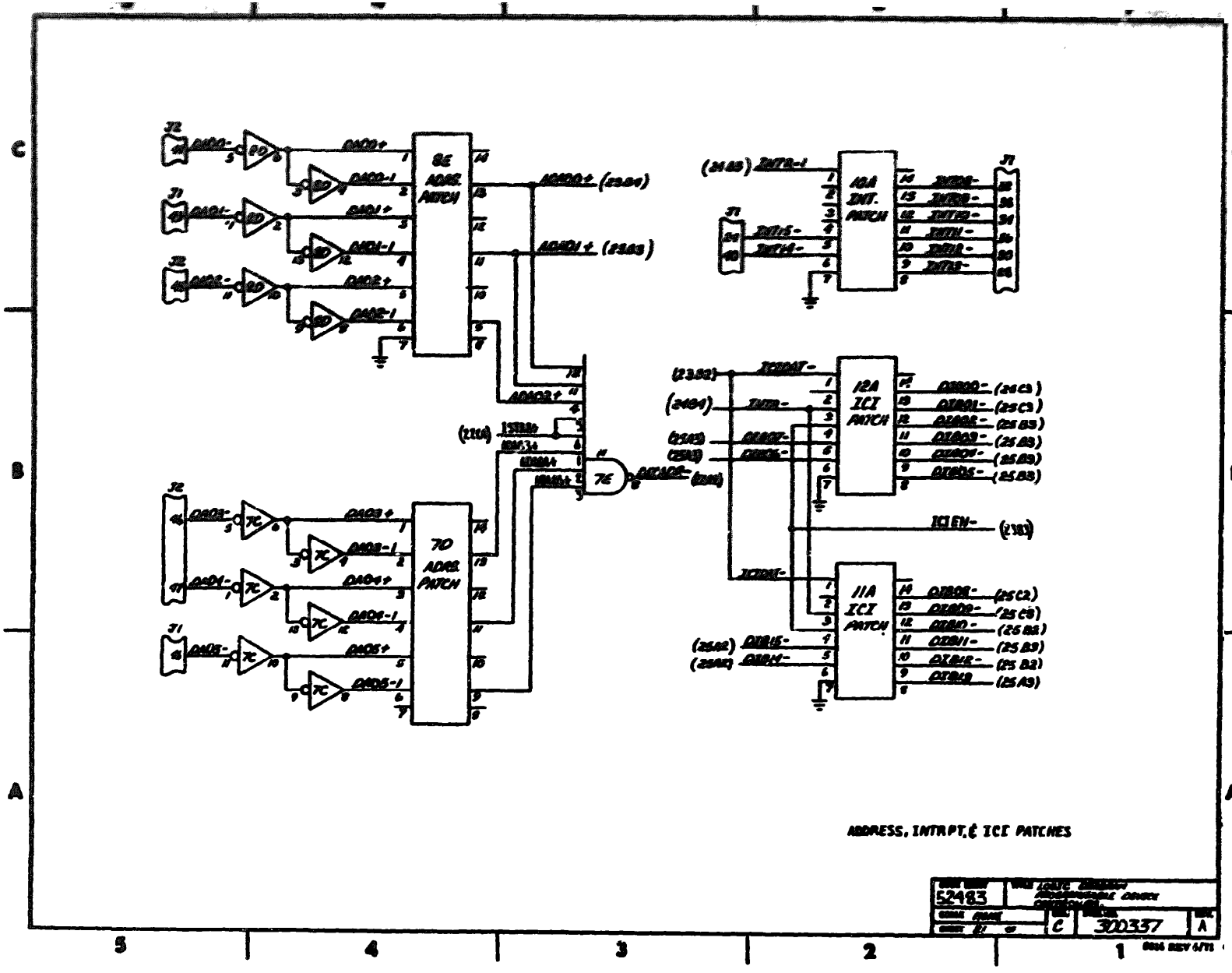

+5V
R5 680
R6 680
Rz
(7A5, 8C3, 9B5, 10C5, 11B2, 11C8, 11B8)
(4A1) BMUX-
(4C4) BMATT-
U46
U47
(4B2)
U45
(4C1) SCLI-
IMFF+ (9A5, 10A5)
IMFF- (14B2)
(3C2) ODDC+
U37
BFA
(15C1) BIC+
U47
SBFA
U45
BFF+ (9A6, 14B5, 7A5)
BFF- (9A5, 10A5, 15C5, 14B6)
IMFF+ (15B4)
(3B1) OEB+
U127
SBYE-
U15
SBYE+
U113
(4C1) CLR-
IMFF- (14B2)
(12A4) SRST-1
BRANCH & I/O CONTROL LOGIC
52483
C
300337
B

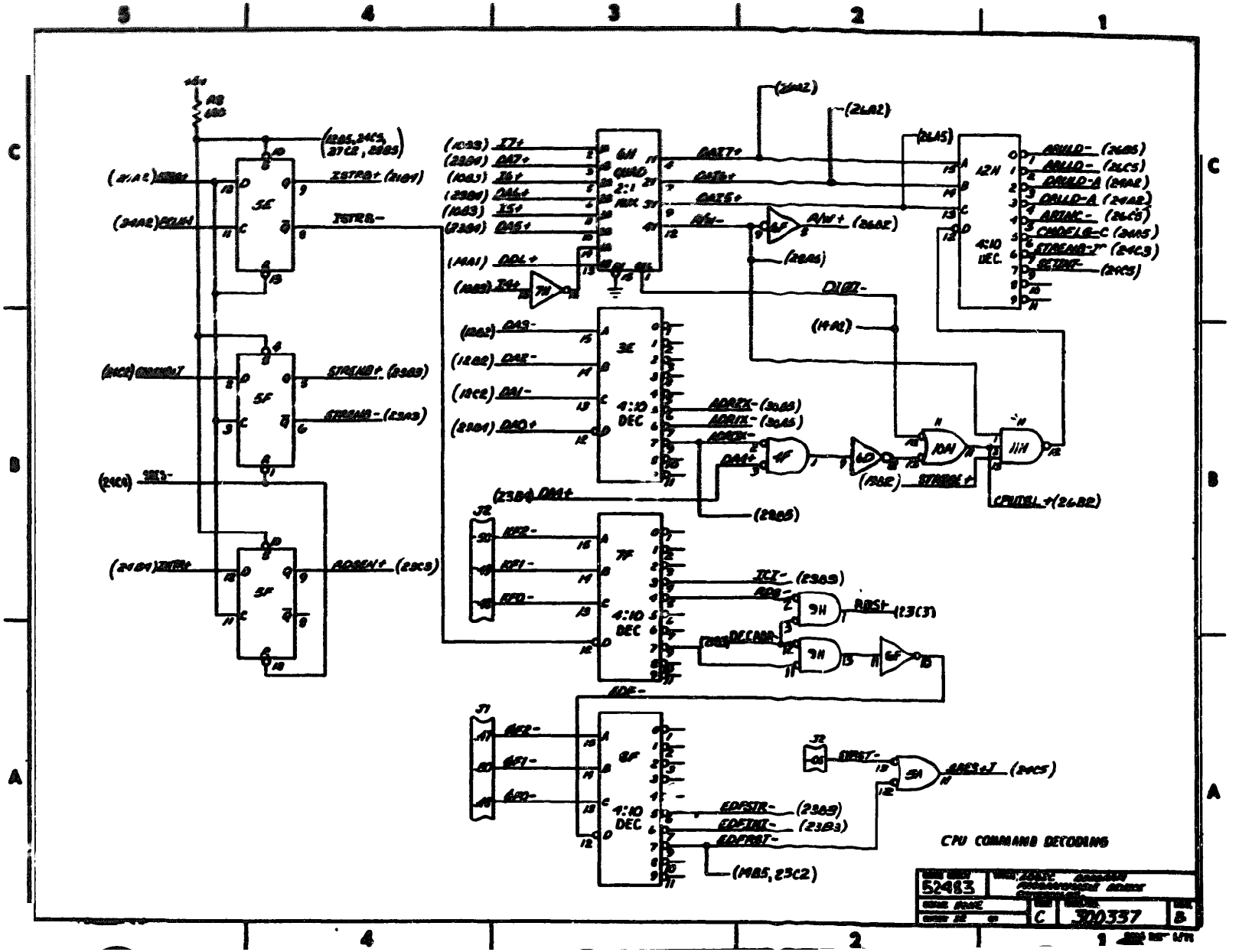

(10C2) XMT+
(10C3) XIR+
(10A1) DACC+
(7104) XIAK-
(10C3) XIR+
(10A2)
U15
U16
U17
XMIT+ (6A5)
XINK- (9C4, 10C4)
(9C5)
(10A1) CLI+
(10A8) XMT+
(10C2) XMT+
Y1
20 MHZ
VCO
U57
+5V
OSCILLATOR
(20MHZ)
INTERRUPT LOGIC
52485
C
300337
A

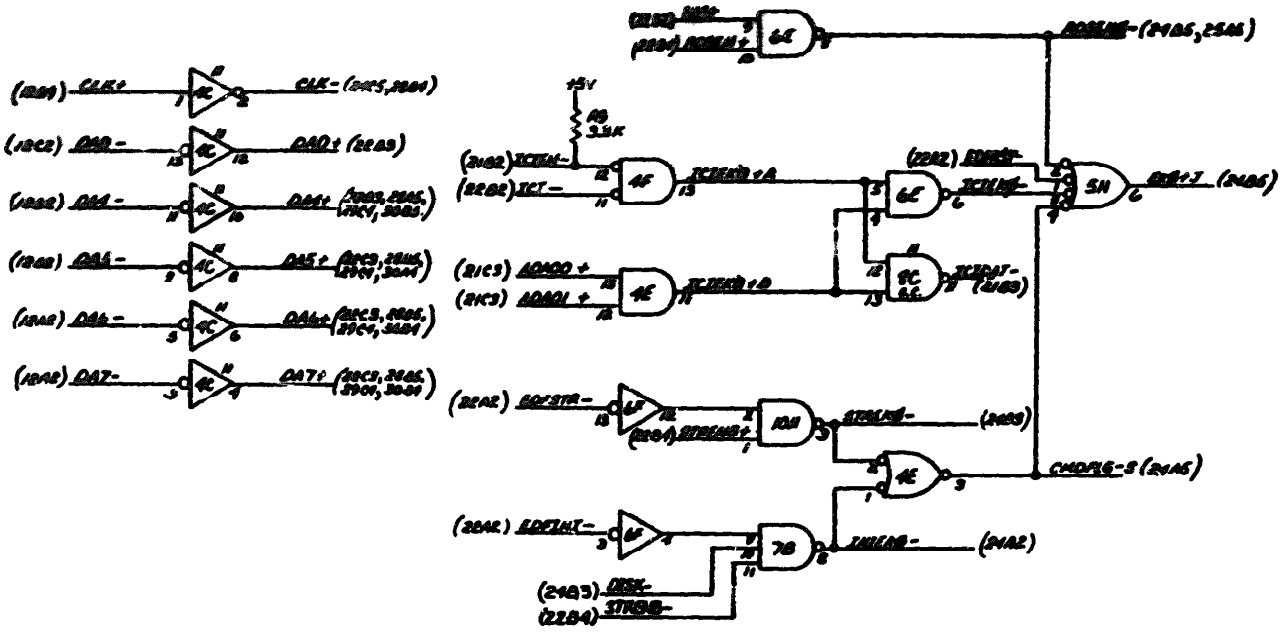

5
4
2
1
C
A
U61
4520
SELECT-0
SELECT-1
SELECT-2
SELECT-3
SELECT-4
SELECT-5
SELECT-6
SELECT-7
U70 & 80
U71 & 81
U72 & 82
U73 & 83
U74 & 84
U75 & 85
U76 & 86
U77 & 87
(98I) P06+
(98I) P05+
(98I) P04+
(9C1) P15+
(9C1) P14+
(9C1) P13+
(9C1) P12+
(98I) P11+
(98I) P10+
(98I) P09+
(98I) P08+
(98I) Parity
U70-
U77
U80-
U87
(10C5)
(10B5)
J12
J11
+5
A7
3.9K
(9C2) R11
CENTRAL MEMORY
52483
C
300337
A


U7
U47
U7
U5
INTERRUPT SYNC & STROBE GENERATOR
52483
C
300337
A


J2
DBB00- DBB00+
DBB01- DBB01+
DBB02- DBB02+
DBB03- DBB03+
DBB04- DBB04+
DBB05- DBB05+
DBB06- DBB06+
DBB07- DBB07+
DBB08- DBB08+
DBB09- DBB09+
DBB10- DBB10+
DBB11- DBB11+
DBB12- DBB12+
DBB13- DBB13+
DBB14- DBB14+
DBB15- DBB15+
(24B1) DBIOBLT+
(11A2) IBDO+
(11A2) IBD1+
(11B2) IBD2+
(11B2) IBD3+
(11B2) IBD4+
(11B2) IBD5+
(11C2) IBD6+
(11C2) IBD7+
(24B1) DRLLD+
(24A1) DRLLD+
9C
9F
9D
9E
DRL0+ (25C5, 26A3)
DRL1+ (25C5, 26A3)
DRL2+ (25B5, 26B3)
DRL3+ (25B5, 26B3)
DRL4+ (25B5, 26B3)
DRL5+ (25B5, 26B3)
DRL6+ (25A5, 26C3)
DRL7+ (25A5, 26C3)
DRM0+ (25A5, 26A3)
DRM1+ (25B5, 26A3)
DRM2+ (25B5, 26B3)
DRM3+ (25B5, 26B3)
DRM4+ (25A5, 26B3)
DRM5+ (25B5, 26B3)
DRM6+ (25A5, 26C3)
DRM7+ (25A5, 26C3)
DBB RECEIVERS & DMA DATA REGISTER
52483
C
300337
A

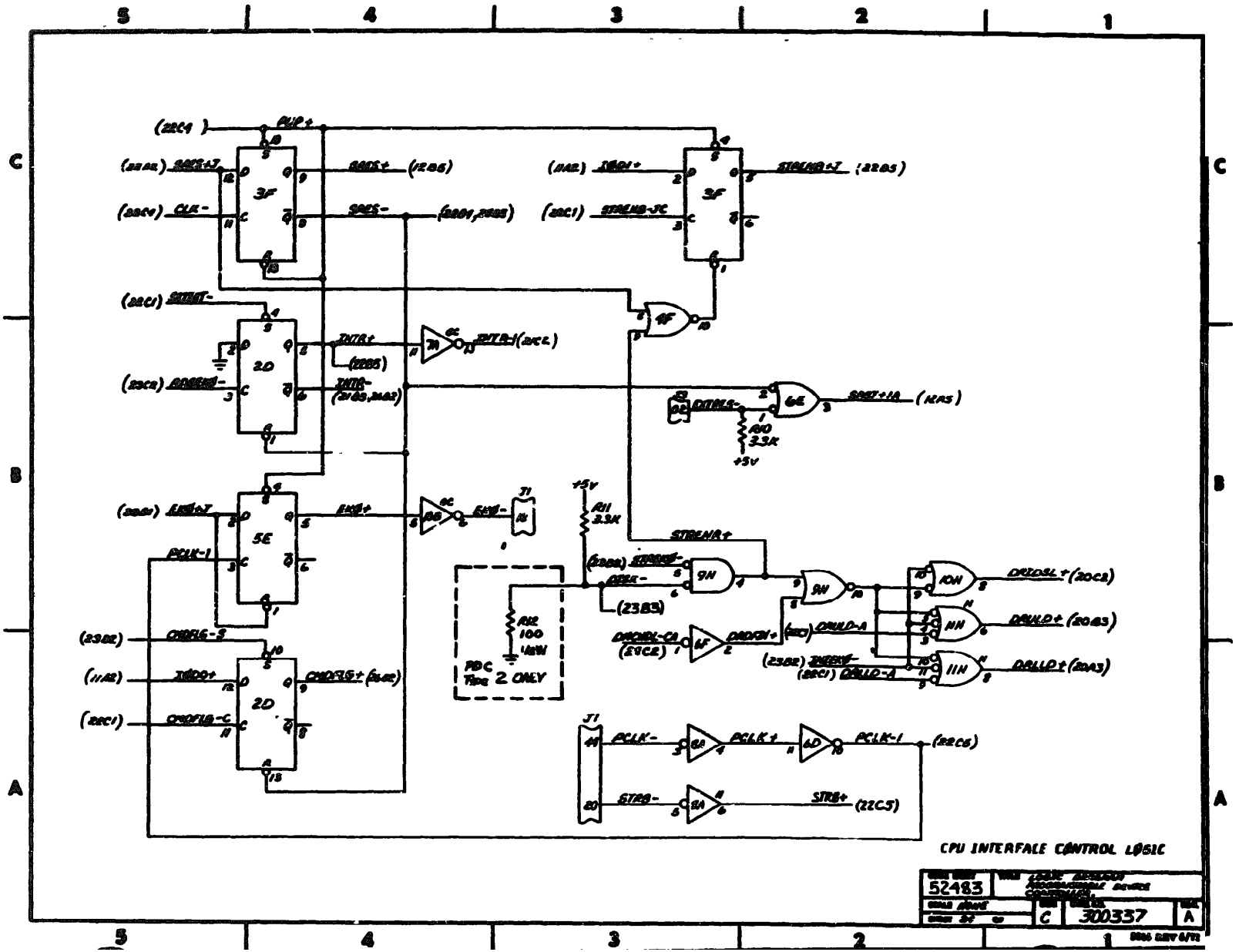

8E ADDR. PATCH
7D ADDR. PATCH
7E
12A ICI PATCH
11A INT. PATCH
11A ICI PATCH
ADDRESS, INTRPT, & ICI PATCHES
52483
300337
C
A

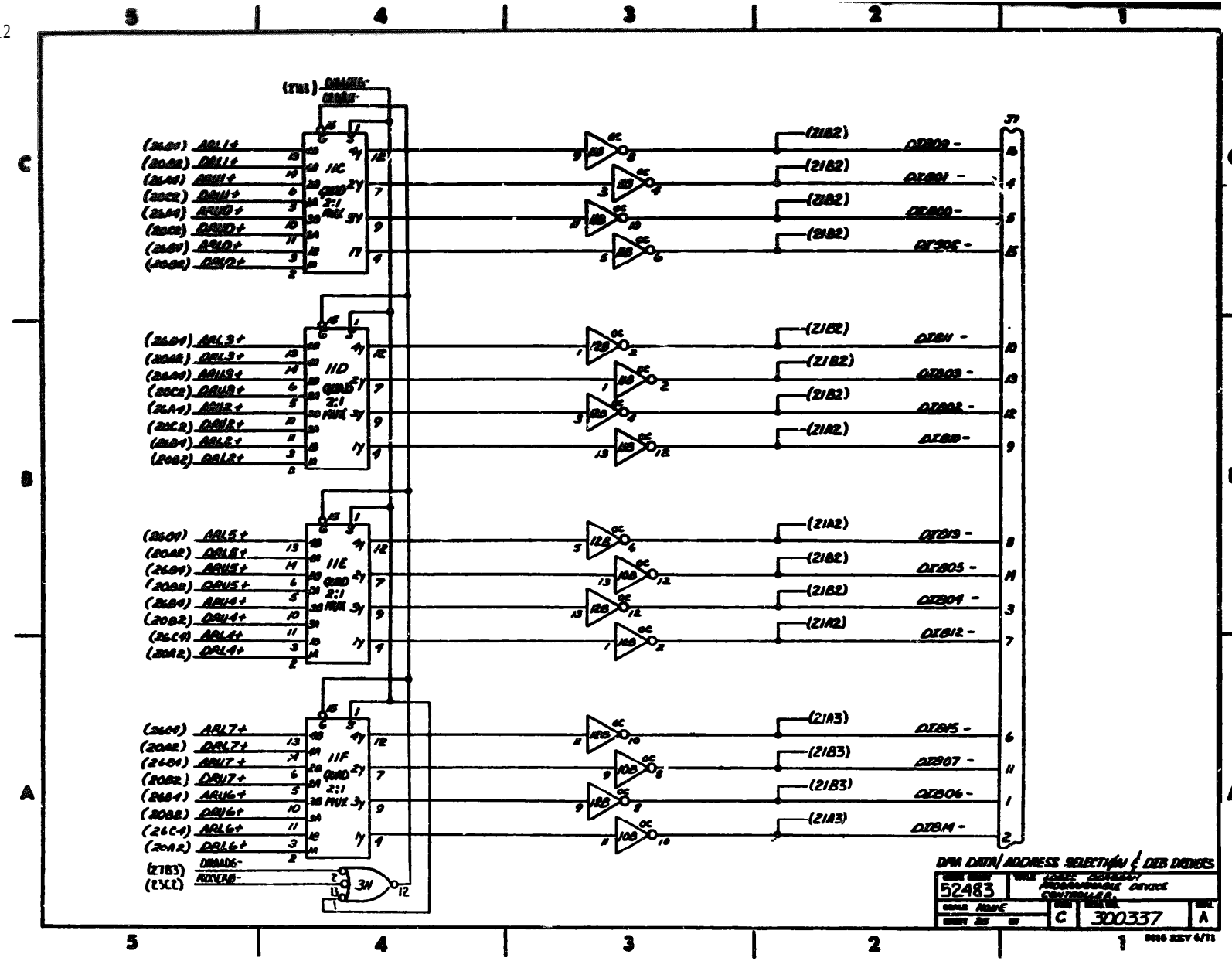

CPU COMMAND DECODING
52483
C
300337
B

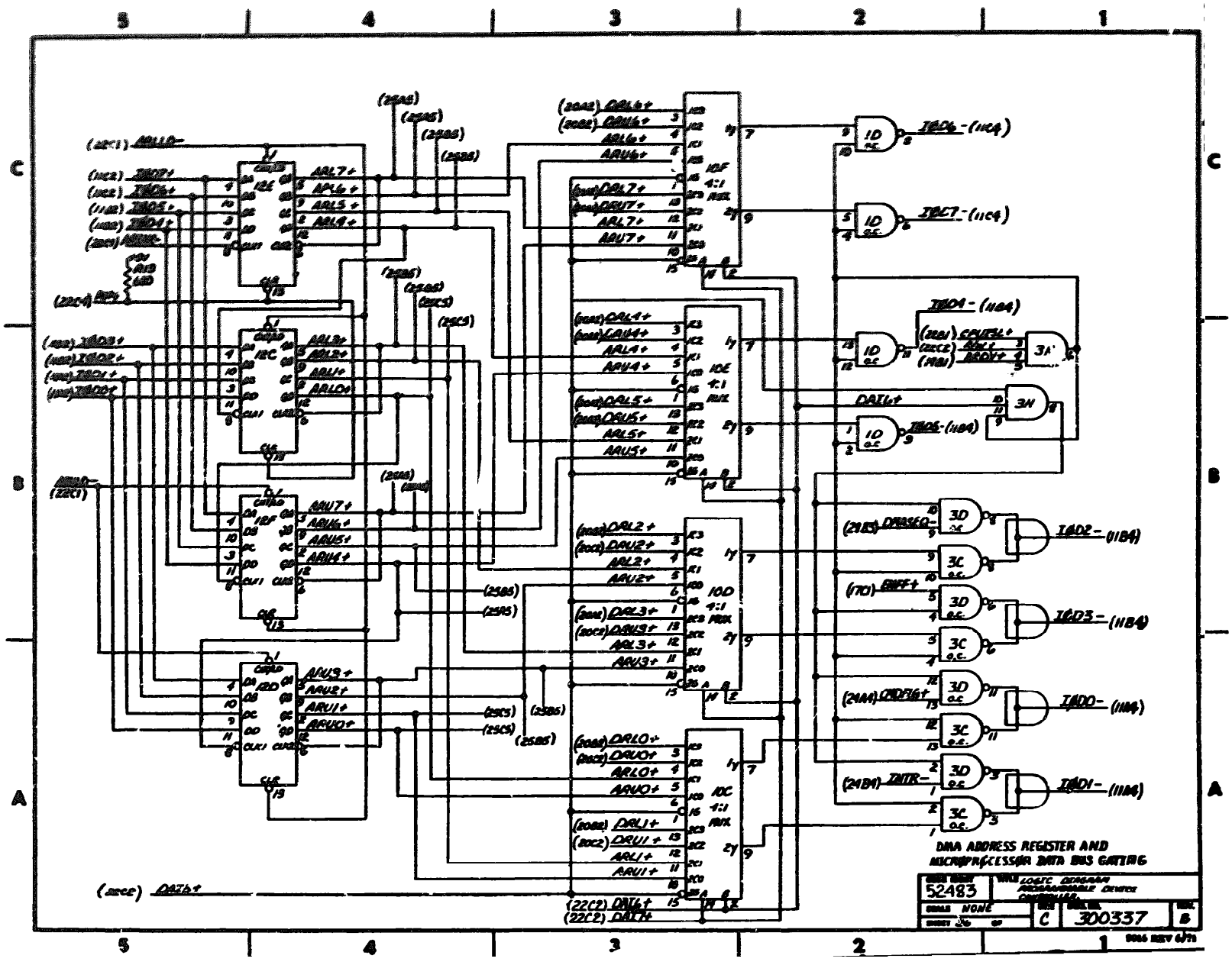


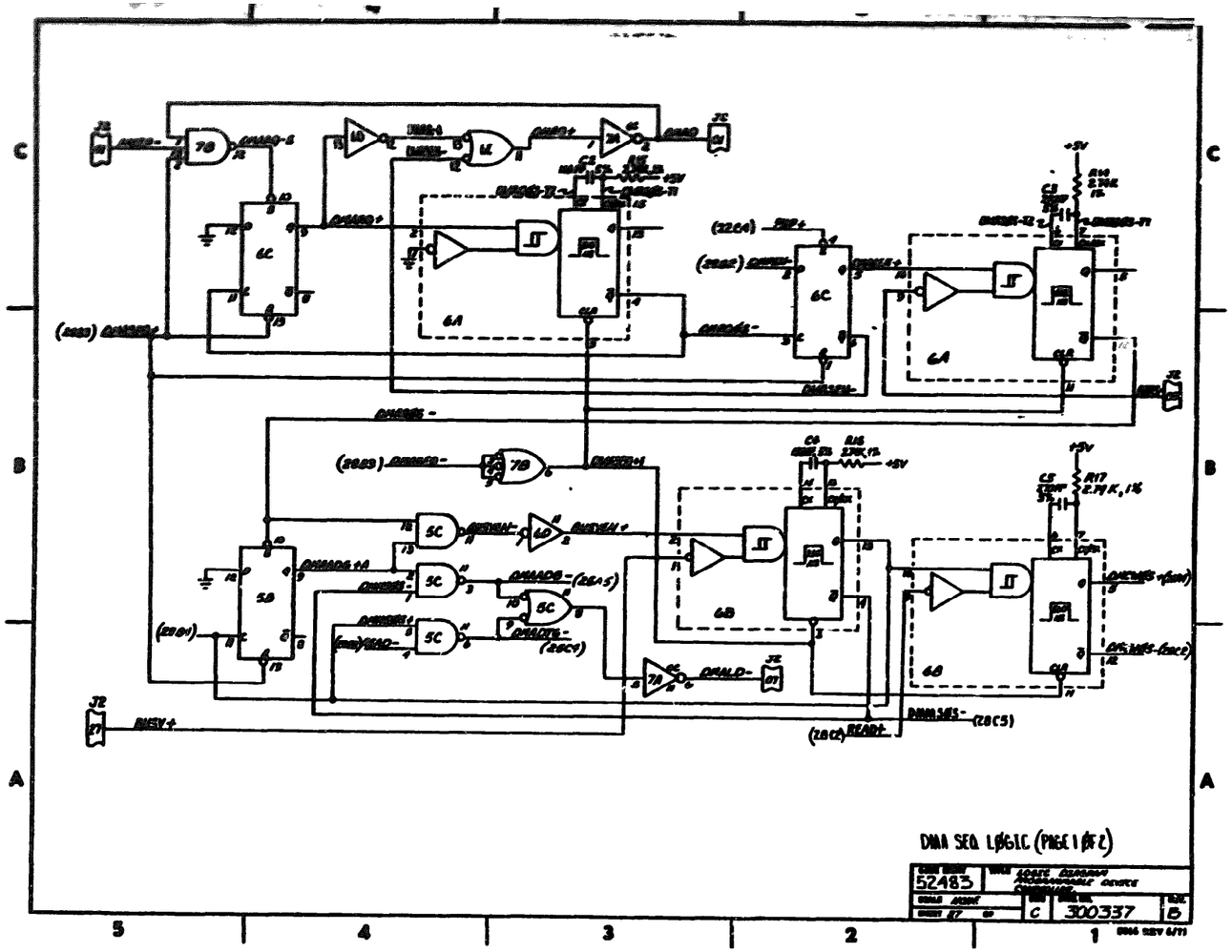
COMMAND EKØ LOGIC

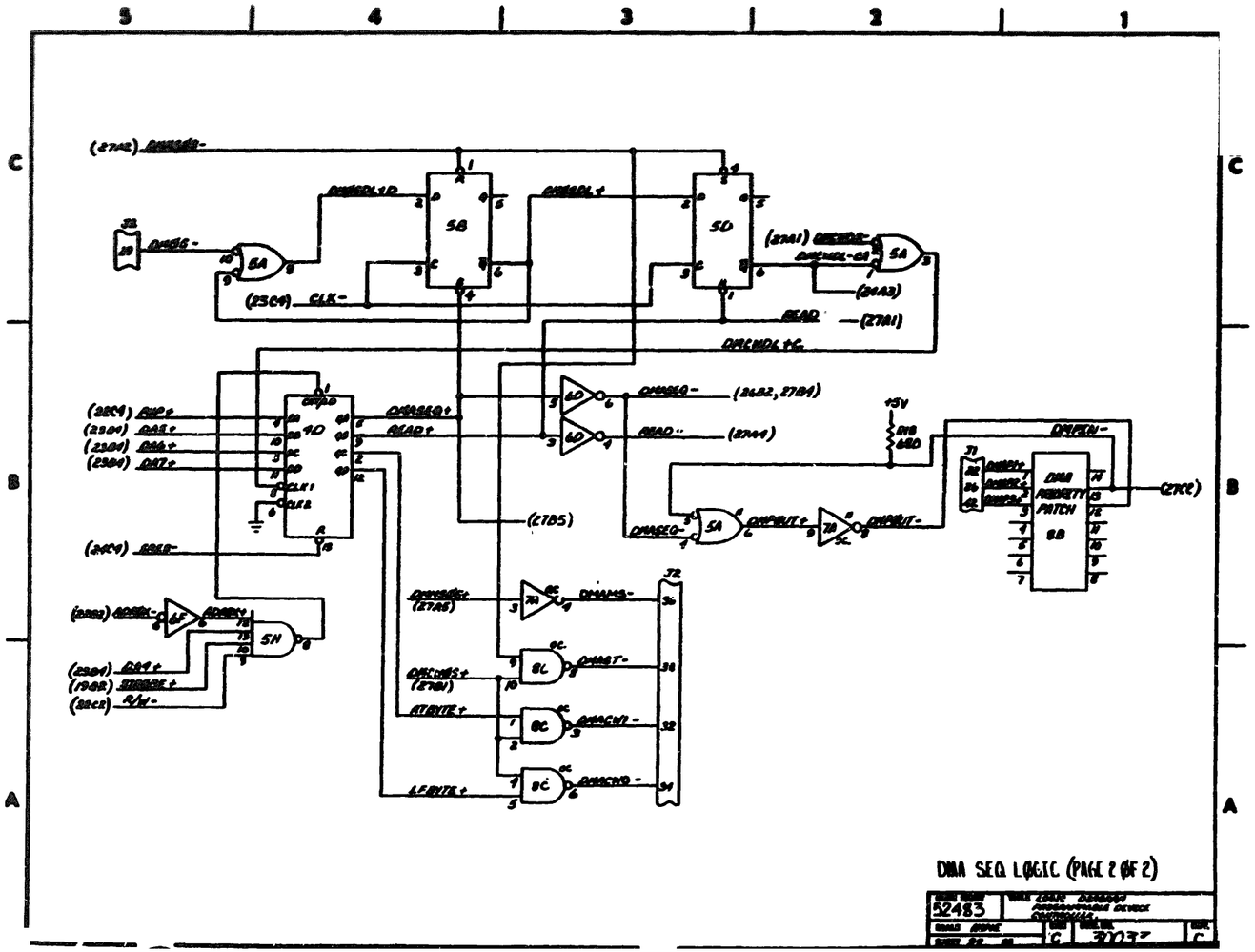
52483			
	C	300337	A

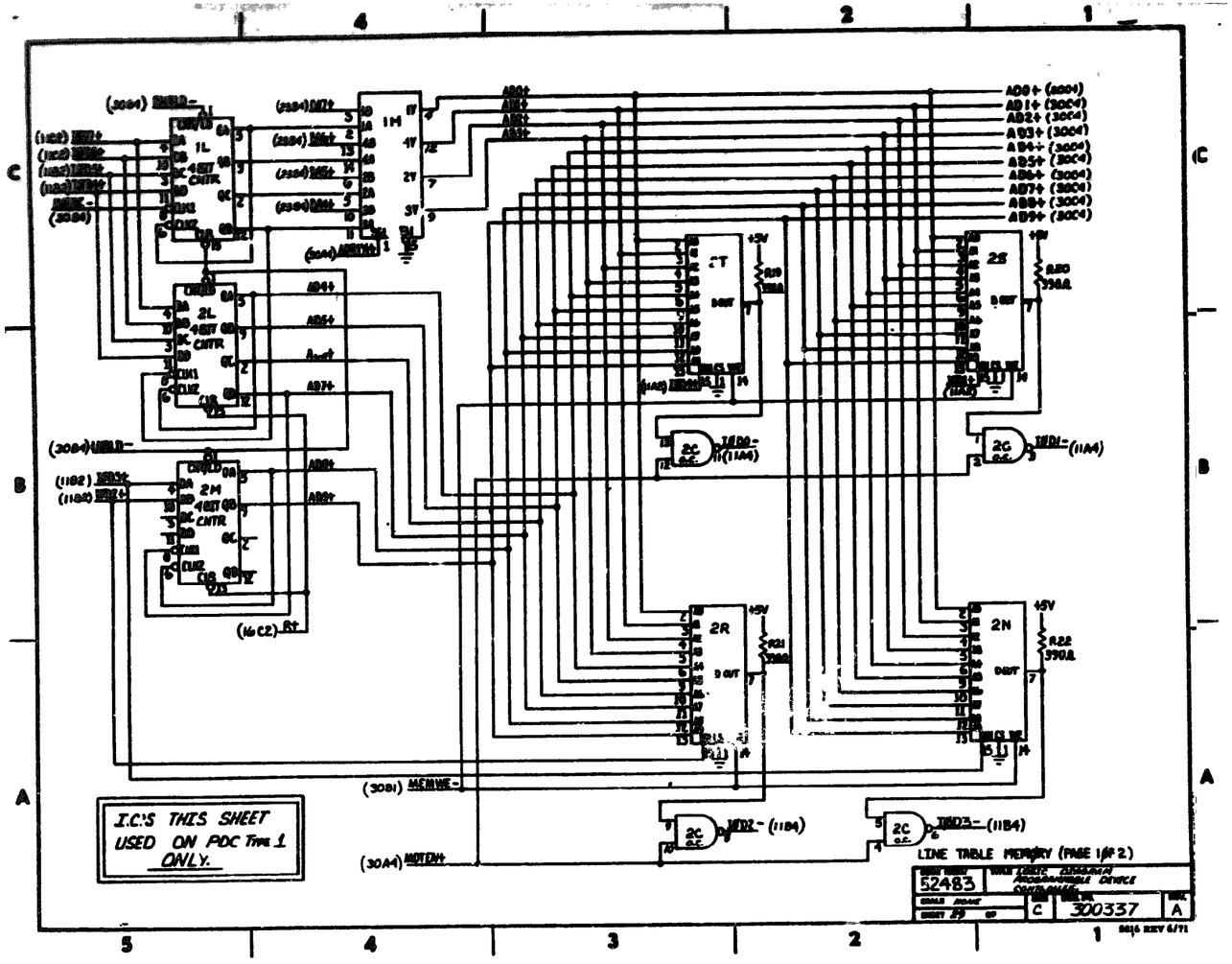

CPU INTERFALE CONTROL LOGIC
52483
300337
C
A
PDC Type 2 ONLY

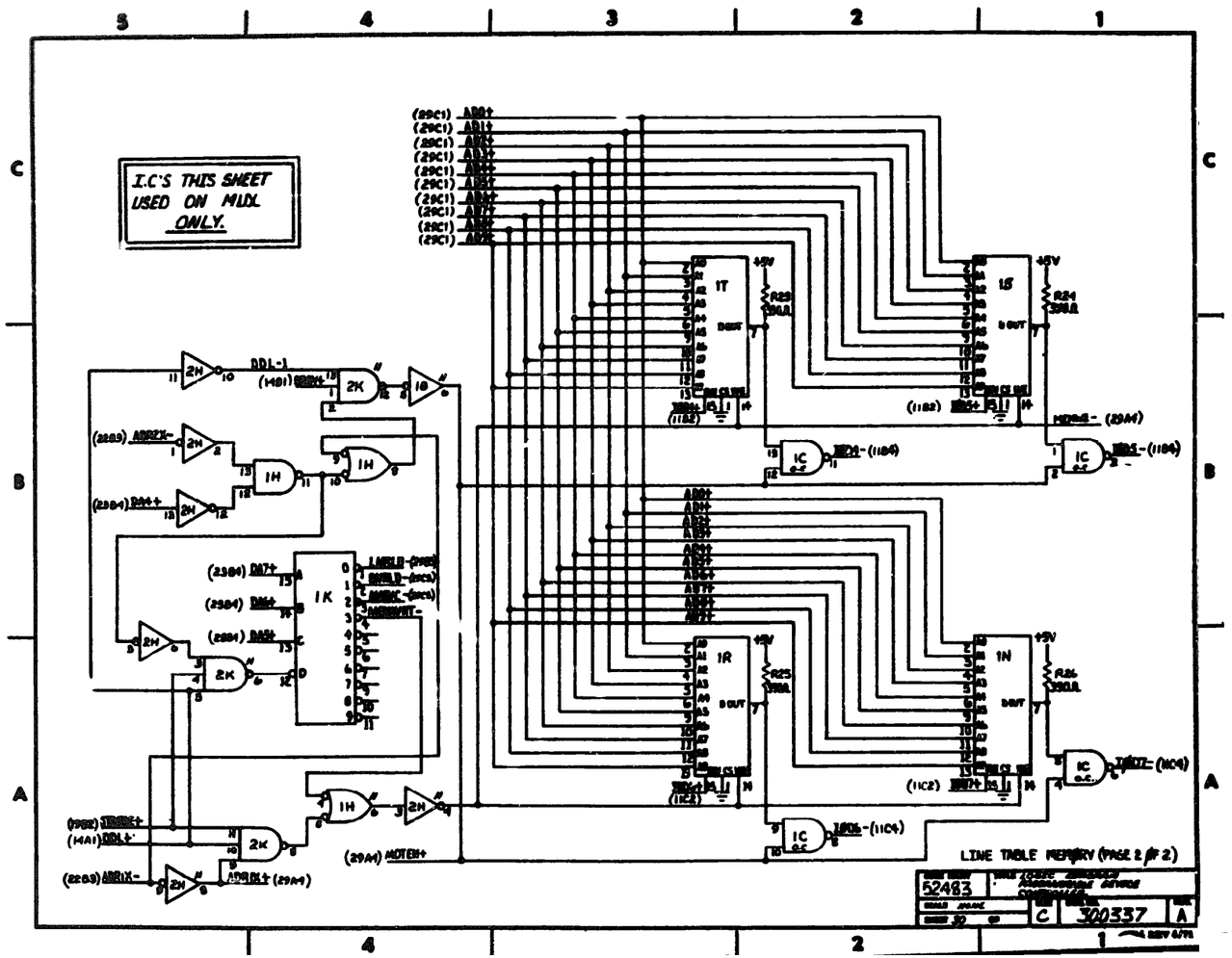

IIC
IID
IIE
IIF
QUAD 2:1 MUX
3W
J7
DIM DATA/ADDRESS SELECTION & DEB DRIVES
52483
C
300337
A

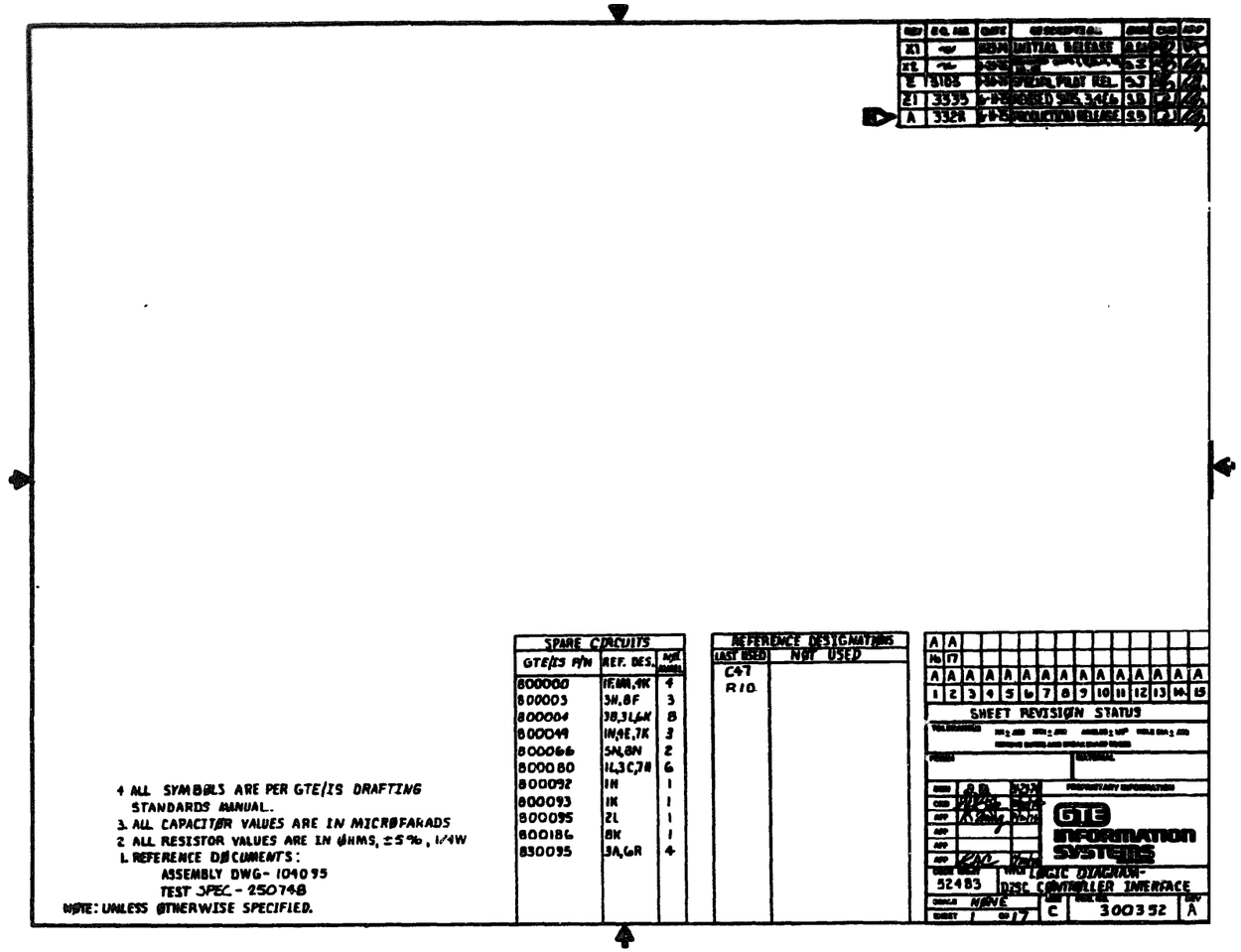

DMA ADDRESS REGISTER AND
MICROPROCESSOR DATA BUS GATING
52483
LOGIC DIAGRAM
NONE
C
300337
B


DMA SEQ LOGIC (PAGE 1 OF 2)
52483
300337
C
B
5
4
3
2
1


DMA SEQ LOGIC (PAGE 2 OF 2)
52483
C
3003?
C

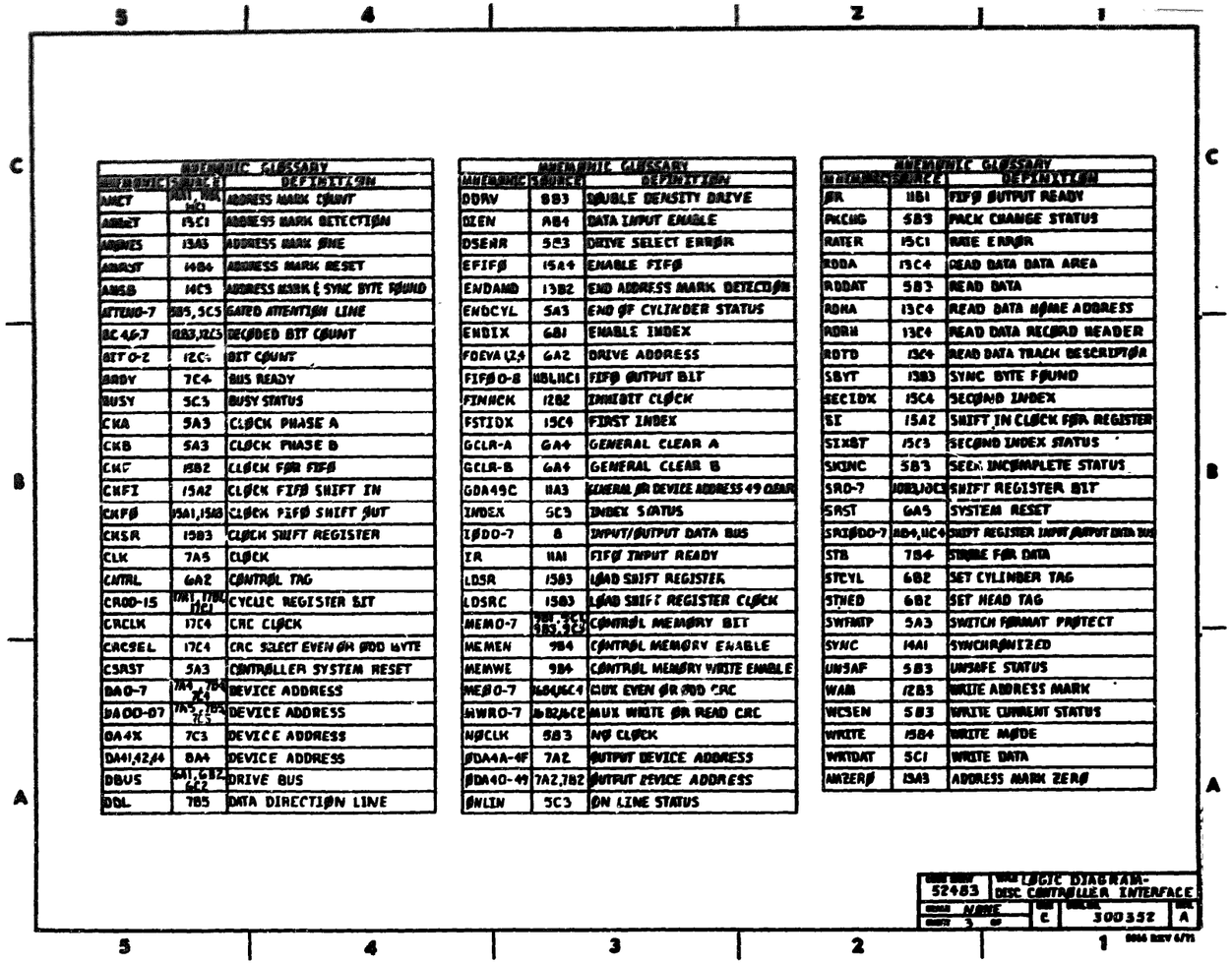

I.C.'S THIS SHEET
USED ON PDC Type 1
ONLY.
LINE TABLE MEMORY (PAGE 1 OF 2)
52483
300337
C
A


I.C.'S THIS SHEET USED ON MIDL ONLY.
LINE TABLE MEMORY (PAGE 2 OF 2)
52483
C
300337
A


SPARE CIRCUITS
GTE/IS P/N
REF. DES.
PIN NUMBER
800000 IE,MM,9K 4
800003 5H,8F 3
800004 3B,3L,6K 8
800049 IN,9E,7K 3
800066 5N,8N 2
800080 1L,3C,7B 6
800092 1N 1
800093 1K 1
800095 2L 1
800186 8K 1
830095 3A,6R 4
REFERENCE DESIGNATIONS
LAST USED
NOT USED
C47
R10
SHEET REVISION STATUS
GTE INFORMATION SYSTEMS
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
C
300352
A
4 ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
2 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
1. REFERENCE DOCUMENTS:
ASSEMBLY DWG- 104095
TEST SPEC - 250748
NOTE: UNLESS OTHERWISE SPECIFIED.

	A	B	C	D	E	F	H	K	L	M	N	R	
10	800173 74151	PATCH	800173 74151	SPARE	800062 74198		800006 7430	SPARE	SPARE		SPARE	SPARE	10
9	800173 74151	800066 7438	800173 74151	830096 PUP	800004 7404	800004 7404	800005 7420	SPARE	SPARE	SPARE	800004 7404	830095 TERM	9
8	800173 74151	800066 7438	800173 74151	800042 7489	800006 7430	800003 7410	800000 7400	800186 74221	800201 3351		800066 7438	800004 7404	8
7	800173 74151	800080 7408	800173 74151	800042 7489	800060 74154		800080 7408	800049 7474	800088 74175	800088 74175	800004 7404	830095 TERM	7
6	800004 7404	800168 7485	SPARE	800005 7420	800004 7404	800088 74175	800005 7420	800004 7404	800064 74157	800064 74157	800004 7404	830095 TERM	6
5	830095 TERM	800004 7404	800000 7400	800004 7404	SPARE	800005 7420	800006 7430	800000 7400	800064 74157	800064 74157	800066 7438	800066 7438	5
4	830095 TERM	800004 7404	800004 7404	800096 7442	800049 7474	800005 7420	800003 7410	800000 7400	800064 74157	800064 74157	800066 7438	800066 7438	4
3	830095 TERM	800004 7404	800080 7408	800052 74161	800092 74107	800092 74107	800003 7410	800186 74221	800004 7404	800088 74175	800088 74175	800044 7486	3
2	800049 7474	800088 74175	800088 74175	800092 74107	800049 7474	800003 7410	800006 7430	800049 7474	800095 7402	800088 74175	800088 74175	800044 7486	2
1	SPARE	800088 74175	800088 74175	800080 7408	SPARE	800000 7400	800092 74107	800093 74108	800080 7408	800000 7400	800049 7474	SPARE	1
	A	B	C	D	E	F	H	K	L	M	N	R	

CAGE NUMBER 52483	SIZE	TITLE LOGIC DIAGRAM- DISC CONTROLLER INTERFACE	
DRAWING NONE		C	300352 A
SHEET 2 OF			



MNEMONIC GLOSSARY

MNEMONIC	SHEET	DEFINITION
AMCT	7B1, 7B2, 7C1	ADDRESS MARK COUNT
AMDET	13C1	ADDRESS MARK DETECTION
AMDES	13A3	ADDRESS MARK DONE
AMRST	14B4	ADDRESS MARK RESET
AMSB	14C3	ADDRESS MARK & SYNC BYTE FOUND
ATTEN0-7	5B5, 5C5	GATED ATTENTION LINE
BC4,6,7	12B3, 12C5	DECODED BIT COUNT
BIT 0-2	12C3	BIT COUNT
BRDY	7C4	BUS READY
BUSY	5C3	BUSY STATUS
CKA	5A3	CLOCK PHASE A
CKB	5A3	CLOCK PHASE B
CKF	15B2	CLOCK FOR FIFO
CKFI	15A2	CLOCK FIFO SHIFT IN
CKFO	15A1, 15A8	CLOCK FIFO SHIFT OUT
CKSR	15B3	CLOCK SHIFT REGISTER
CLK	7A5	CLOCK
CNTRL	6A2	CONTROL TAG
CRC0-15	11A1, 11B1, 11C1	CYCLIC REGISTER BIT
CRCLK	17C4	CRC CLOCK
CRCSEL	17C4	CRC SELECT EVEN OR ODD BYTE
CSRST	5A3	CONTROLLER SYSTEM RESET
DA0-7	7A4, 7B4, 7C4	DEVICE ADDRESS
DADD-07	7A5, 7B5, 7C5	DEVICE ADDRESS
DA4X	7C3	DEVICE ADDRESS
DA41,42,44	8A4	DEVICE ADDRESS
DBUS	6A1, 6B2, 6C2	DRIVE BUS
DDL	7B5	DATA DIRECTION LINE

MNEMONIC GLOSSARY

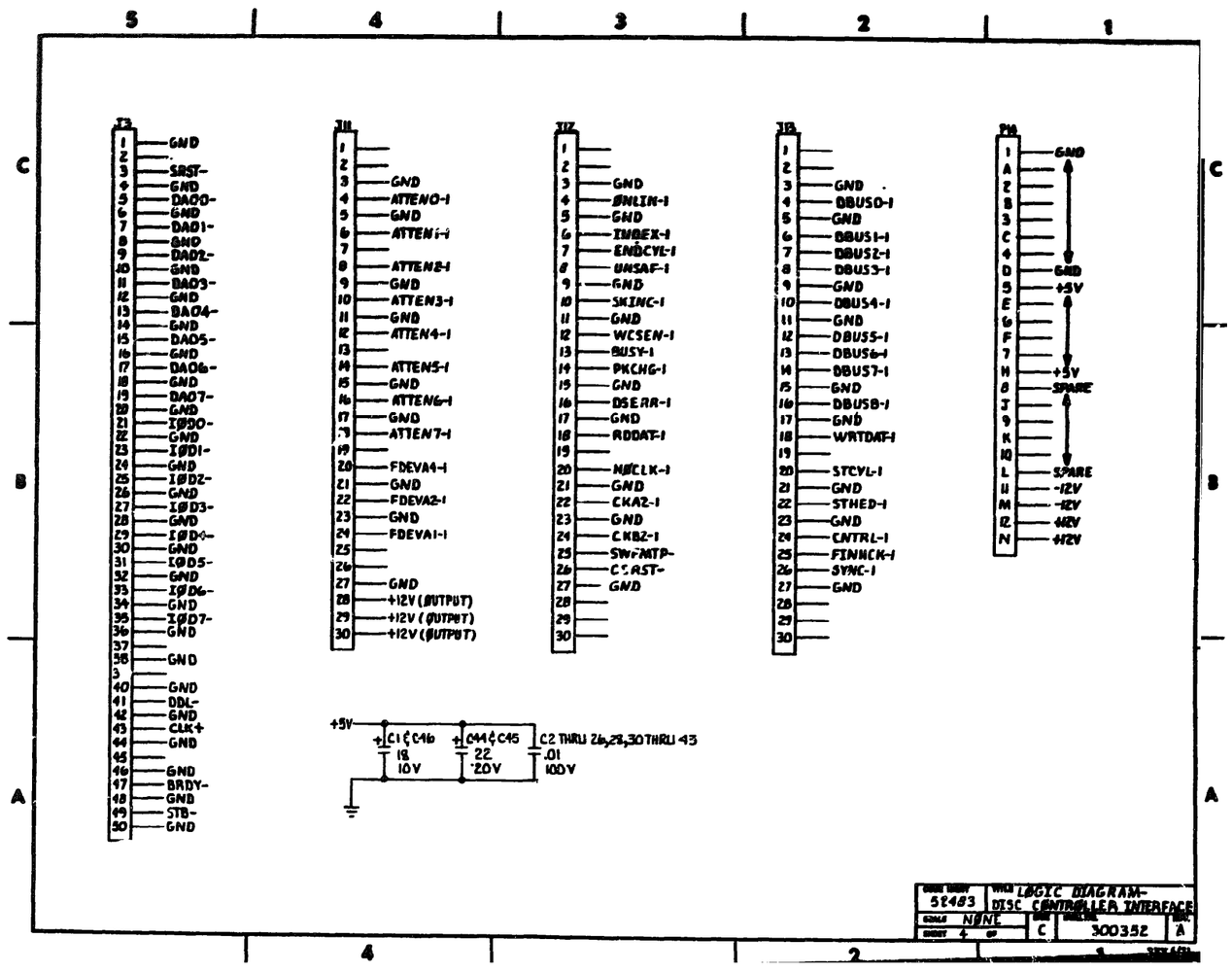
MNEMONIC	SHEET	DEFINITION
DDRV	9B3	DOUBLE DENSITY DRIVE
DIEN	4B4	DATA INPUT ENABLE
DSELR	5C3	DRIVE SELECT ERROR
EFIFO	15A4	ENABLE FIFO
ENDAMD	13B2	END ADDRESS MARK DETECTION
ENDCYL	5A3	END OF CYLINDER STATUS
ENDIX	6B1	ENABLE INDEX
FDEVA 1,2,4	6A2	DRIVE ADDRESS
FIFO 0-8	11B1, 11C1	FIFO OUTPUT BIT
FINACK	12B2	INHIBIT CLOCK
FSTIDX	15C4	FIRST INDEX
GCLR-A	6A4	GENERAL CLEAR A
GCLR-B	6A4	GENERAL CLEAR B
GDA49C	11A3	GENERAL OR DEVICE ADDRESS 49 CLEAR
INDEX	5C3	INDEX STATUS
IODO-7	8	INPUT/OUTPUT DATA BUS
IR	11A1	FIFO INPUT READY
LDSR	15B3	LOAD SHIFT REGISTER
LDSRC	15B3	LOAD SHIFT REGISTER CLOCK
MEM0-7	9B1, 9C1, 9B3, 9C3	CONTROL MEMORY BIT
MEMEN	9B4	CONTROL MEMORY ENABLE
MEMWE	9B4	CONTROL MEMORY WRITE ENABLE
MEO-7	4B4, 4C4	MUX EVEN OR ODD CRC
MWRO-7	4B2, 4C2	MUX WRITE OR READ CRC
NOCLK	5B3	NO CLOCK
ODA4A-4F	7A2	OUTPUT DEVICE ADDRESS
ODA40-49	7A2, 7B2	OUTPUT DEVICE ADDRESS
ONLIN	5C3	ON LINE STATUS

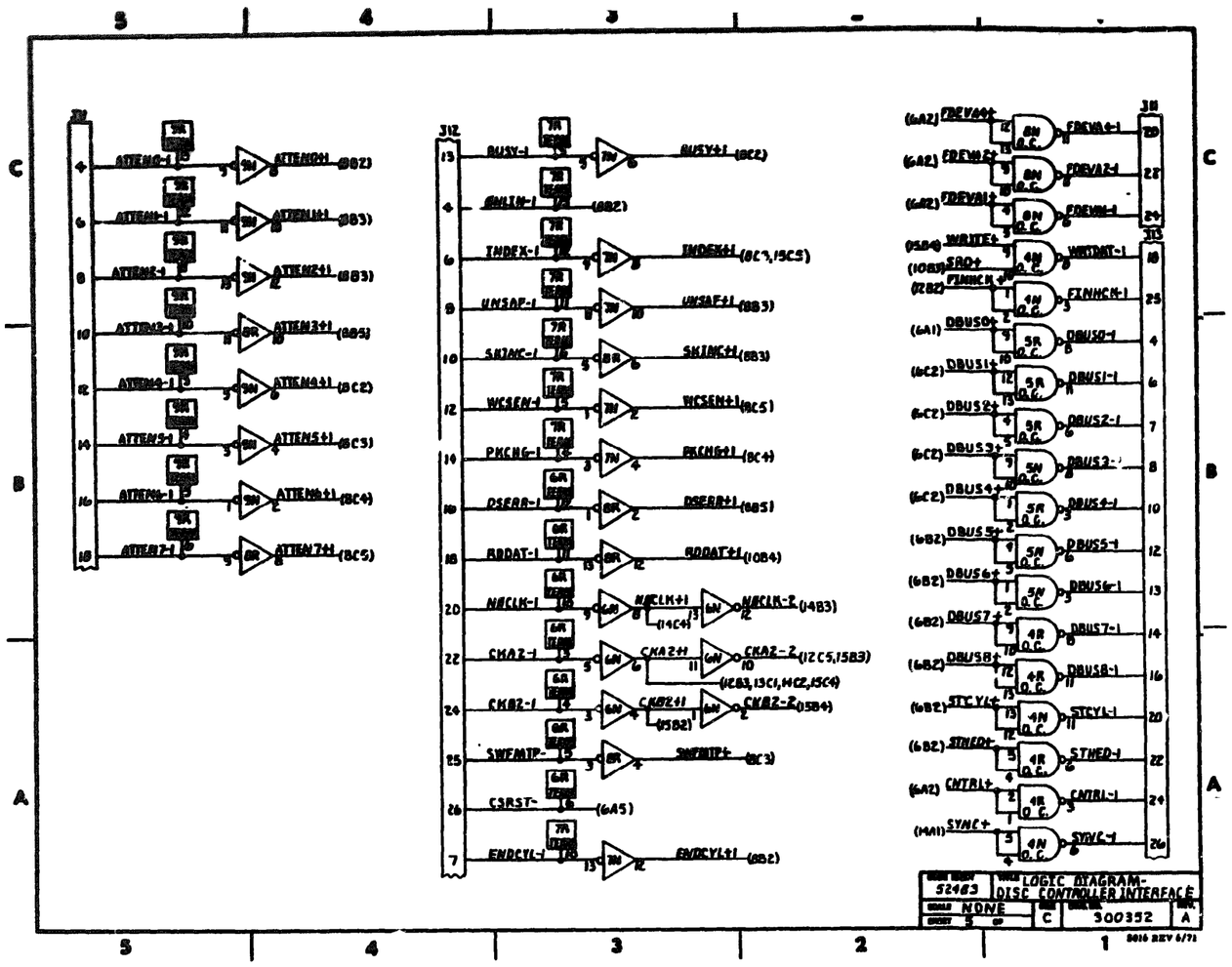
MNEMONIC GLOSSARY

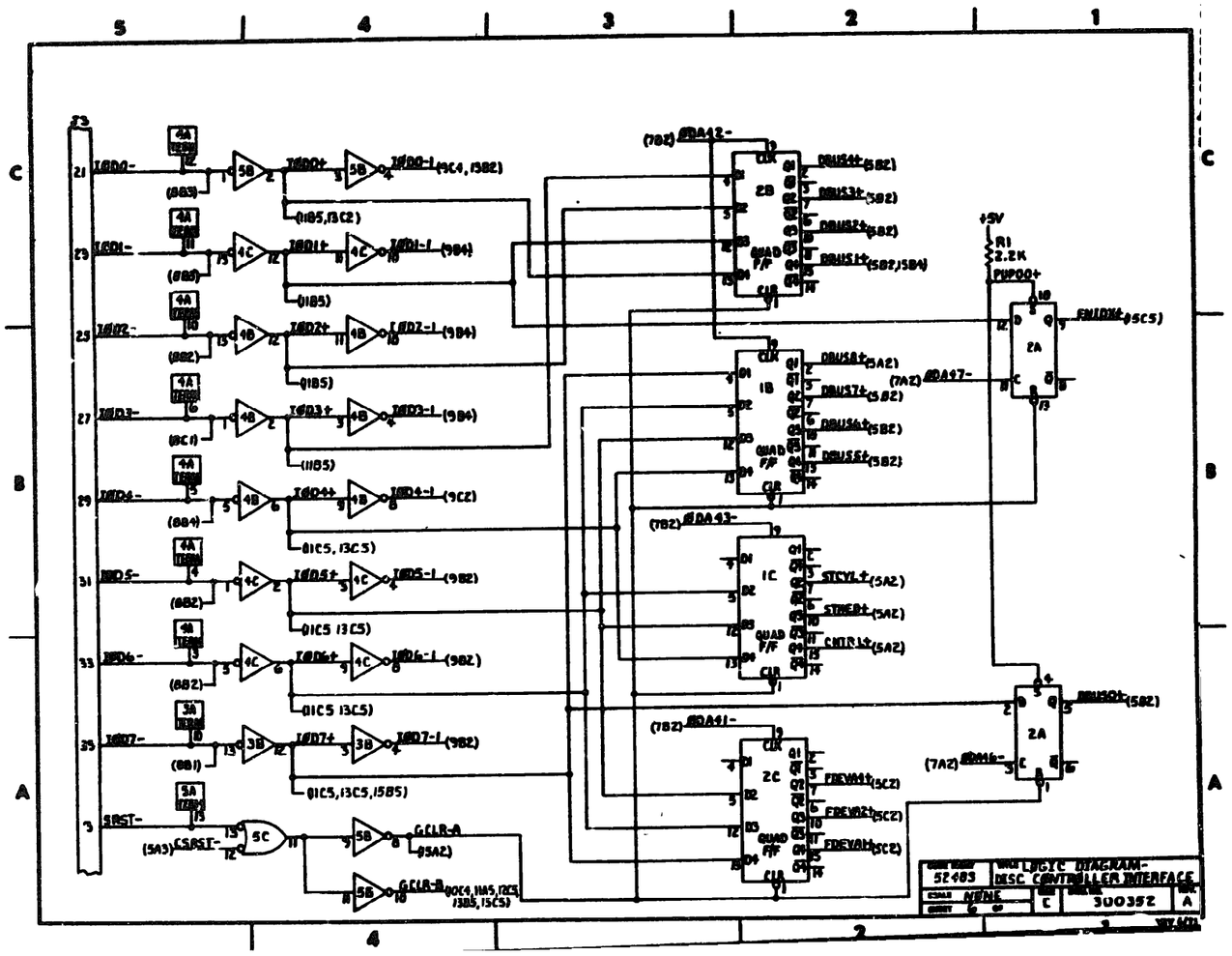
MNEMONIC	SHEET	DEFINITION
OR	11B1	FIFO OUTPUT READY
PKCHG	5B3	PACK CHANGE STATUS
RATER	15C1	RATE ERROR
RDDA	13C4	READ DATA DATA AREA
RDDAT	5B3	READ DATA
RDHA	13C4	READ DATA HOME ADDRESS
RDRH	13C4	READ DATA RECORD HEADER
RDTD	13C4	READ DATA TRACK DESCRIPTOR
SBYT	13B3	SYNC BYTE FOUND
SECIDX	15C4	SECOND INDEX
SI	15A2	SHIFT IN CLOCK FOR REGISTER
SIXST	15C3	SECOND INDEX STATUS
SKINC	5B3	SEEK INCOMPLETE STATUS
SRO-7	10B1, 10C1	SHIFT REGISTER BIT
SRST	6A5	SYSTEM RESET
SRIODO-7	8B4, 11C4	SHIFT REGISTER INPUT/OUTPUT DATA BUS
STB	7B4	STROBE FOR DATA
STCYL	6B2	SET CYLINDER TAG
STHED	6B2	SET HEAD TAG
SWFMTP	5A3	SWITCH FORMAT PROTECT
SYNC	14A1	SYNCHRONIZED
UNSAF	5B3	UNSAFE STATUS
WAM	12B3	WRITE ADDRESS MARK
WCSEN	5B3	WRITE CURRENT STATUS
WRITE	15B4	WRITE MODE
WRTDAT	5C1	WRITE DATA
AMZERO	13A3	ADDRESS MARK ZERO

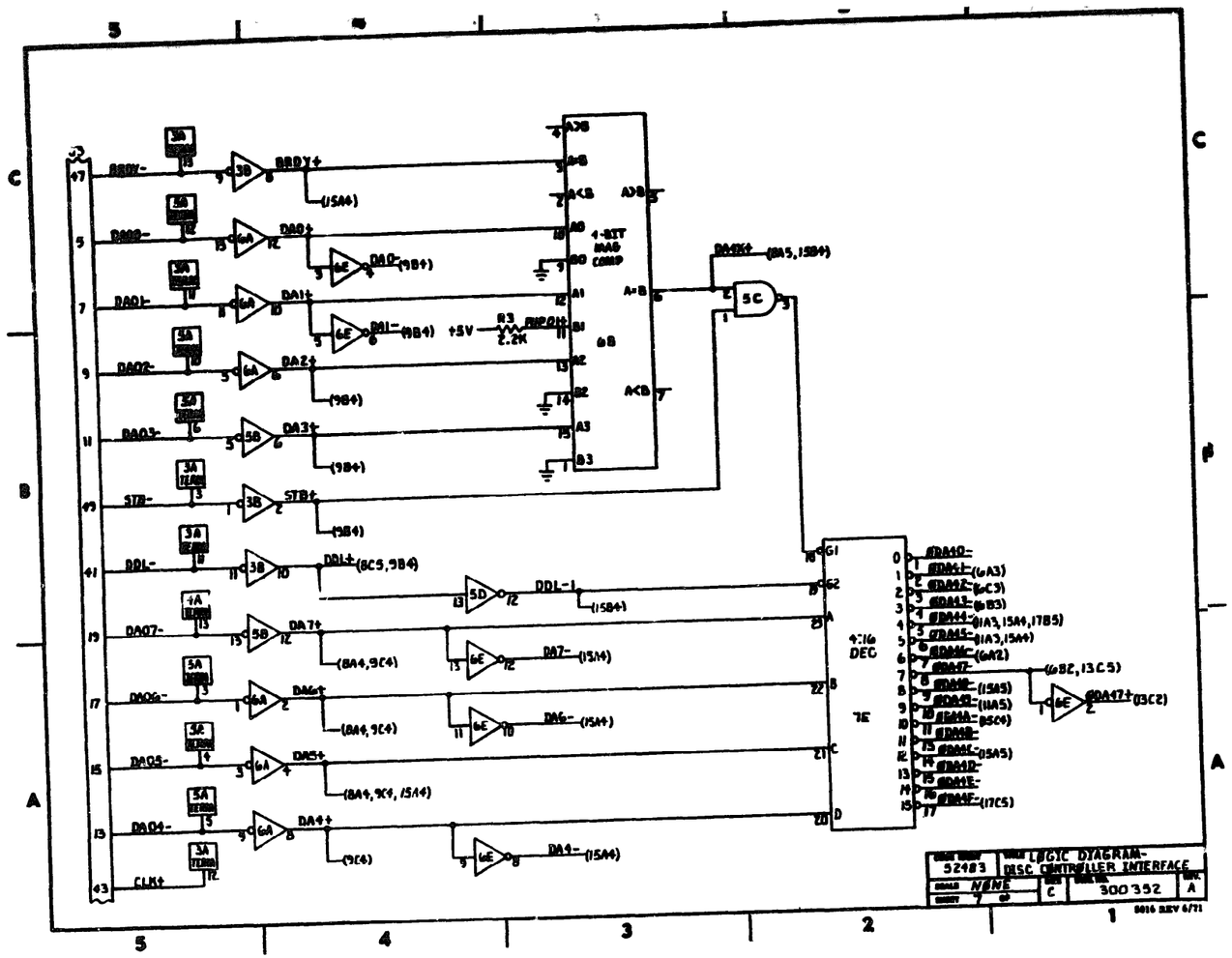
DWG NUMBER 52483	TITLE LOGIC DIAGRAM- DISC CONTROLLER INTERFACE		
DESIGN NAME	SHEET 3 OF	SIZE C	DRAWING 300352 REV A

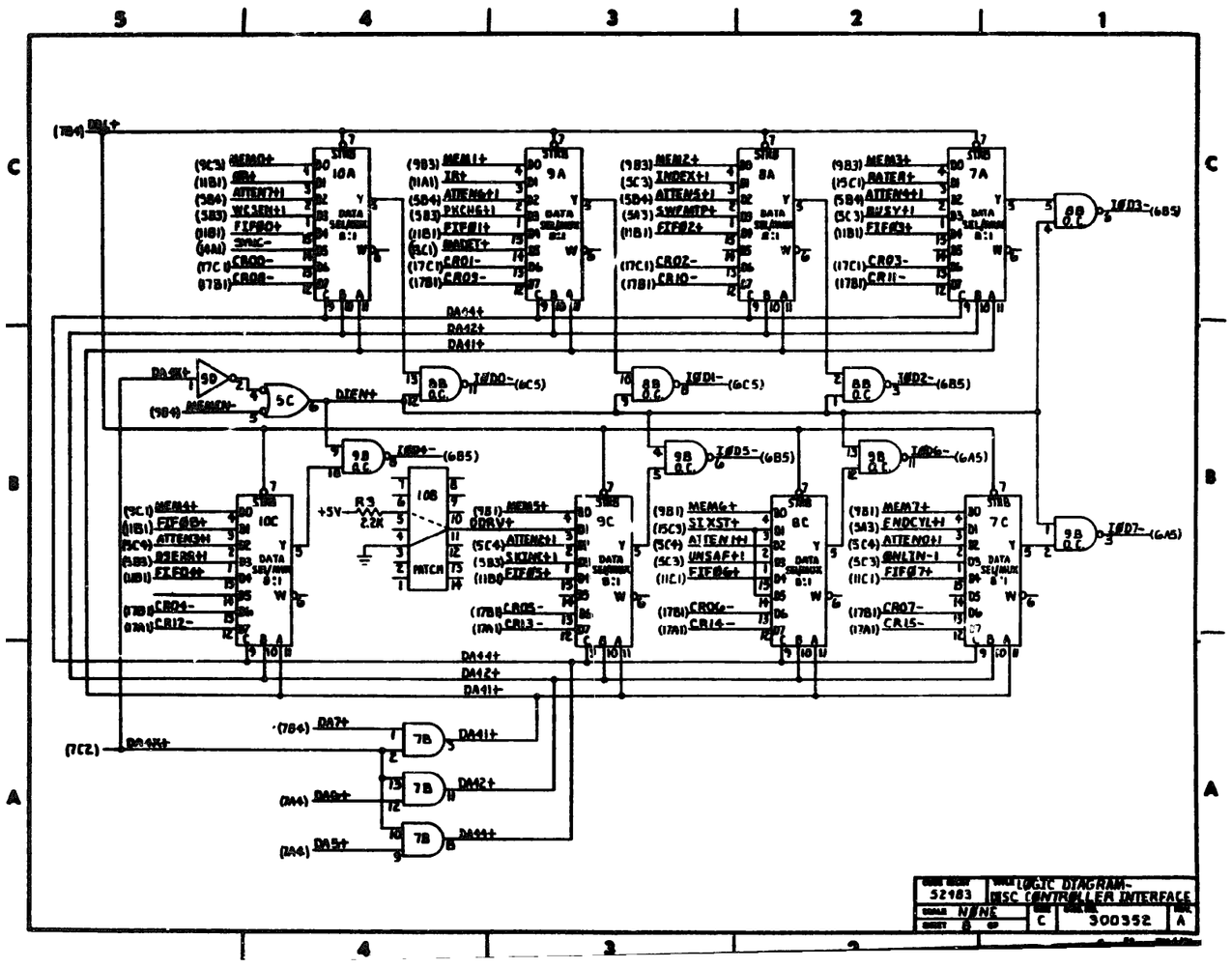
8086 REV 6/75

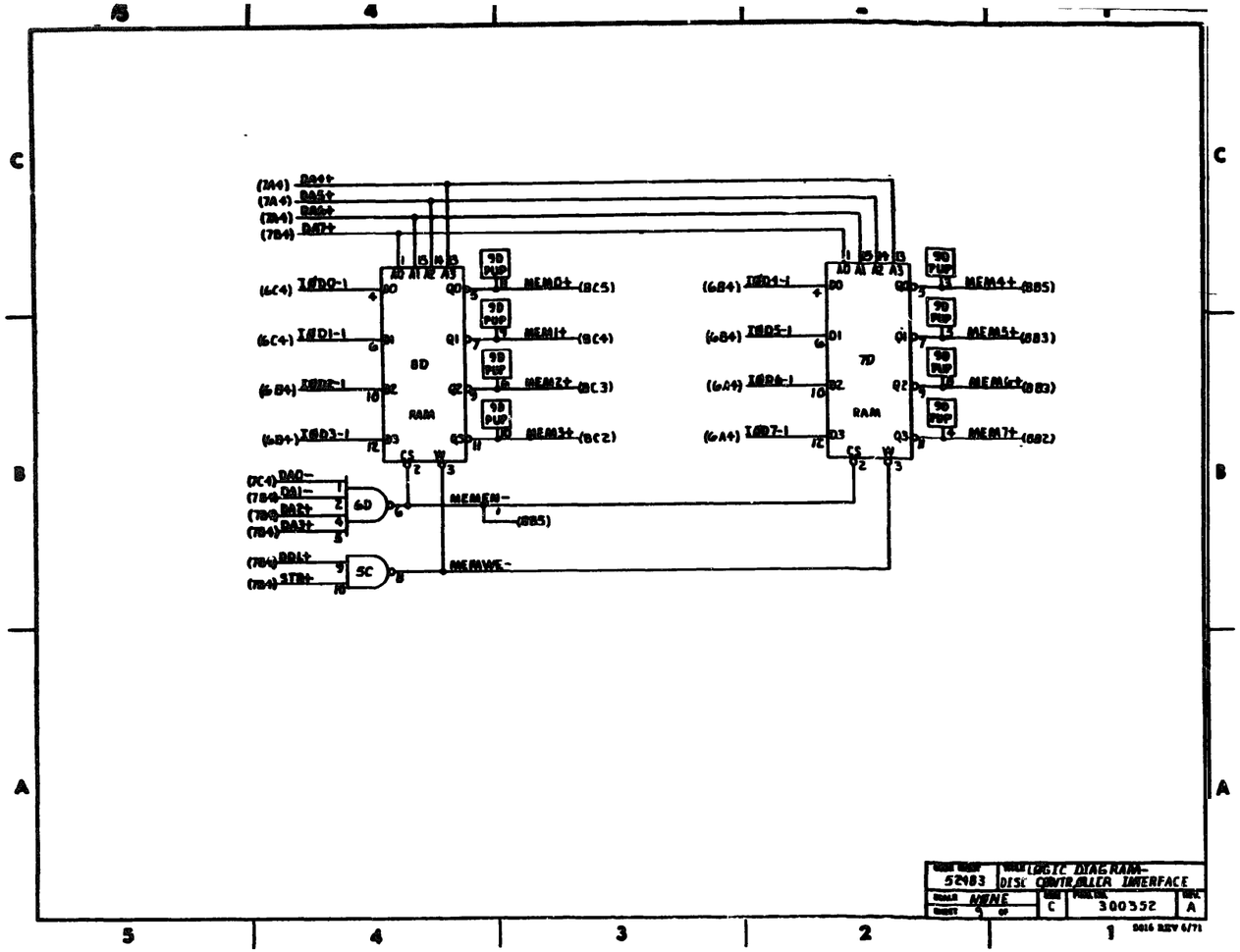

5
4
3
2
1
C
B
A
J3
1 GND
2
3 SRST-
4 GND
5 DAO0-
6 GND
7 DAO1-
8 GND
9 DAO2-
10 GND
11 DAO3-
12 GND
13 DAO4-
14 GND
15 DAO5-
16 GND
17 DAO6-
18 GND
19 DAO7-
20 GND
21 IØDO-
22 GND
23 IØD1-
24 GND
25 IØD2-
26 GND
27 IØD3-
28 GND
29 IØD4-
30 GND
31 IØD5-
32 GND
33 IØD6-
34 GND
35 IØD7-
36 GND
37
38 GND
39
40 GND
41 DDL-
42 GND
43 CLK+
44 GND
45
46 GND
47 BRDY-
48 GND
49 STB-
50 GND
J11
1
2
3 GND
4 ATTEN0-1
5 GND
6 ATTEN1-1
7
8 ATTEN2-1
9 GND
10 ATTEN3-1
11 GND
12 ATTEN4-1
13
14 ATTEN5-1
15 GND
16 ATTEN6-1
17 GND
18 ATTEN7-1
19
20 FDEVA4-1
21 GND
22 FDEVA2-1
23 GND
24 FDEVA1-1
25
26
27 GND
28 +12V (OUTPUT)
29 +12V (OUTPUT)
30 +12V (OUTPUT)
J12
1
2
3 GND
4 BNLIN-1
5 GND
6 INDEX-1
7 ENDCYL-1
8 UNSAF-1
9 GND
10 SKINC-1
11 GND
12 WCSEN-1
13 BUSY-1
14 PKCHG-1
15 GND
16 DSERR-1
17 GND
18 RDDAT-1
19
20 NRCLK-1
21 GND
22 CKA2-1
23 GND
24 CKB2-1
25 SWFMTP-
26 CSRST-
27 GND
28
29
30
J13
1
2
3 GND
4 DBUS0-1
5 GND
6 DBUS1-1
7 DBUS2-1
8 DBUS3-1
9 GND
10 DBUS4-1
11 GND
12 DBUS5-1
13 DBUS6-1
14 DBUS7-1
15 GND
16 DBUSB-1
17 GND
18 WRTDAT-1
19
20 STCYL-1
21 GND
22 STHED-1
23 GND
24 CNTRL-1
25 FINNCH-1
26 SYNC-1
27 GND
28
29
30
P14
1 GND
A
2
B
3
C
4
D GND
5 +5V
E
6
F
7
H +5V
8 SPARE
J
9
K
10
L SPARE
11 -12V
M -12V
12 +12V
N +12V
+5V
+ C1 ≠ C46 18 10V
+ C44 ≠ C45 22 20V
C2 THRU 26,28,30 THRU 43 .01 100V
SIZE 52483
TITLE LOGIC DIAGRAM- DISC CONTROLLER INTERFACE
SCALE NONE
SHEET 4 OF
DWG NO 300352
REV A

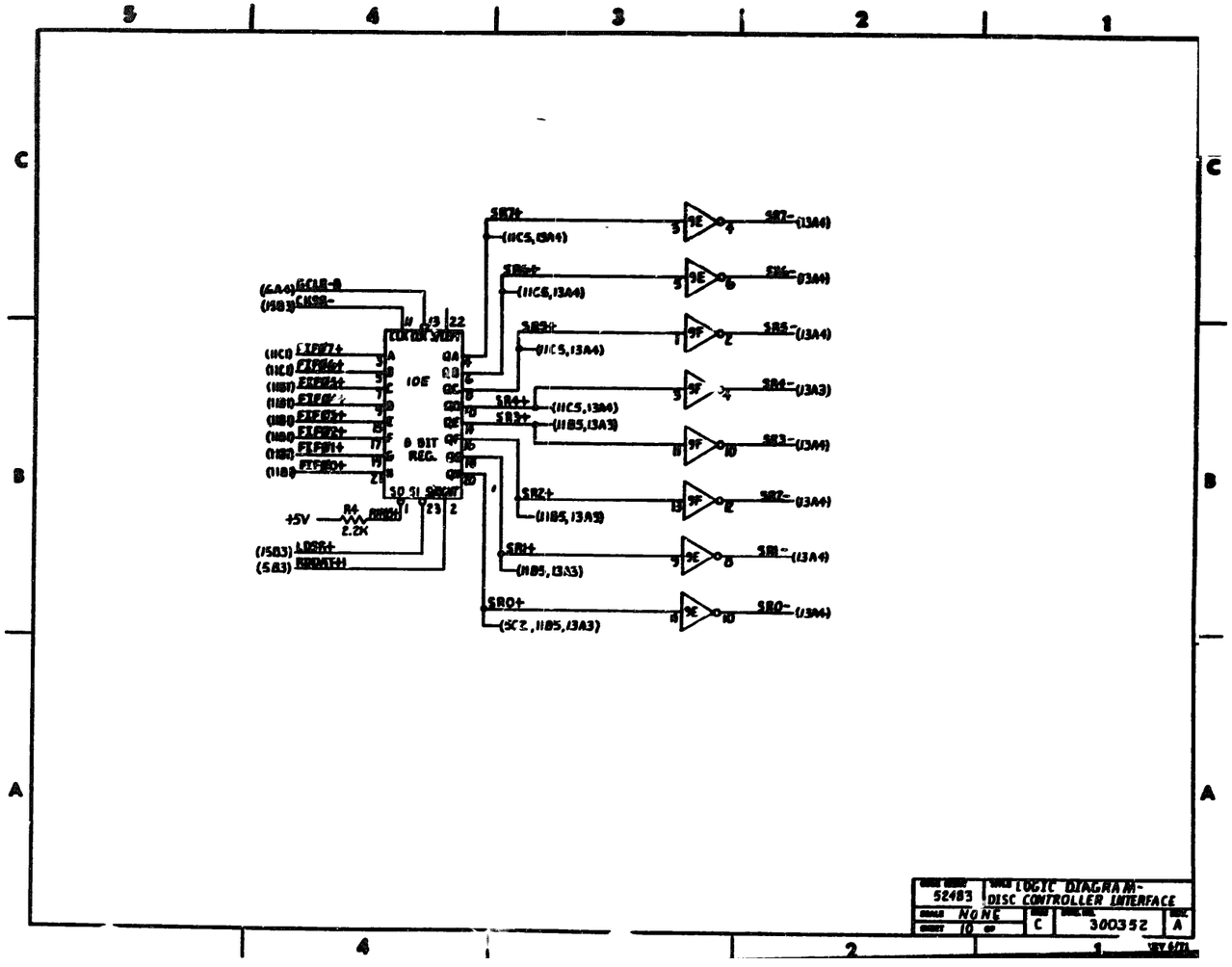

LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
C
300352
A

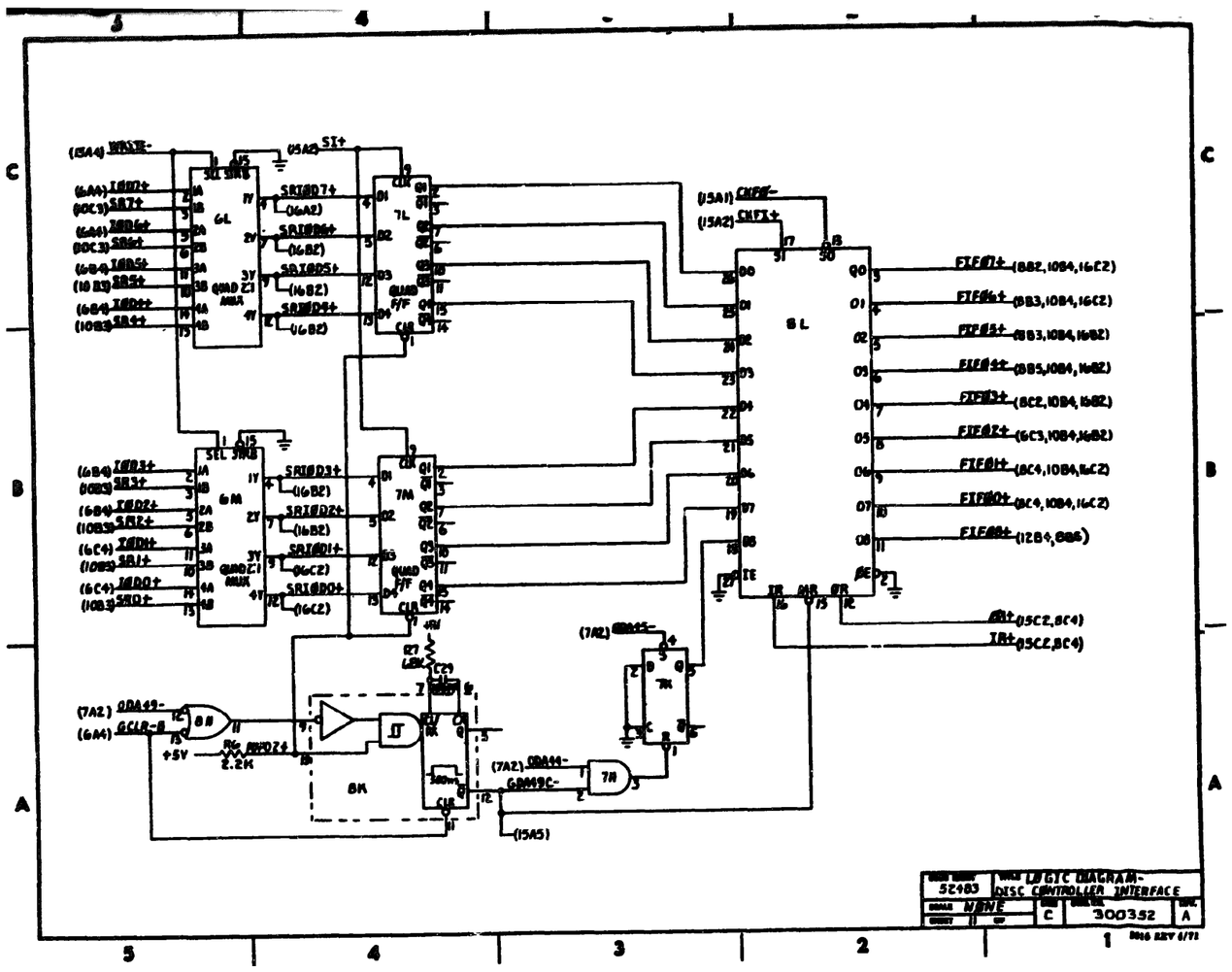

5
4
3
2
1
C
B
A
J3
IØD0-
IØD0+
IØD0-I
IØD1-
IØD1+
IØD1-I
IØD2-
IØD2+
IØD2-I
IØD3-
IØD3+
IØD3-I
IØD4-
IØD4+
IØD4-I
IØD5-
IØD5+
IØD5-I
IØD6-
IØD6+
IØD6-I
IØD7-
IØD7+
IØD7-I
SRST-
CSRST-
G.CLR-A
G.CLR-B
4A
4B
4C
5A
5B
5C
5B
3B
1B
2B
1C
2C
2A
1A
QUAD F/F
CLR
CLK
+5V
R1
2.2K
PUPOO+
FNIDIR
DBUS0+
DBUS1+
DBUS2+
DBUS3+
DBUS4+
DBUS5+
DBUS6+
DBUS7+
STCYL+
STREQ+
CNTRL+
FREVM1+
FREVM2+
FREVM+
DBUS01+
SYSCYC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
300352
A

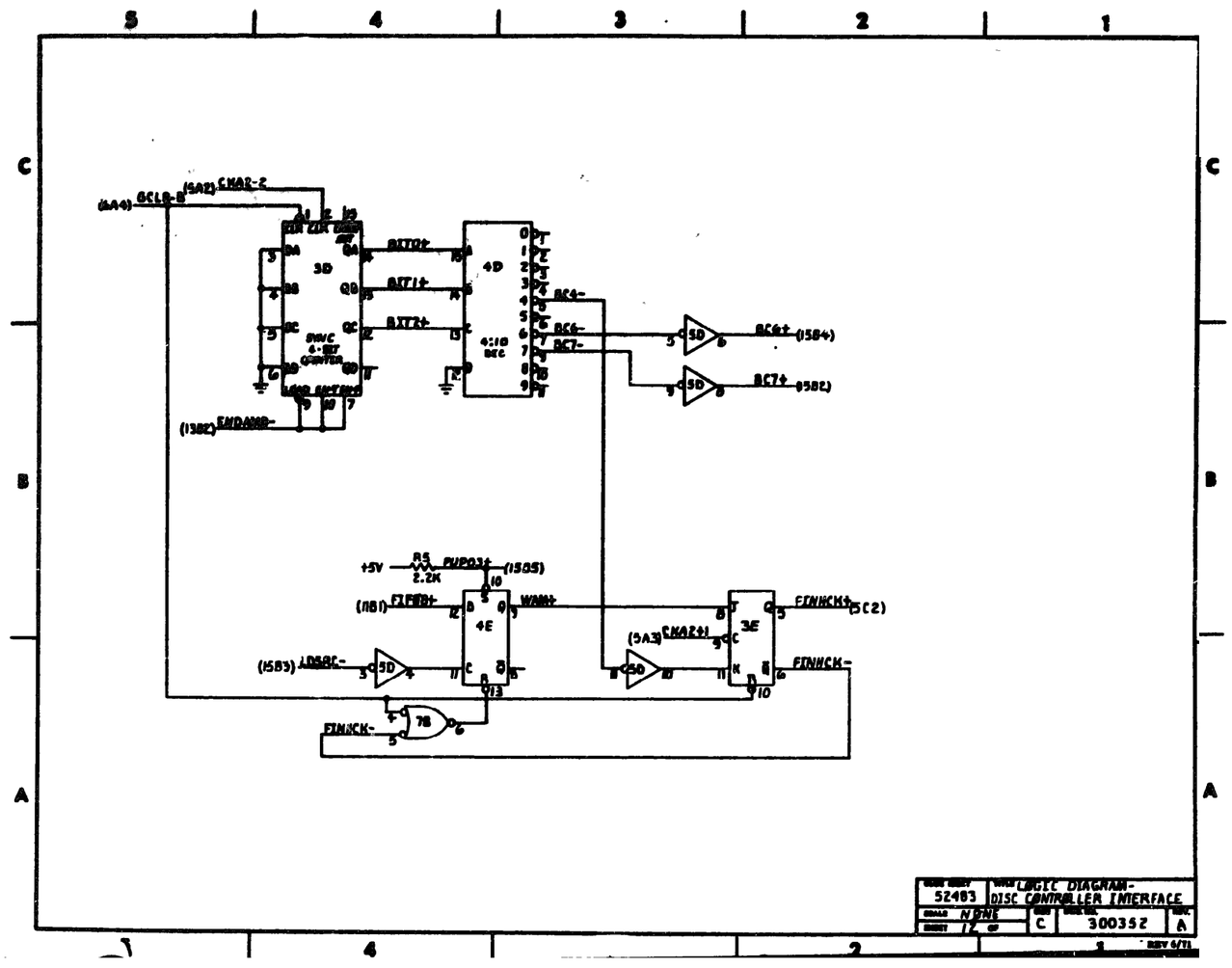

DA00-
DA01-
DA02-
DA03-
STB-
DDL-
DA07-
DA06-
DA05-
DA04-
CLK+
4-BIT MAG COMP
A=B
A<B
6B
5C
4:16 DEC
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
C
300392
A

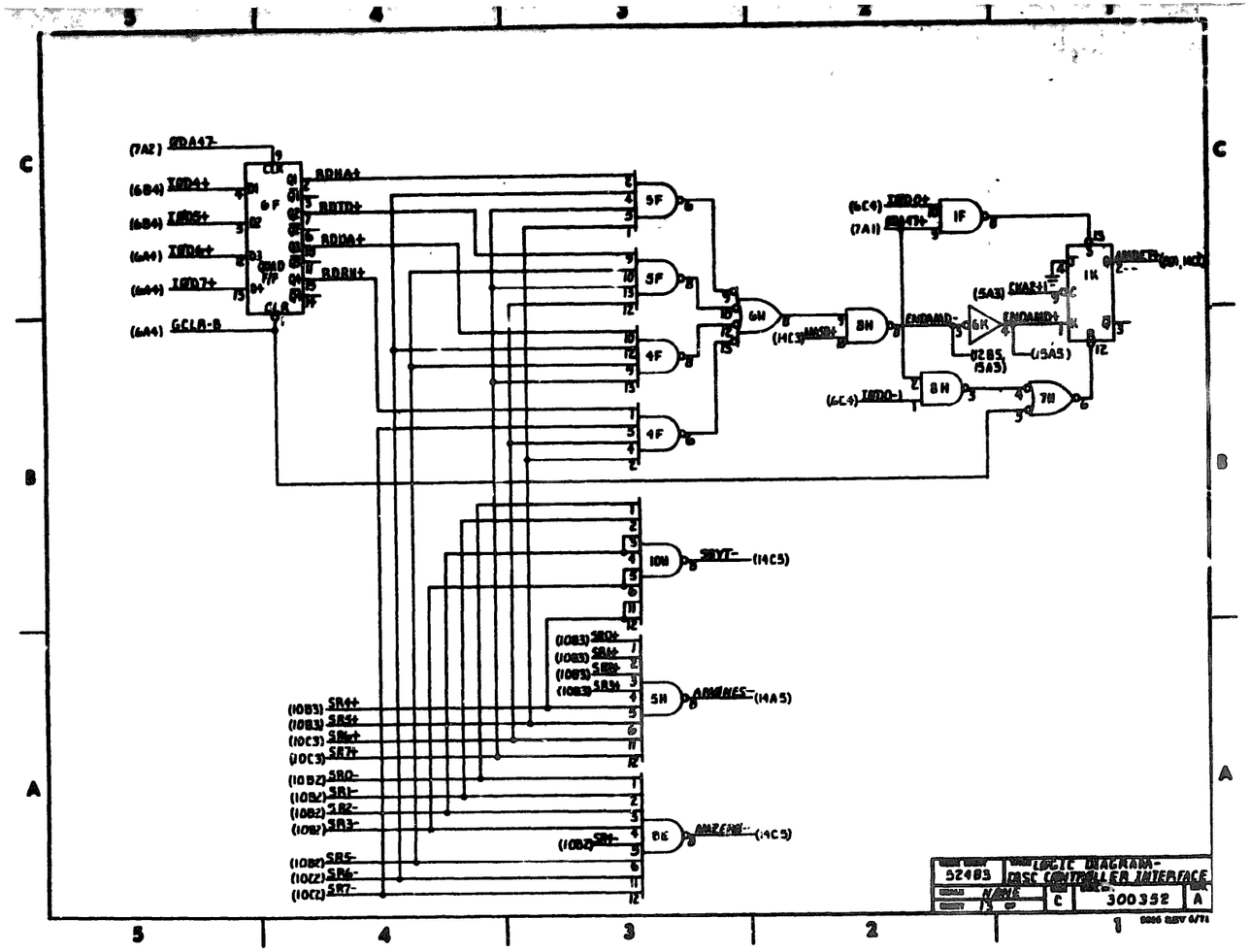

5
4
3
2
1
C
B
A
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52983
NONE
C
300352
A

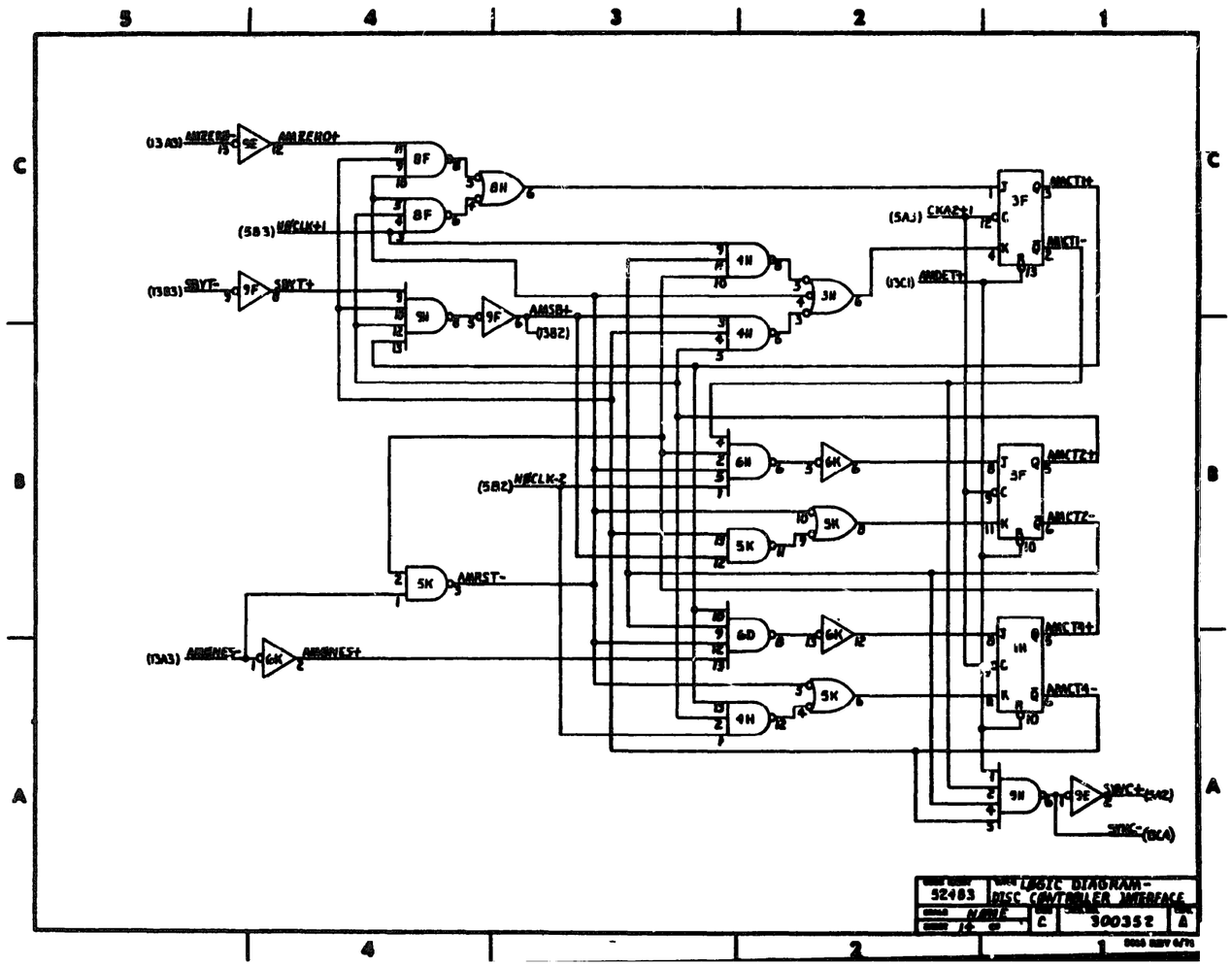

8D
RAM
7D
RAM
6D
5C
MEMEN-
MEMWE-
MEM0+
MEM1+
MEM2+
MEM3+
MEM4+
MEM5+
MEM6+
MEM7+
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
C
300352
A

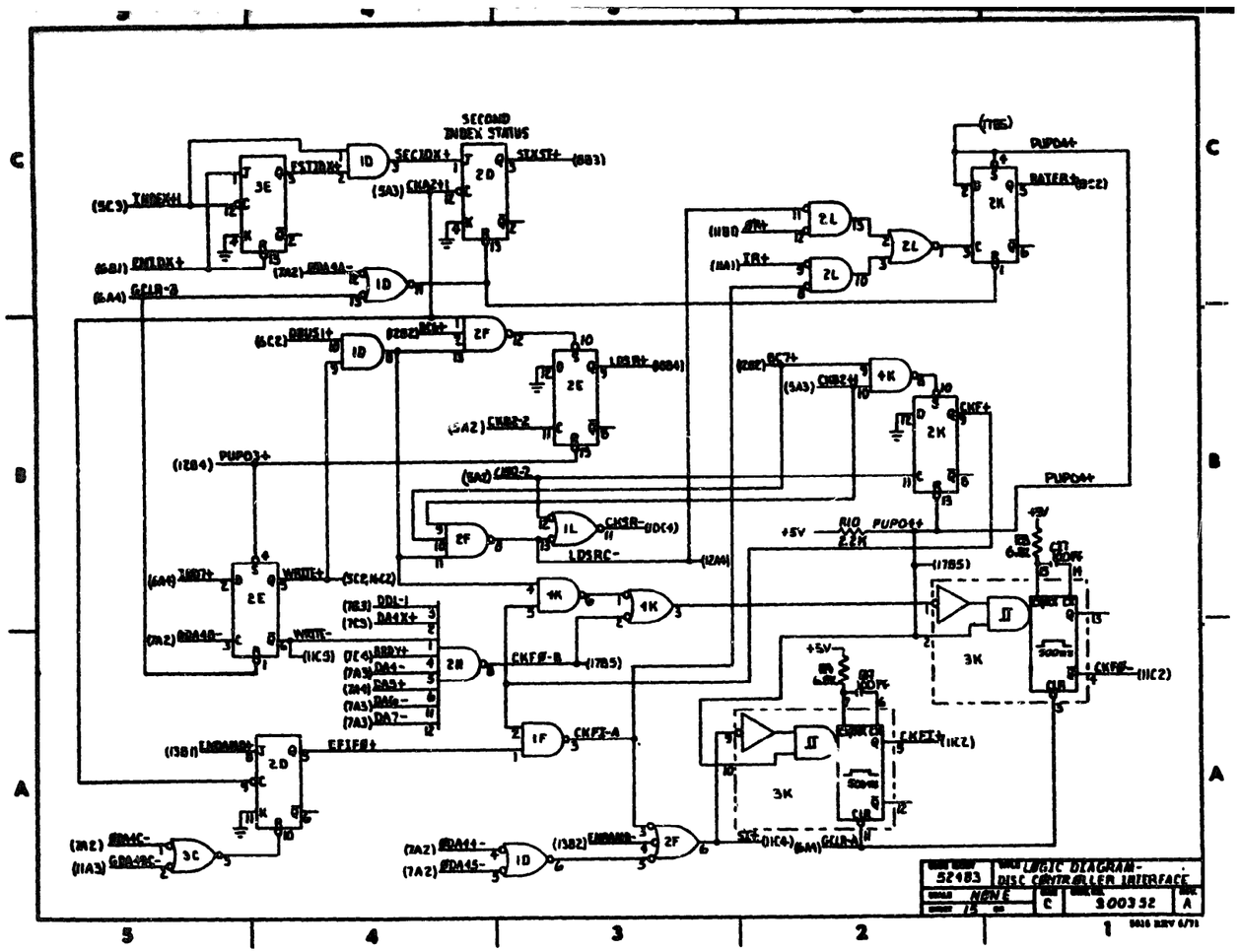

5
4
3
2
1
C
B
A
SR7+
(IIC5,I3A4)
SR6+
(IIC6,I3A4)
SR5+
(IIC5,I3A4)
SR4+
(IIC5,I3A4)
SR3+
(IIB5,I3A3)
SR2+
(IIB5,I3A3)
SR1+
(IIB5,I3A3)
SR0+
(SC2,IIB5,I3A3)
SR7-(I3A4)
SR6-(I3A4)
SR5-(I3A4)
SR4-(I3A3)
SR3-(I3A4)
SR2-(I3A4)
SR1-(I3A4)
SR0-(I3A4)
(6A4)GCLR-B
(I5B3)CNTR-
(IIC0) FIFO7+
(IIC0) FIFO6+
(IIB1) FIFO5+
(IIB0) FIFO4+
(IIB0) FIFO3+
(IIB0) FIFO2+
(IIB1) FIFO1+
(IIB0) FIFO0+
IOE
8 BIT REG.
+5V
R4 2.2K
(I5B3) LOAD+
(5B3) RESET+H
52483
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
NONE
C
300352
A

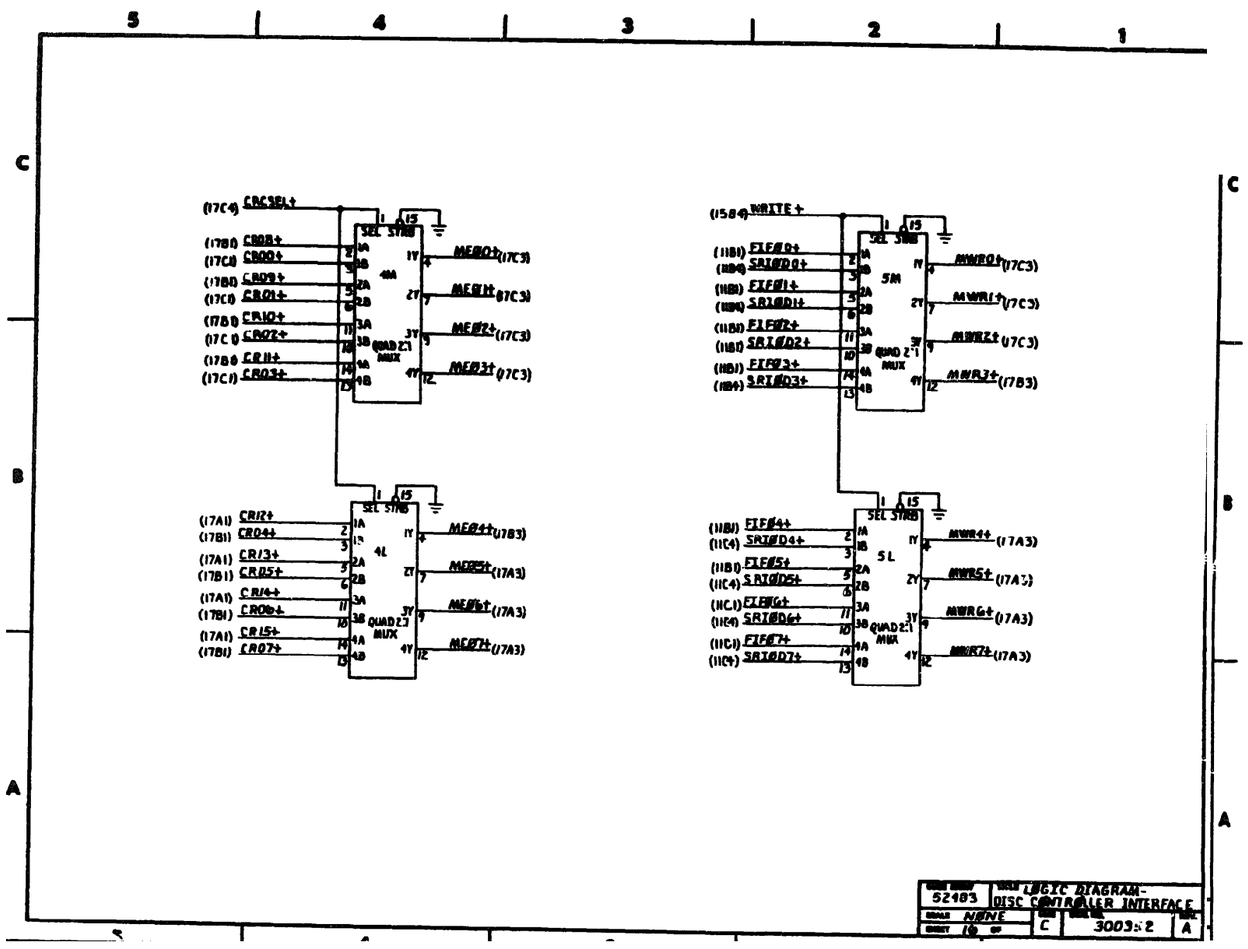

6L
7L
6M
7M
8L
8K
7K
7H
8B
SEL SRCE
QUAD 2:1 MUX
QUAD F/F
SRIBD7+
SRIBD6+
SRIBD5+
SRIBD4+
SRIBD3+
SRIBD2+
SRIBD1+
SRIBD0+
SI+
CHFX+
CHFX-
FIFB7+
FIFB6+
FIFB5+
FIFB4+
FIFB3+
FIFB2+
FIFB1+
FIFB0+
FIFB8+
IR+
GBA49-
GCLR-B
GBA44-
GBA49C-
+5V
2.2K
LOGIC DIAGRAM-
DESC CONTROLLER INTERFACE
52483
NONE
300392

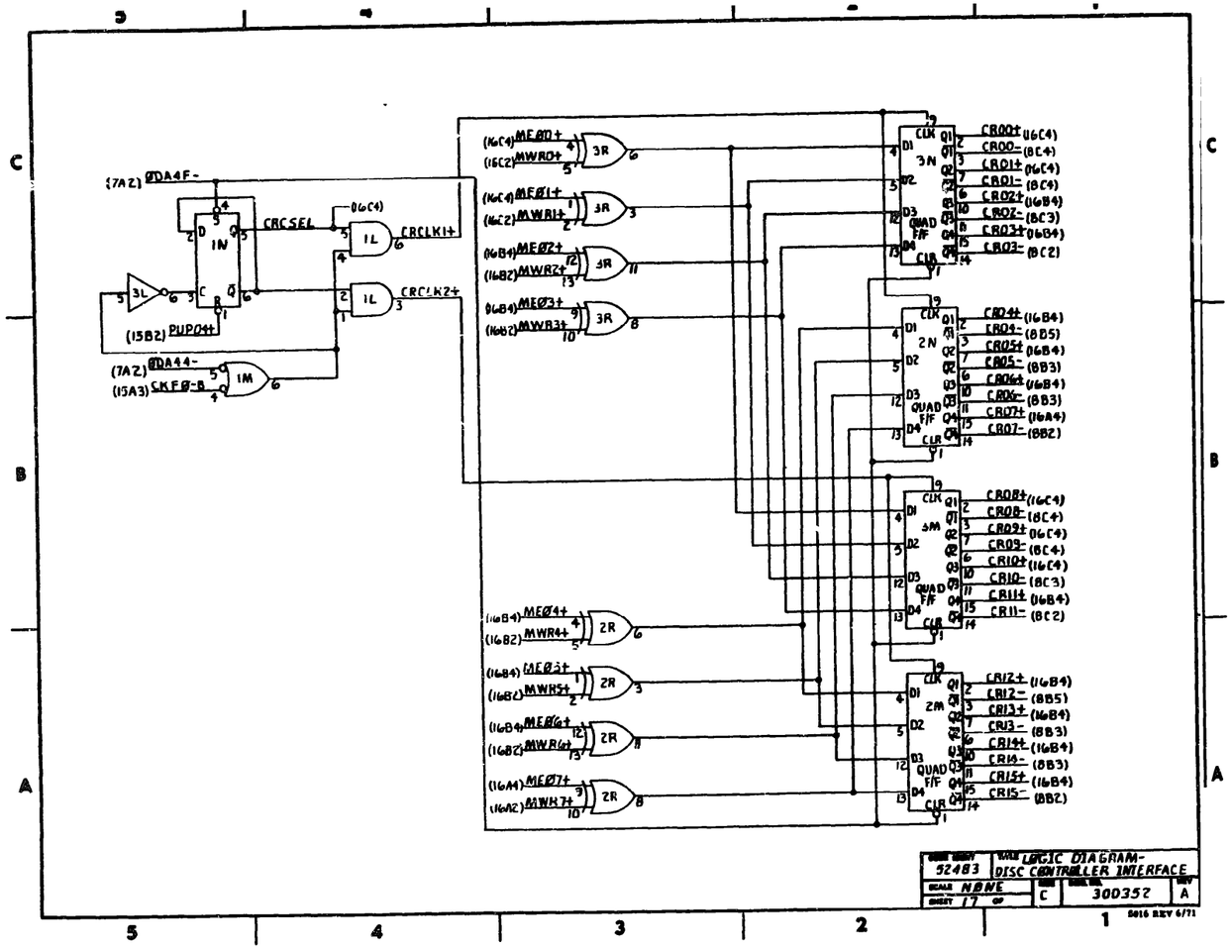

5
4
3
2
1
C
B
A
(5A4) GCLK-B
(5A2) CHAR-2
3D
4D
4:16 DEC
BIT0+
BIT1+
BIT2+
BC4-
BC6-
BC7-
BC6+ (1584)
BC7+ (1582)
(1582) ENDADD-
+5V
RP5
2.2K
PUP03+ (1585)
4E
(1581) FIFRD+
WAM+
3E
(5A3) CHAR2+
FINHCK+ (5C2)
FINHCK-
(1583) LDSEC-
7B
FINHCK-
52483
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
NONE
C
300352
A

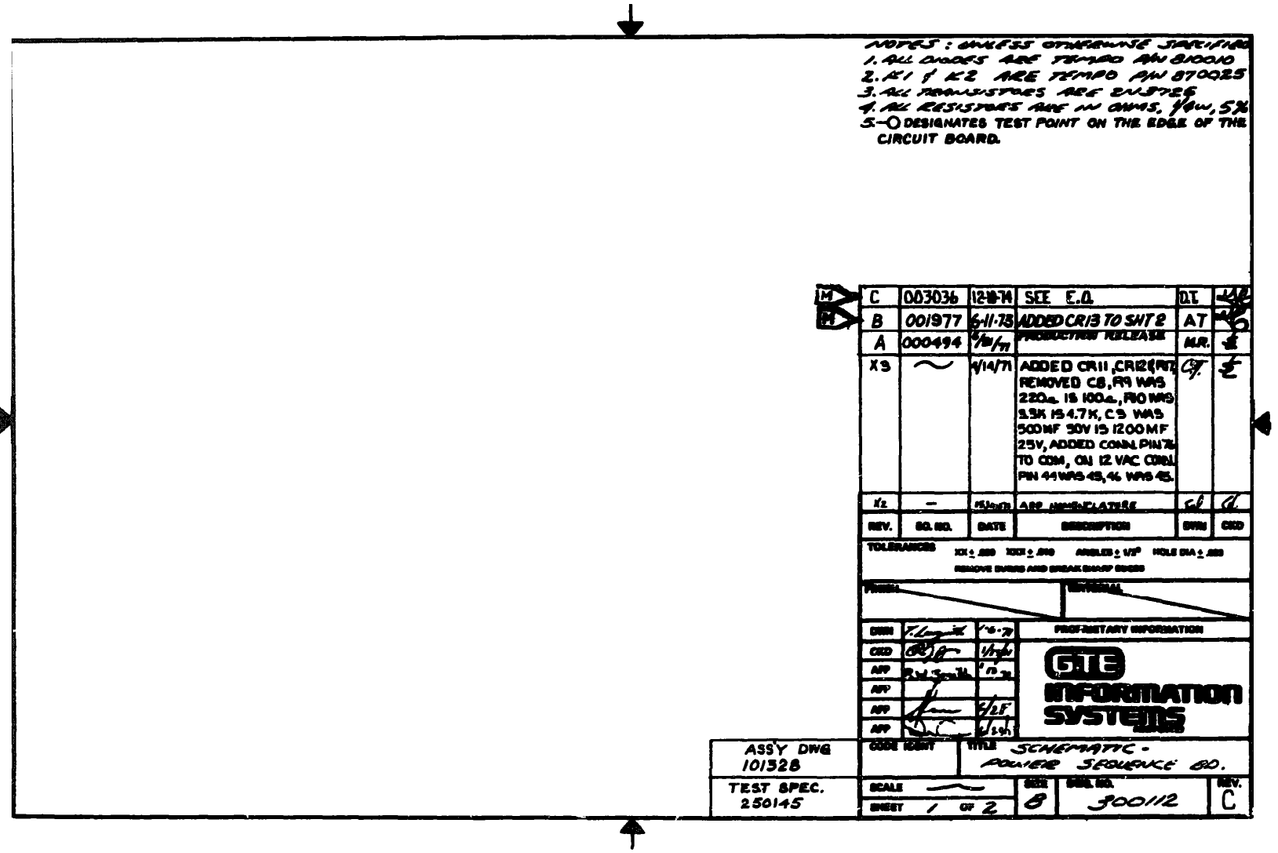

(7A2) RDA47-
(6B4) IRD4+
(6B4) IRD5+
(6A4) IRD6+
(6A4) IRD7+
(6A4) GCLR-B
CLK
CLR
RDHA+
RRTN+
RDDA+
RDRN+
5F
5F
4F
4F
6H
8H
(14C3) MMSY+
(6C4) IRDO+
(7A1) RRATN+
1F
(5A3) CMAE+
ENRAMD-
ENRAMD+
6K
1K
(0285, 5A3)
(5A3)
(6C4) IRDO-
8H
7H
10H
SBYT-
(14C5)
(10B3) SR4+
(10B3) SR5+
(10C3) SR6+
(10C3) SR7+
(10B2) SR0-
(10B2) SR1-
(10B2) SR2-
(10B2) SR3-
(10B2) SR4-
(10B2) SR5-
(10C2) SR6-
(10C2) SR7-
5H
AMRMES-
(14A5)
8E
AMZERO-
(14C5)
52483
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
NAME
C
300352
A

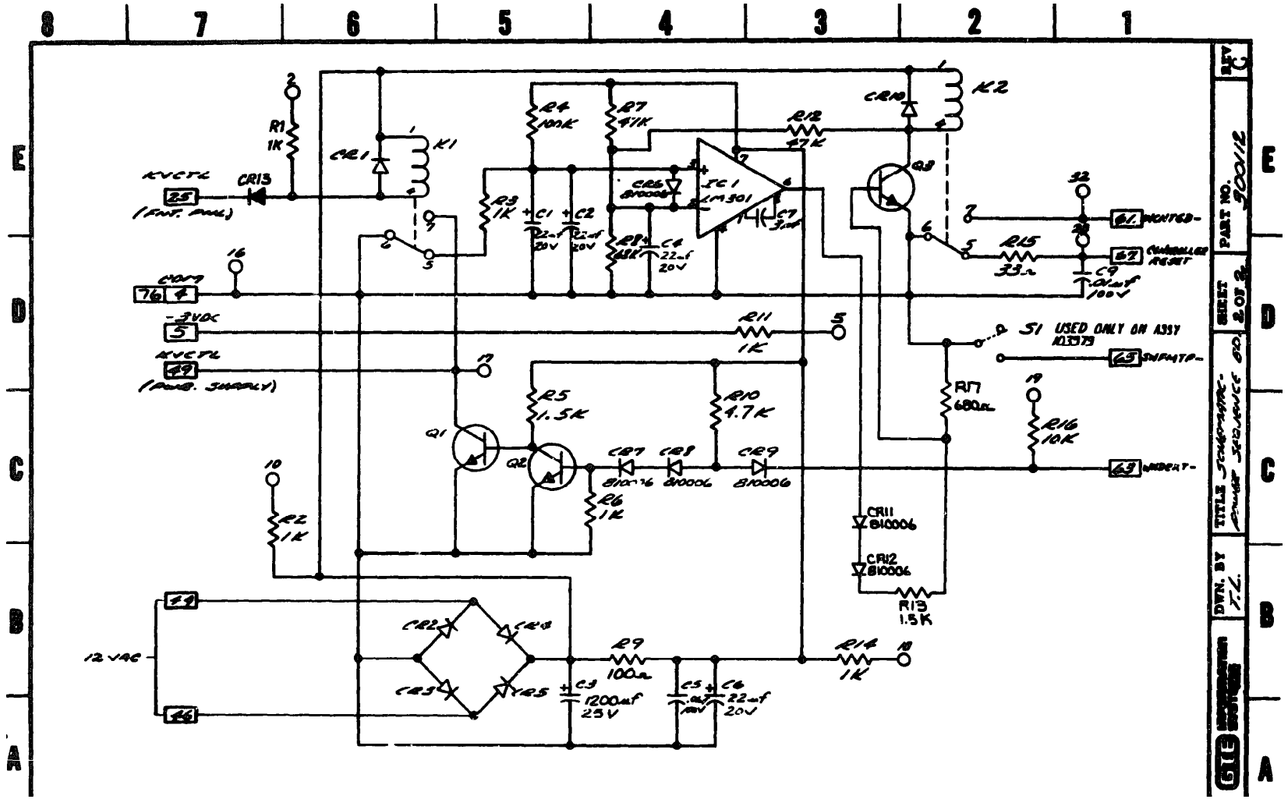

5
4
3
2
1
C
B
A
8F
8H
9F
9H
9E
3F
4N
3N
6N
6K
5M
5K
6D
4H
9N
3C
AMZERO+
AMRST-
AMRES+
AMRCT+
AMRCT-
AMRCT2+
AMRCT2-
AMRCT4+
AMRCT4-
AMSB+
SBYT-
SBYT+
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
300352

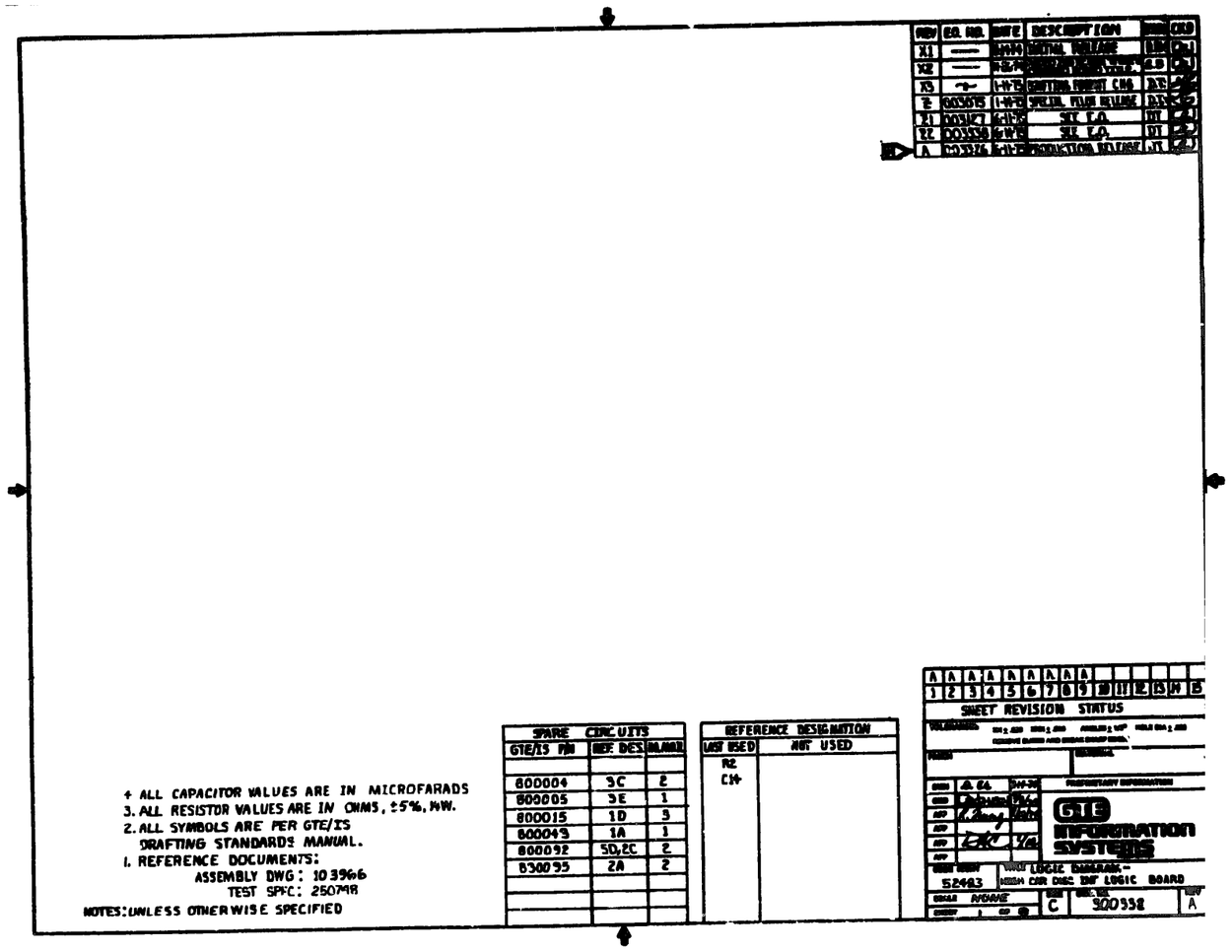

SECOND INDEX STATUS
LOGIC DIAGRAM - DISC CONTROLLER INTERFACE
52483
NONE
C
300352
A

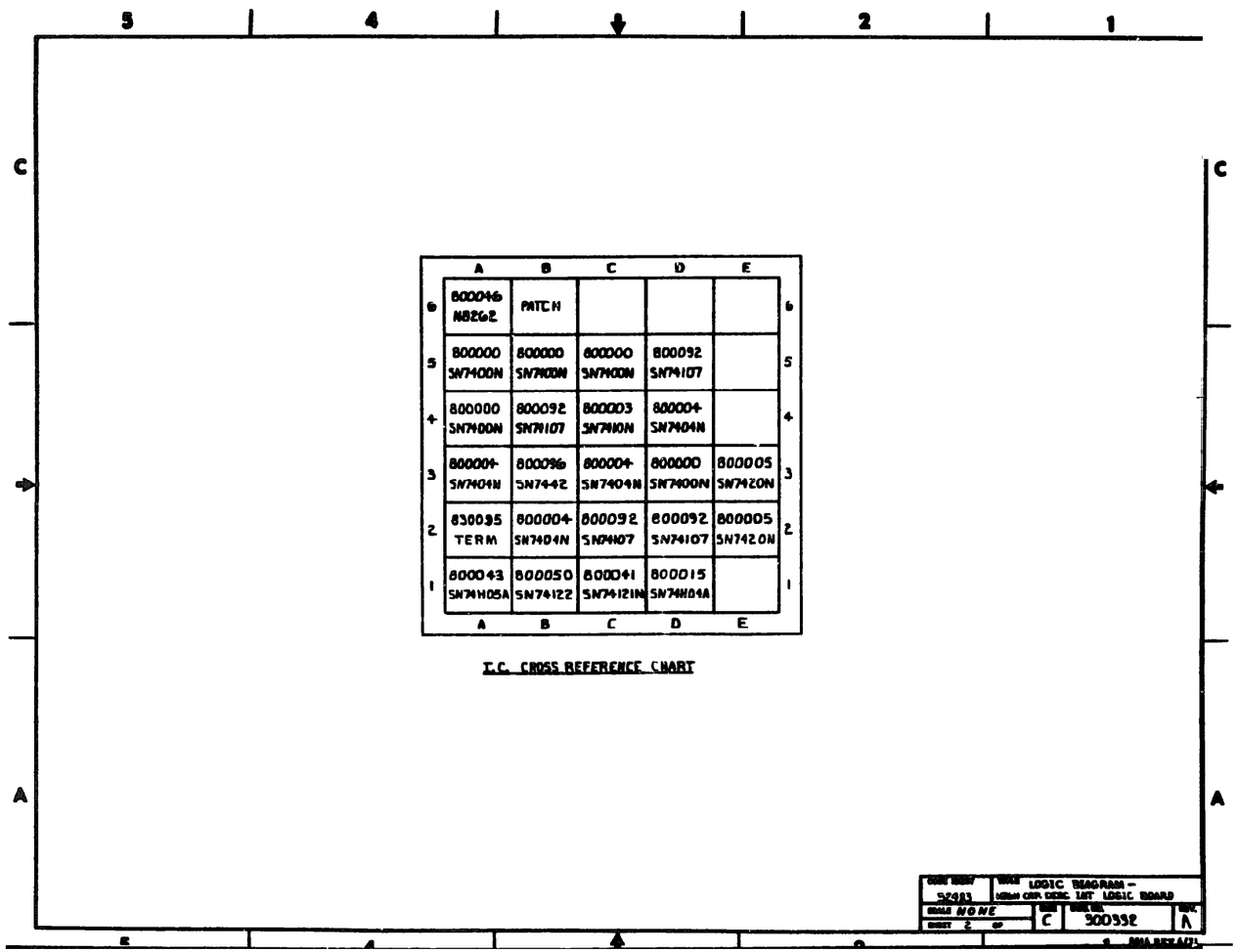

5
4
3
2
1
C
B
A
(17C4) CACSEL+
(17B8) CR08+
(17C8) CR00+
(17B8) CR09+
(17C8) CR01+
(17B8) CR10+
(17C8) CR02+
(17B8) CR11+
(17C8) CR03+
SEL STRB
QUAD 2:1 MUX
4M
ME@0+ (17C3)
ME@1+ (17C3)
ME@2+ (17C3)
ME@3+ (17C3)
(17A1) CR12+
(17B1) CR04+
(17A1) CR13+
(17B1) CR05+
(17A1) CR14+
(17B1) CR06+
(17A1) CR15+
(17B1) CR07+
4L
ME@4+ (17B3)
ME@5+ (17A3)
ME@6+ (17A3)
ME@7+ (17A3)
(1584) WRITE+
(11B1) FIF@0+
(11B0) SRI@D0+
(11B1) FIF@1+
(11B0) SRI@D1+
(11B0) FIF@2+
(11B1) SRI@D2+
(11B1) FIF@3+
(11B0) SRI@D3+
5M
MWR0+ (17C3)
MWR1+ (17C3)
MWR2+ (17C3)
MWR3+ (17B3)
(11B1) FIF@4+
(11C0) SRI@D4+
(11B1) FIF@5+
(11C0) SRI@D5+
(11C1) FIF@6+
(11C0) SRI@D6+
(11C1) FIF@7+
(11C0) SRI@D7+
5L
MWR4+ (17A3)
MWR5+ (17A3)
MWR6+ (17A3)
MWR7+ (17A3)
52483
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
NONE
C
3003582
A


(7A2) @DA4F-
CRCSEL
@6C4
CRCLK1+
CRCLK2+
(15B2) PUP04+
(7A2) @DA44-
(15A3) CKF@-B
(16C4) ME@0+
(16C2) MWR0+
(16C4) ME@1+
(16C2) MWR1+
(16B4) ME@2+
(16B2) MWR2+
(16B4) ME@3+
(16B2) MWR3+
(16B4) ME@4+
(16B2) MWR4+
(16B4) ME@5+
(16B2) MWR5+
(16B4) ME@6+
(16B2) MWR6+
(16A4) ME@7+
(16A2) MWR7+
CR00+ (16C4)
CR00- (8C4)
CR01+ (16C4)
CR01- (8C4)
CR02+ (16B4)
CR02- (8C3)
CR03+ (16B4)
CR03- (8C2)
CR04+ (16B4)
CR04- (8B5)
CR05+ (16B4)
CR05- (8B3)
CR06+ (16B4)
CR06- (8B3)
CR07+ (16A4)
CR07- (8B2)
CR08+ (16C4)
CR08- (8C4)
CR09+ (16C4)
CR09- (8C4)
CR10+ (16C4)
CR10- (8C3)
CR11+ (16B4)
CR11- (8C2)
CR12+ (16B4)
CR12- (8B5)
CR13+ (16B4)
CR13- (8B3)
CR14+ (16B4)
CR14- (8B3)
CR15+ (16B4)
CR15- (8B2)
LOGIC DIAGRAM-
DISC CONTROLLER INTERFACE
52483
NONE
300352
A
C


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE TEMPO AN 810010
2. K1 & K2 ARE TEMPO AN 870025
3. ALL TRANSISTORS ARE 2N3906
4. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
5. ○ DESIGNATES TEST POINT ON THE EDGE OF THE CIRCUIT BOARD.
C 003036 12-18-74 SEE E.O. D.T.
B 001977 6-11-73 ADDED CR13 TO SHT 2 AT
A 000494 PRODUCTION RELEASE M.R.
X3 4/14/71 ADDED CR11, CR12(NT), REMOVED C8, R9 WAS 220Ω, IS 100Ω, R10 WAS 3.3K IS 4.7K, C9 WAS 500MF 50V IS 1200 MF 25V, ADDED CONN. PIN 7& TO COM, ON 12 VAC COIL PIN 44 WAS 43, 44 WAS 45.
REV. NO. NO. DATE DESCRIPTION DWN CKD
TOLERANCES
PROPRIETARY INFORMATION
GTE INFORMATION SYSTEMS
ASSY DWG 101328
TEST SPEC. 250145
CODE IDENT
TITLE SCHEMATIC - POWER SEQUENCE BD.
SCALE
SHEET 1 OF 2
SIZE B
DWG NO. 300112
REV. C


8
7
6
5
4
3
2
1
E
D
C
B
A
R1 1K
CR1
K1
KVCTL
CR13
(FNT. PNL.)
R4 100K
R7 47K
R12 47K
CR10
K2
Q3
IC1 LM301
CR6 BY100006
C7 .1uf
R3 1K
+C1 22uf 20V
+C2 22uf 20V
R8 68K
C4 22uf 20V
32
J1 MONITOR-
J2 CONTROLLER RESET
R15 33Ω
C9 220uf 100V
+8VDC
J3
R11 1K
S1 USED ONLY ON ASSY A13579
J3 SHUNT-
KVCTL
(PWR. SUPPLY)
R5 1.5K
R10 4.7K
R17 680Ω
R16 10K
Q1
Q2
CR7 BY100006
CR8 BY100006
CR9 BY100006
J3 VIDEO-
R2 1K
CR11 BY100006
CR12 BY100006
R13 1.5K
J1
J6
12 VAC
CR2
CR4
CR3
CR5
C3 1200uf 25V
R9 100Ω
C5 .1uf
C6 22uf 20V
R14 1K
TITLE SCHEMATIC-POWER SOURCE
PART NO. 300112
SHEET 2 OF 2
DWN. BY T.L.
GTE

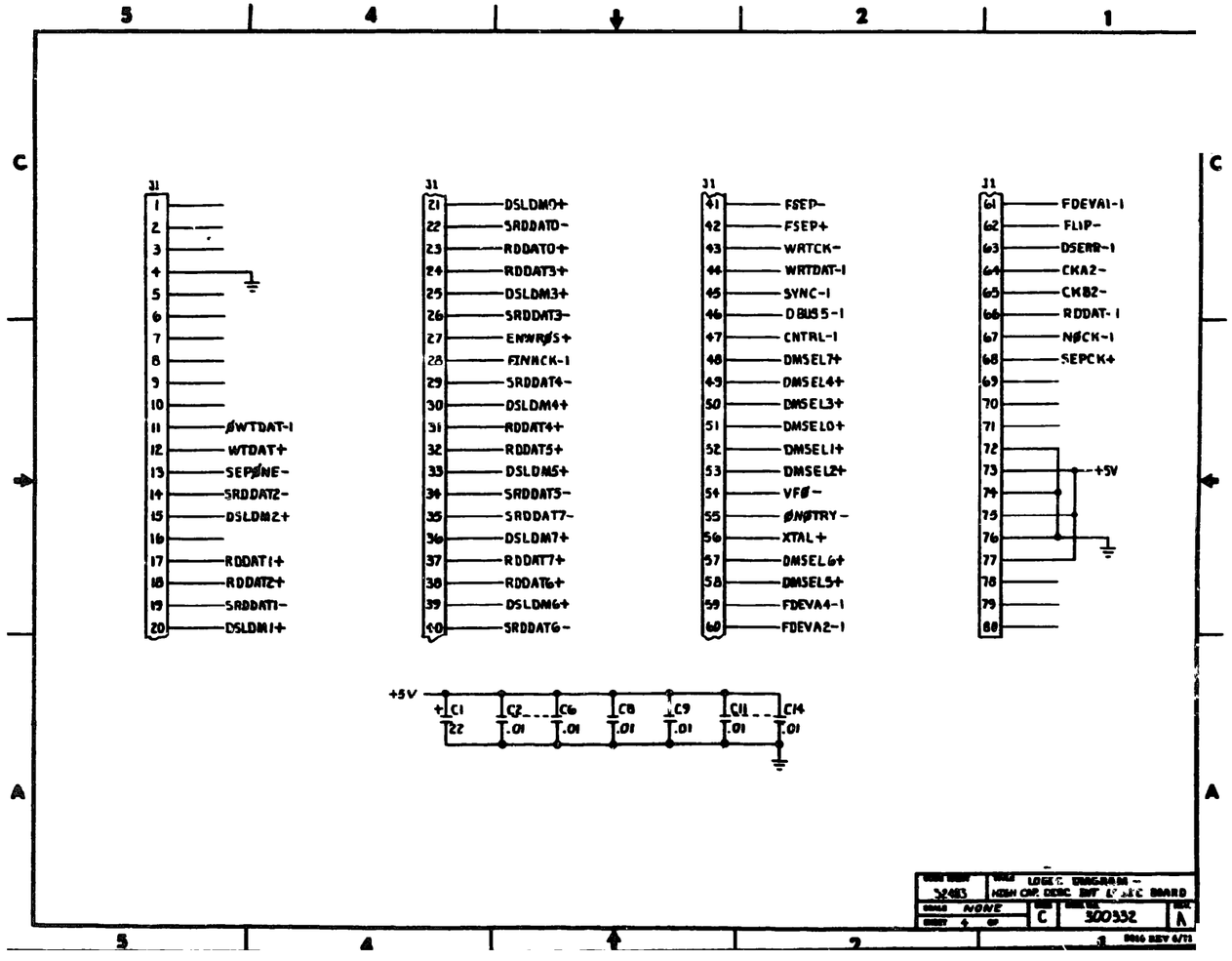

REV | ECO. NO. | DATE | DESCRIPTION | DRN | CKD
X1
X2
X3
X
X1
X2
A
SPARE CIRCUITS
GTE/IS P/N | REF. DES. | NUMBER
800004 | 3C | 2
800005 | 3E | 1
800015 | 1D | 3
800049 | 1A | 1
800092 | 5D,2C | 2
830035 | 2A | 2
REFERENCE DESIGNATION
LAST USED | NOT USED
R2
C14
SHEET REVISION STATUS
GTE INFORMATION SYSTEMS
52483
LOGIC BOARD
SCALE NONE
C
500358
A
+ ALL CAPACITOR VALUES ARE IN MICROFARADS
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.
1. REFERENCE DOCUMENTS:
ASSEMBLY DWG: 103966
TEST SPEC: 250718
NOTES: UNLESS OTHERWISE SPECIFIED

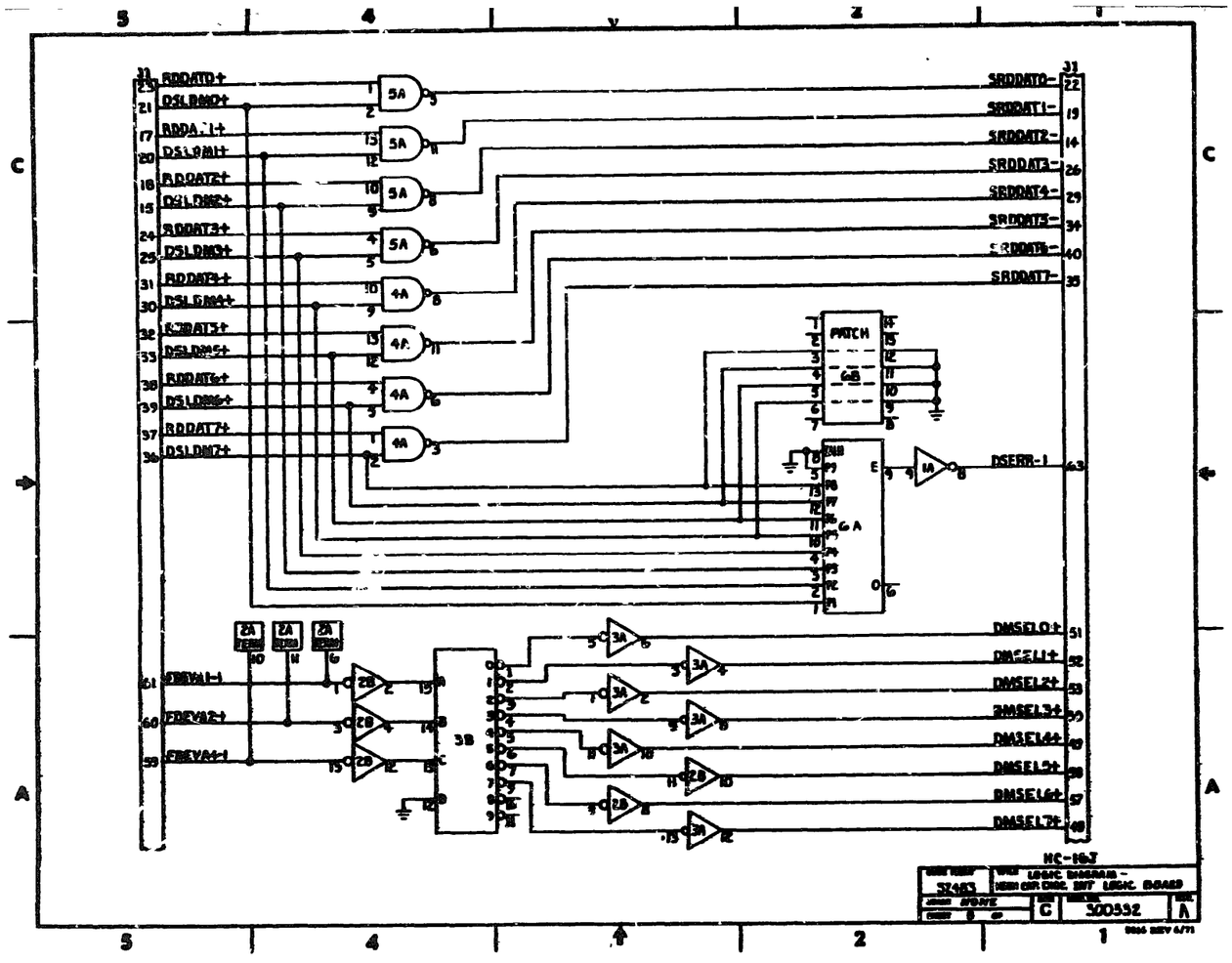

5
4
3
2
1
C
A
B
C
D
E
6
5
4
3
2
1
800046 N8262
PATCH
800000 SN7400N
800092 SN74107
800004 SN7404N
800096 SN7442
800005 SN7420N
830035 TERM
800043 SN74H05A
800050 SN74122
800041 SN74121N
800015 SN74H04A
I.C. CROSS REFERENCE CHART
LOGIC DIAGRAM - 16bit CPU DISPL. INT. LOGIC BOARD
NONE
C
300392
A

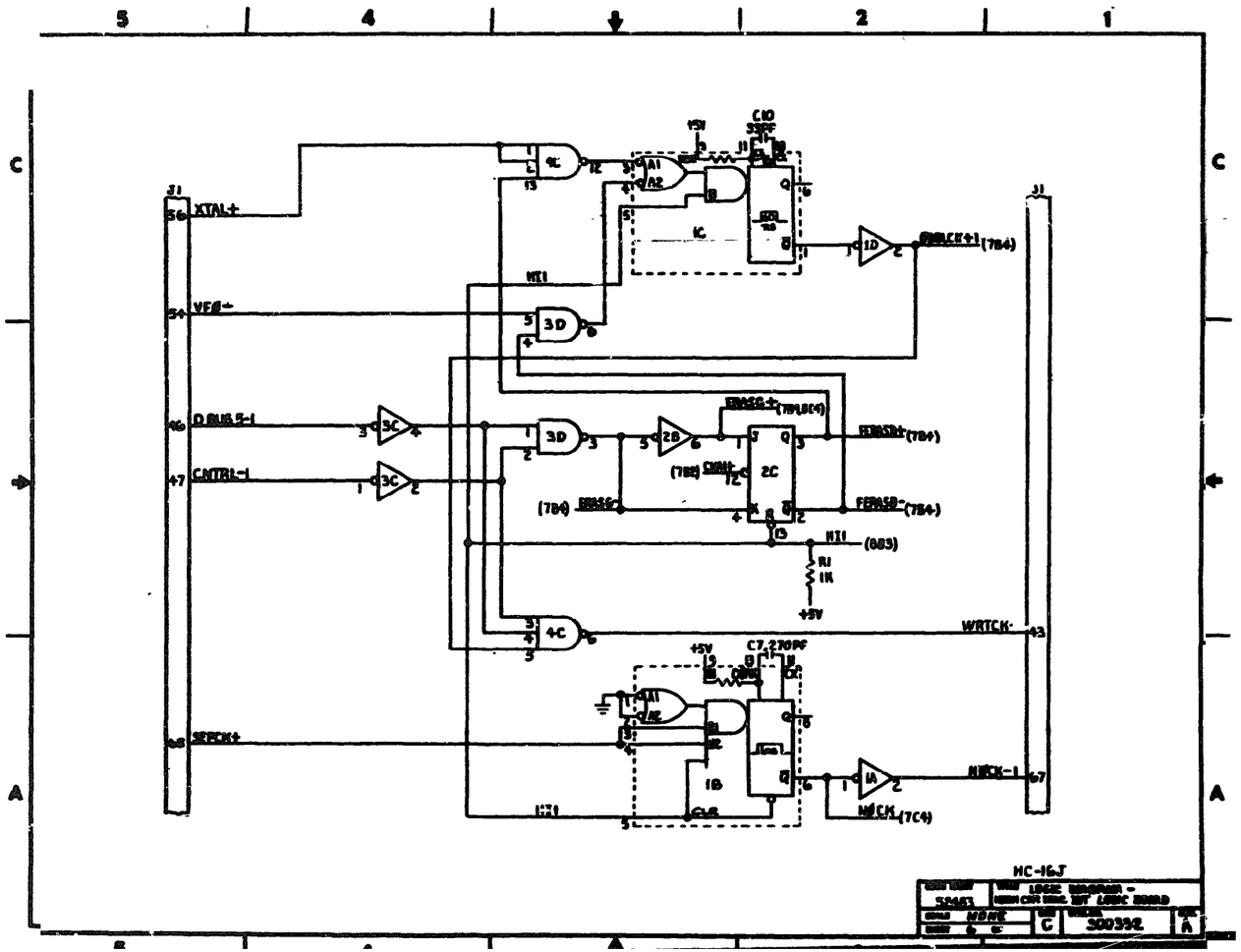
MNEMONIC GLOSSARY		
MNEMONIC	SOURCE	DEFINITION
DBUS	6B5	DRIVE BUS
CHA	7B3	CLOCK PHASE A
CHB	7A1	CLOCK PHASE B
CNTRL	6B5	CONTROL TAG
DMSEL	5A1	DRIVE MODULE SELECT
DSERR	5B1	DRIVE SELECT ERROR
DSLDM	5B5,5C5	SELECTED MODULE FROM DRIVE
ENWRDS	7A1	ENABLE WRITING ONES
ERASG	6B3	ERASE GATE
FDEVA	5A5	DRIVE ADDRESS
FENSEP	7C3	ENABLE SEPARATE CLOCK
FERASD	6B2	ERASE GATE DELAYED BY ONE CLOCK
FINHCK	7A5	INHIBIT WRITING CLOCKS
FLIP	7C2	FLIP THE SEPARATE FLIP-FLOP
FSEP	7B1	SEPARATE CLOCK A AND B

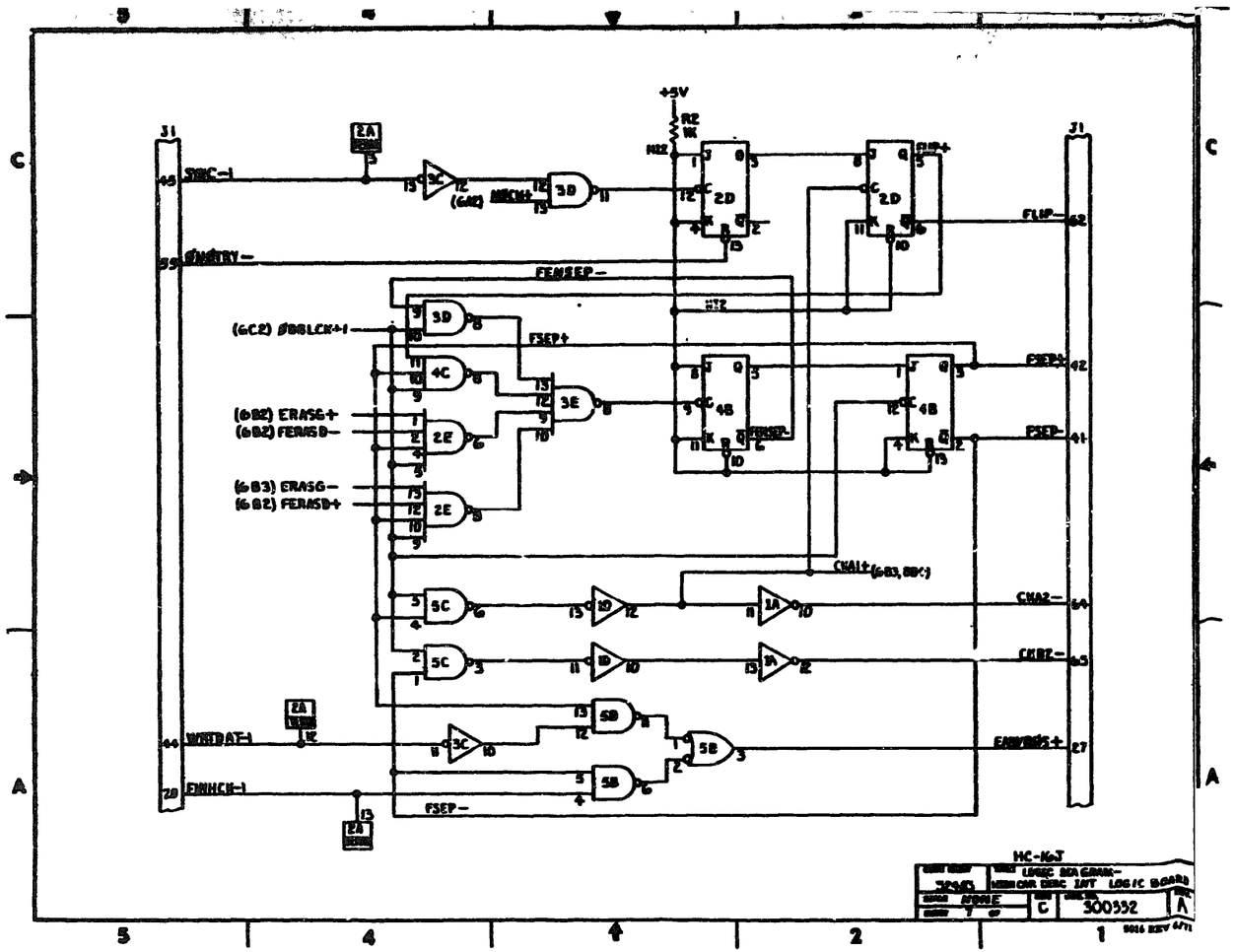
MNEMONIC GLOSSARY		
MNEMONIC	SOURCE	DEFINITION
HI	6B2, 7C5	HIGH FOR UNUSED INPUT
MBCK	6A2	MB CLOCK
MDBLCK	6C2	DOUBLE CLOCKS, PHASE A AND B
ONESW	7C5	ONE BIT RE-SYNC ONE SHOT
QWTDAT	8C4	SHAPED WRITE DATA
RDDAT	5B5,5C5, 6B2	READ DATA
SEPCK	6A5	DETECTED CLOCKS FROM BIT STREAM
SEPONE	6B4	DETECTED ONES FROM BIT STREAM
SRDDAT	5C1	SELECTED READ DATA
SYNC	7C5	SYNCHRONIZED TO VFO
VFO	6C5	VARIABLE FREQUENCY OSCILLATOR
WRTCK	6B1	WRITE CLOCK
WRTDAT	7A5	WRITE DATA FROM CONTROLLER
WTDAT	8C2	WRITE DATA TO DRIVER
XTAL	6C5	CRYSTAL OSCILLATOR (5MHz)

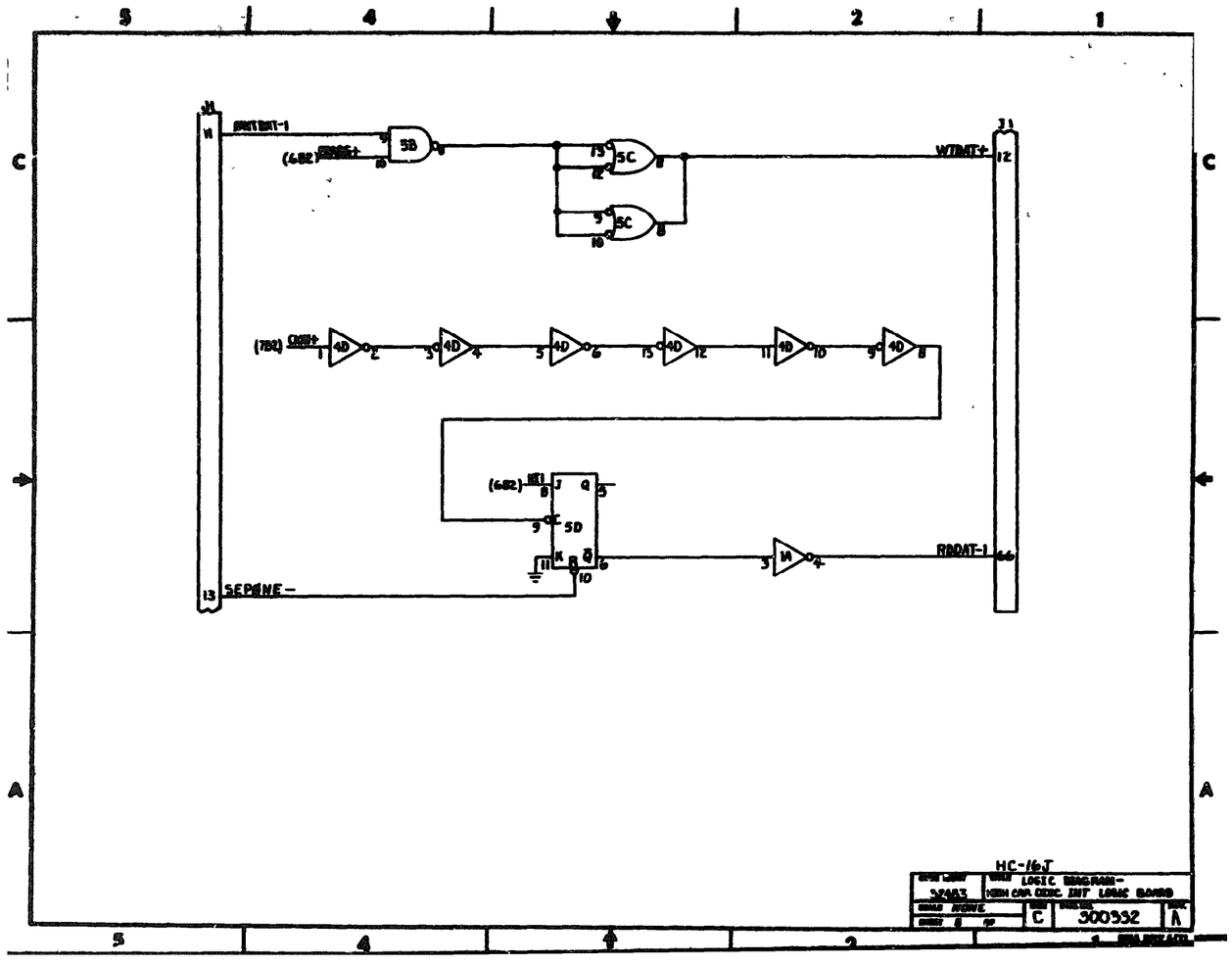
32483	LOGIC DIAGRAM - HSDA CMD DECOD UNIT LOGIC BOARD		
SCALE NONE	SIZE C	300332	REV A
SHEET 5 OF			9016 REV 6/71

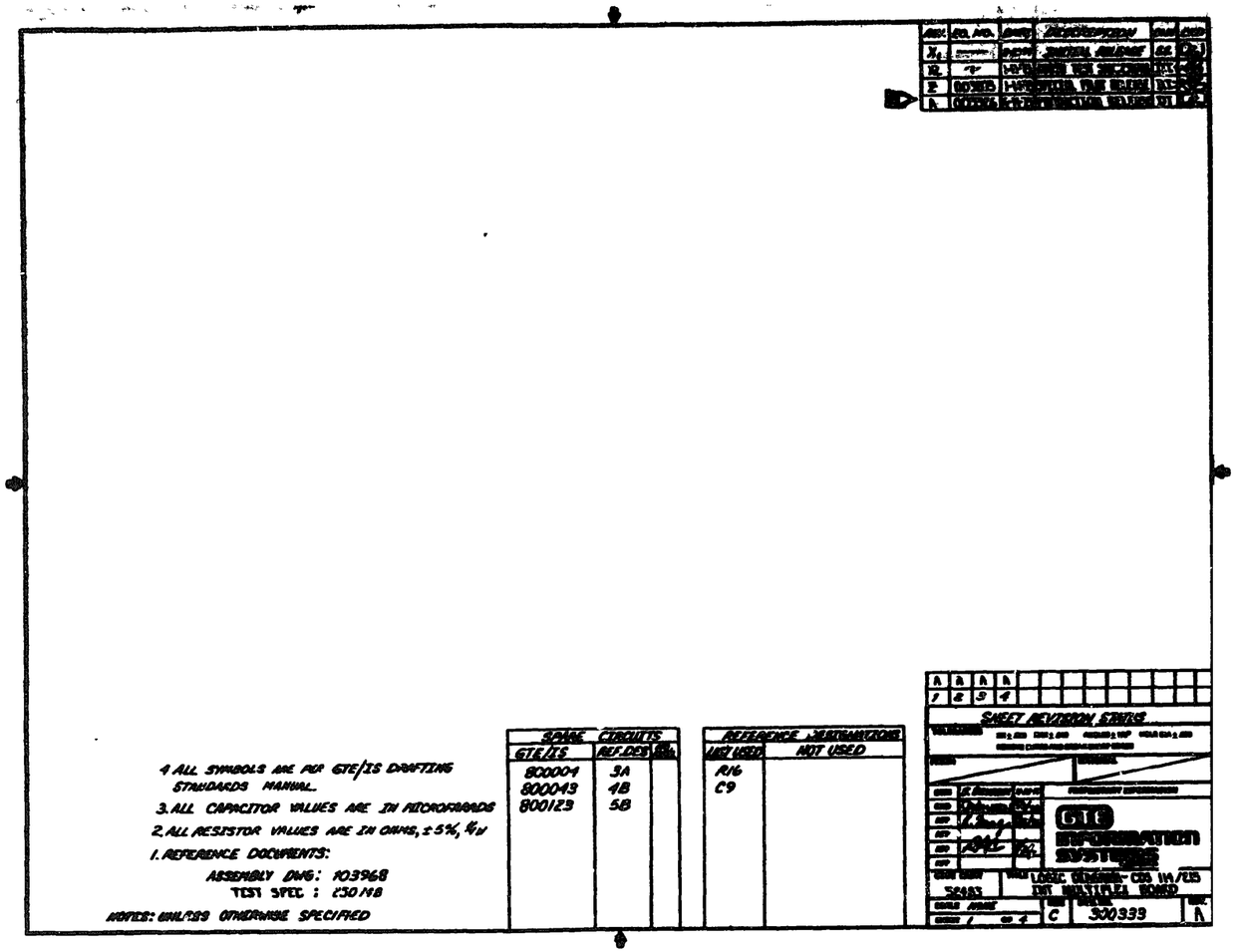

5
4
3
2
1
C
A
J1
1 2 3 4 5 6 7 8 9 10 11 WTDAT-1 12 WTDAT+ 13 SEPONE- 14 SRDDAT2- 15 DSLDM2+ 16 17 RDDAT1+ 18 RDDAT2+ 19 SRDDAT1- 20 DSLDM1+
21 DSLDM0+ 22 SRDDAT0- 23 RDDAT0+ 24 RDDAT3+ 25 DSLDM3+ 26 SRDDAT3- 27 ENWRGS+ 28 FINACK-1 29 SRDDAT4- 30 DSLDM4+ 31 RDDAT4+ 32 RDDAT5+ 33 DSLDM5+ 34 SRDDAT5- 35 SRDDAT7- 36 DSLDM7+ 37 RDDAT7+ 38 RDDAT6+ 39 DSLDM6+ 40 SRDDAT6-
41 FSED- 42 FSEP+ 43 WRTCK- 44 WRTDAT-1 45 SYNC-1 46 DBUS5-1 47 CNTRL-1 48 DMSEL7+ 49 DMSEL4+ 50 DMSEL3+ 51 DMSEL0+ 52 DMSEL1+ 53 DMSEL2+ 54 VFO- 55 ONOTRY- 56 XTAL+ 57 DMSEL6+ 58 DMSEL5+ 59 FDEVA4-1 60 FDEVA2-1
61 FDEVA1-1 62 FLIP- 63 DSERR-1 64 CKA2- 65 CKB2- 66 RDDAT-1 67 NOCK-1 68 SEPCK+ 69 70 71 72 73 +5V 74 75 76 77 78 79 80
+5V
+ C1 22
C2 .01
C6 .01
C8 .01
C9 .01
C11 .01
C14 .01
LOGIC DIAGRAM -
HIGH CAP. DISC INT. LOGIC BOARD
52483
NONE
C
300332
A


RDDATD+
DSLDMD+
RDDAT1+
DSLDM1+
RDDAT2+
DSLDM2+
RDDAT3+
DSLDM3+
RDDAT4+
DSLDM4+
RDDAT5+
DSLDM5+
RDDAT6+
DSLDM6+
RDDAT7+
DSLDM7+
SRDDAT0-
SRDDAT1-
SRDDAT2-
SRDDAT3-
SRDDAT4-
SRDDAT5-
SRDDAT6-
SRDDAT7-
PATCH
DSERR-1
DMSEL0+
DMSEL1+
DMSEL2+
DMSEL3+
DMSEL4+
DMSEL5+
DMSEL6+
DMSEL7+
FREVA1-1
FREVB2-1
FREVA4-1
HC-167
C
300532


5
4
3
2
1
C
A
J1
XTAL+
VFB+
D BUS 5-1
CNTRL-1
SERCK+
4C
3D
3C
2B
2C
1D
1A
1C
1B
C10
330PF
C7,270PF
+5V
WRITE
ERASE+
ERASE-
WRTCK-
RCLK-1
RCLK
HC-16J
LOGIC DIAGRAM -
MONICHROME CRT LOGIC BOARD
MOORE
C
300392
A


+5V
R2
1K
J1
2A
3C
3B
2D
3D
4C
3E
2E
4B
5C
1A
5B
FLIP-
FSEP+
FSEP-
FEMSEP-
CHA1+(683,88C)
CHA2-
CHB2-
FSEP-
HC-H6T
LOGIC DATA CHAN-
NEL CHR ERSC INT LOGIC BOARD
300552
A


J1
11
WTDAT-1
(682) SBSEL+
15
5B
9
75
5C
12
8
9
5C
10
8
J1
12
WTDAT+
(782) CMBF+
1
4D
2
3
4D
4
5
4D
6
15
4D
12
11
4D
10
9
4D
8
(682) MR1
9
CK
5D
11
R
Q
6
10
5
1A
4
RRDAT-1
66
13
SERINE-
HC-16J
LOGIC DIAGRAMS-
MAIN CPA CERC. INT LOGIC BOARD
C
300332
A

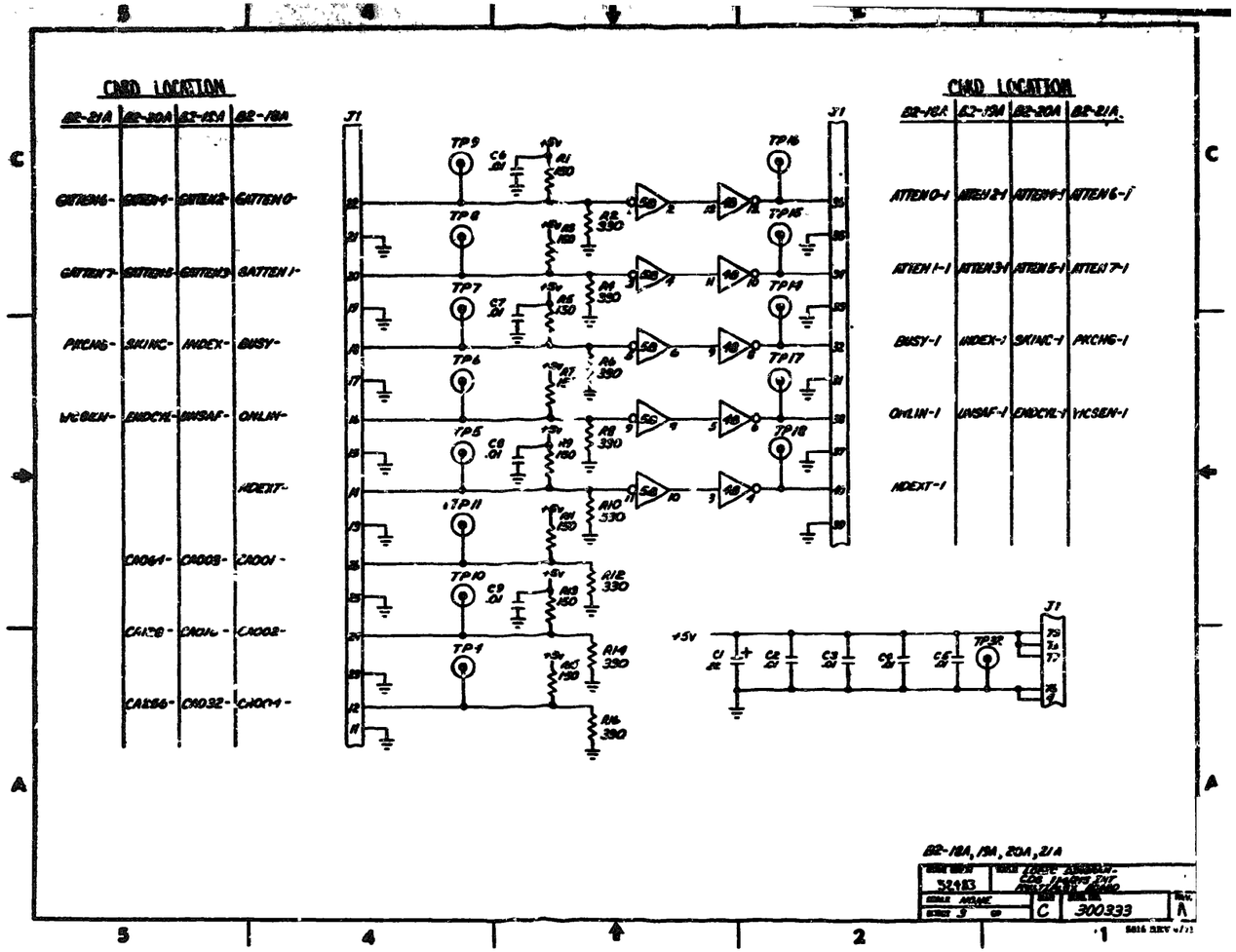

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W
1. REFERENCE DOCUMENTS:
ASSEMBLY DWG: 103968
TEST SPEC : 250198
NOTES: UNLESS OTHERWISE SPECIFIED
SIMILAR CIRCUITS
GTE/IS
800004
800043
800123
REF DES
3A
4B
5B
REFERENCE DESIGNATIONS
NOT USED
R16
C9
SHEET REVISION STATUS
GTE
INFORMATION SYSTEMS
LOGIC BOARD - CDS 114/125
C
500339

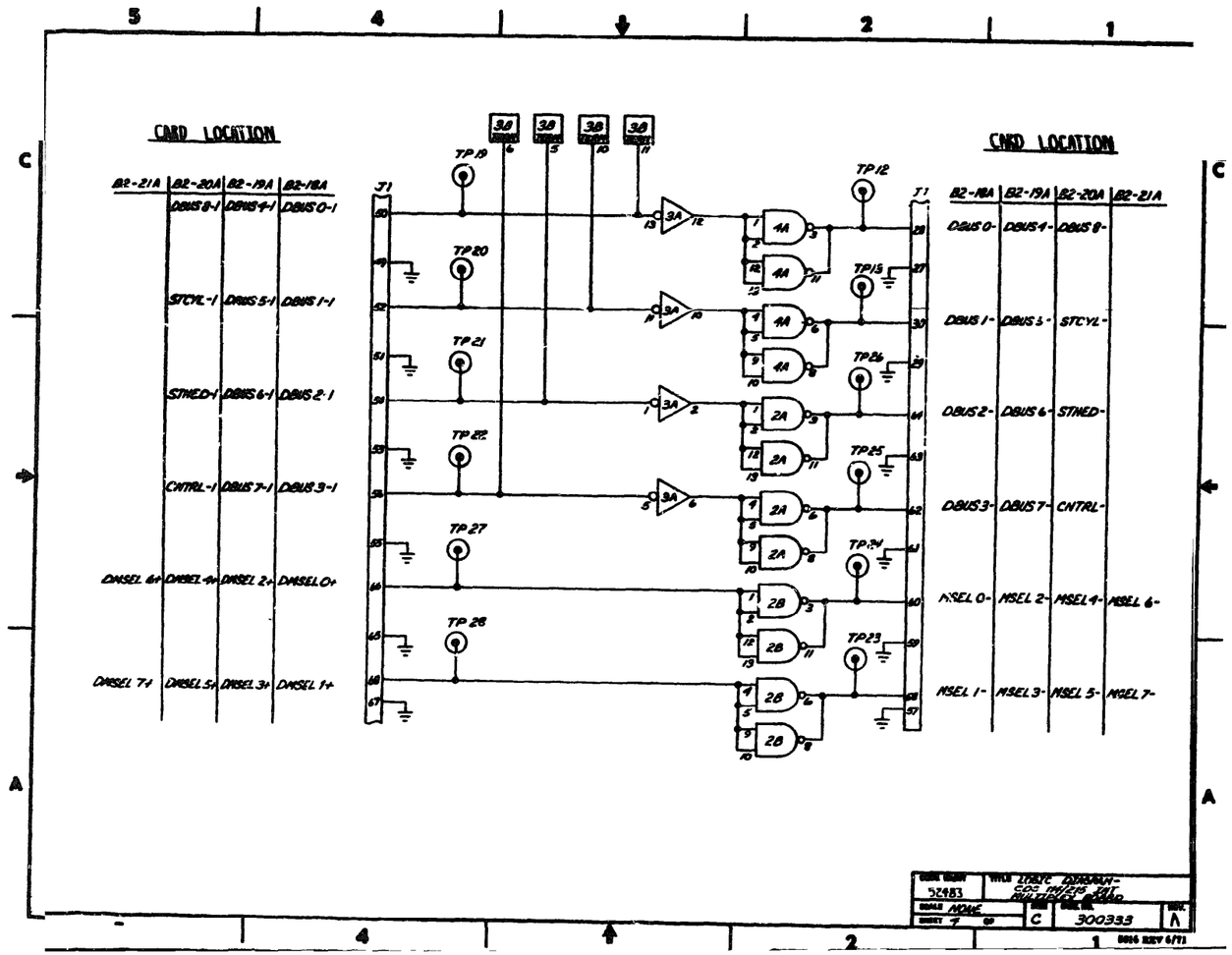
	A	B
6	SAME	SAME
5		800123 7414
4	800046 7438	800043 74405
3	800004 7401	830095 7E84
2	800046 7438	800046 7438
1	SAME	SAME

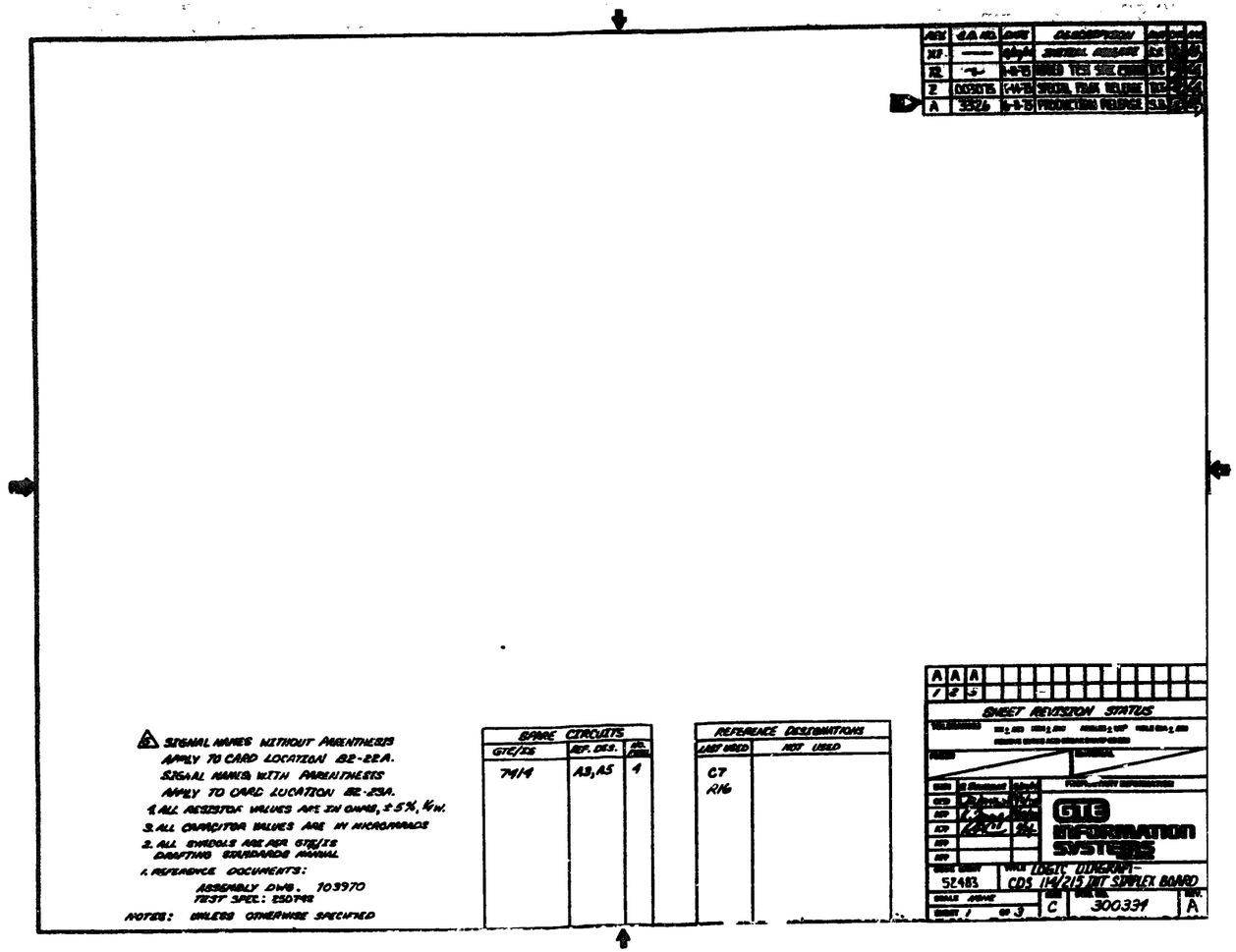
MNEMONIC GLOSSARY		
ABBREVIATE	SQUARE	DEFINITION
ATTEN	3C1	ATTENTION
BUSY	382,384	BUSY STATUS
CAXXY	385,385	CYLINDER ADDRESS REGISTER
CNTRL	421,405	CONTROL TAG
DBUS	384F,385, 381,4C1	DRIVE BUS
DNSEL	4RE,4R5	DRIVE MODULE SELECT
ENDCYL	381,385	END OF CYLINDER STATUS
GATTEN	3C5	GATED ATTENTION
HDEXT	382,384	HEADS EXTENDED
INDEX	381,385	INDEX STATUS
MSEL	4R1,4R2	MODULE SELECT
ONLIN	382,384	ON LINE STATUS
PKCHG	384,385	PACK CHANGE STATUS
SEINC	384,3B5	SEEK INCOMPLETE STATUS
STCYL	4C1,4C5	SET CYLINDER TAG
STHED	4B1,4B5	SET HEAD TAG
UNSAF	381,385	UNSAFE STATUS
WCSEN	384,385	WRITE CURRENT SENSE STATUS

SIZE 5248	TITLE LOGIC ASSEMBLY CYL ADDRESS REG. MULTIPLEX		
SCALE NONE		C	DWG NO. 300333
SHEET 2 OF			REV A

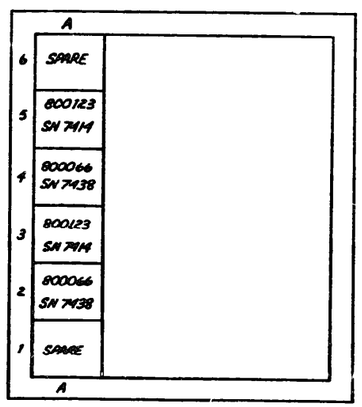
SCALE 1=1 DEV 6/71

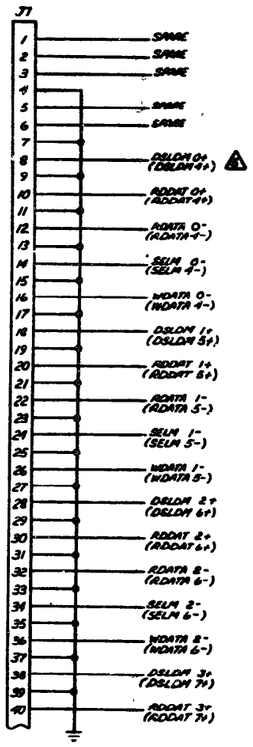

CARD LOCATION
B2-21A
B2-20A
B2-19A
B2-18A
GATEEN6-
GATEEN4-
GATEEN2-
GATTEN0-
GATTEN7-
GATTEN5-
GATTEN3-
GATTEN1-
PKCHG-
SKINC-
INDEX-
BUSY-
MCGEN-
ENDCYL-
UNSAF-
ONLIN-
NDEXT-
CA064-
CA008-
CA001-
CA128-
CA016-
CA002-
CA256-
CA032-
CA004-
J1
TP9
TP8
TP7
TP6
TP5
TP11
TP10
TP4
TP16
TP15
TP14
TP17
TP18
TP12
C6 .01
C7 .01
C8 .01
C9 .01
C4 .01
R1 330
R2 330
R3 330
R4 330
R5 330
R6 330
R7 330
R8 330
R9 150
R10 330
R11 330
R12 330
R13 150
R14 330
R15 150
R16 330
+5V
5G8
4G8
5G6
4G6
5G4
4G4
5G2
4G2
ATTEN0-1
ATTEN2-1
ATTEN4-1
ATTEN6-1
ATTEN1-1
ATTEN3-1
ATTEN5-1
ATTEN7-1
BUSY-1
INDEX-1
SKINC-1
PKCHG-1
ONLIN-1
UNSAF-1
ENDCYL-1
YKCSEN-1
NDEXT-1
C1 .02
C2 .01
C3 .01
C4 .01
C5 .01
TP13
B2-18A, 19A, 20A, 21A
52483
C
300333

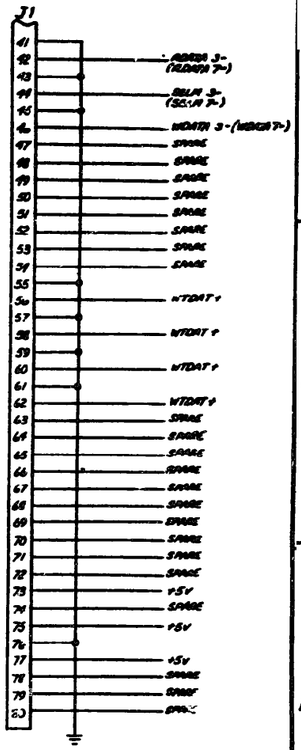

CARD LOCATION
B2-21A
B2-20A
B2-19A
B2-18A
DBUS 0-1
DBUS 4-1
DBUS 8-1
STCYL-1
DBUS 5-1
DBUS 1-1
STMED-1
DBUS 6-1
DBUS 2-1
CNTRL-1
DBUS 7-1
DBUS 3-1
DMSEL 6+
DMSEL 4+
DMSEL 2+
DMSEL 0+
DMSEL 7+
DMSEL 5+
DMSEL 3+
DMSEL 1+
J1
3A
4A
2A
2B
TP19
TP20
TP21
TP22
TP27
TP28
TP12
TP15
TP26
TP25
TP24
TP23
CARD LOCATION
B2-18A
B2-19A
B2-20A
B2-21A
DBUS 0-
DBUS 4-
DBUS 8-
DBUS 1-
DBUS 5-
STCYL-
DBUS 2-
DBUS 6-
STMED-
DBUS 3-
DBUS 7-
CNTRL-
MSEL 0-
MSEL 2-
MSEL 4-
MSEL 6-
MSEL 1-
MSEL 3-
MSEL 5-
MSEL 7-
52483
C
300333
A


SIGNAL NAMES WITHOUT PARENTHESIS APPLY TO CARD LOCATION B2-22A.
SIGNAL NAMES WITH PARENTHESIS APPLY TO CARD LOCATION B2-23A.
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL
4. REFERENCE DOCUMENTS:
ASSEMBLY DWG. 703970
TEST SPEC.: 250798
NOTES: UNLESS OTHERWISE SPECIFIED
SPARE CIRCUITS
GTE/IS
REF. DES.
NO. PINS
74/4
A3, A5
4
REFERENCE DESIGNATIONS
LAST USED
NOT USED
C7
R16
SHEET REVISION STATUS
GTE INFORMATION SYSTEMS
LOGIC DIAGRAM - CDS 114/215 INT. SIMPLEX BOARD
52483
C
300331
A

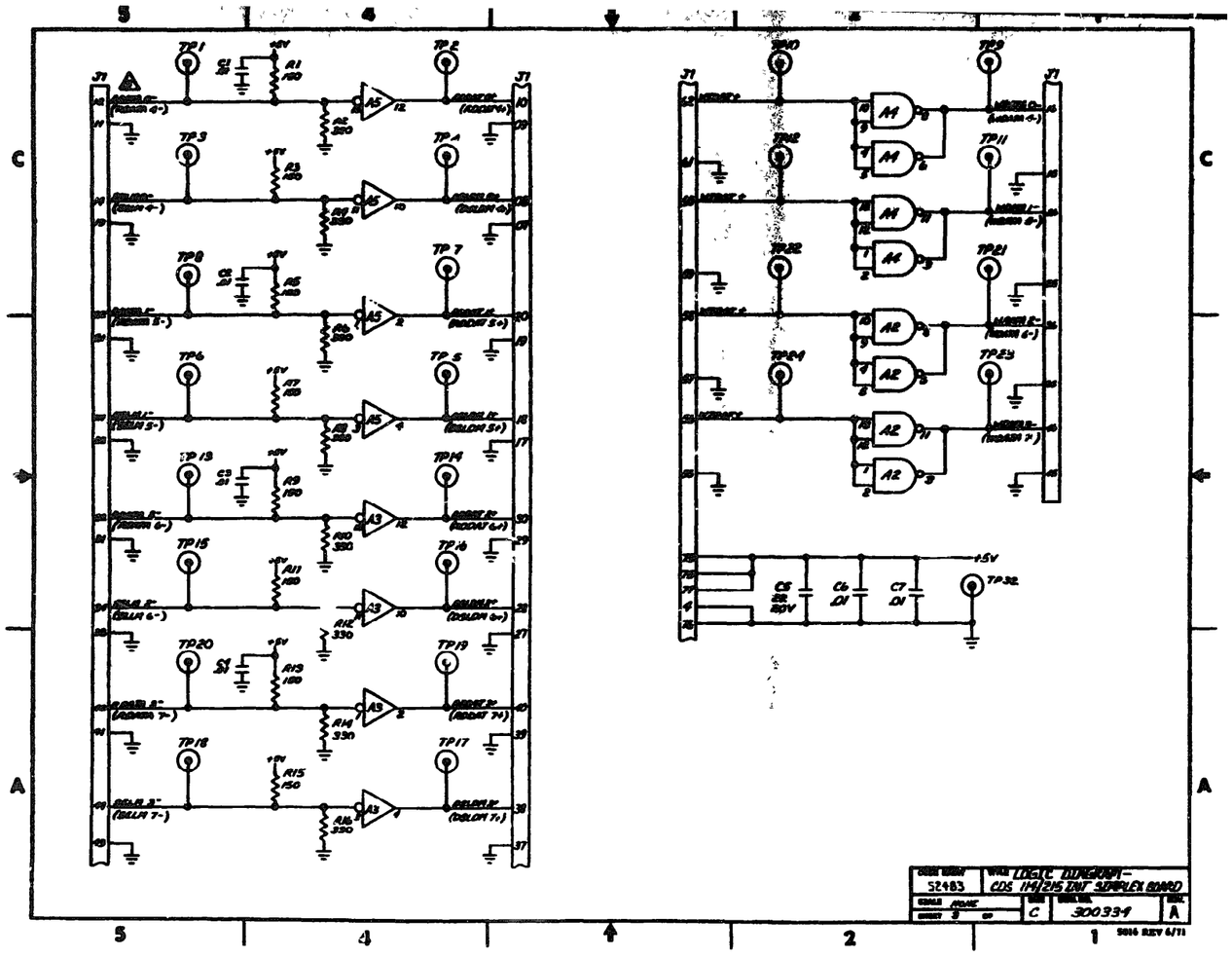
MNEMONIC GLOSSARY		
MNEMONIC	SOURCE	DEFINITION
DSLDM	306, 804, 302	SELECT MODULE TO CONTROLLER
RDATA	305, 805, 303	READ DATA FROM DISC DRIVE
RDDAT	306, 804, 304	READ DATA TO CONTROLLER
SELM	302, 802, 308	SELECT MODULE TO DISC DRIVE
WDATA	301, 801	WRITE DATA TO DISC DRIVE
WTDAT	303, 803	WRITE DATA TO CONTROLLER







52483	CDC M-41/25 INT. SERIALEX BOARD		
SIZE C		300339	A


LOGIC DIAGRAM -
CDS 1M/21S INT SIMPLEX BOARD
52483
300334
C
A

REV	E.N.O	DATE	DESCRIPTION
W	—	[illegible]	[illegible]
Z	3980	[illegible]	[illegible]
A	3926	[illegible]	[illegible]
B	3970	04-1	SEE E.O.

6. ALL TRANSISTORS ARE 2N2369A
5. ALL DIODES ARE 810006.
4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.
3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W
1. REFERENCE DOCUMENTS:
ASSEMBLY DWG. 104295
TEST SPEC: 250778
NOTES: UNLESS OTHERWISE SPECIFIED

SPARE CIRCUITS

GTE/IS PIN	REF DES	USE WITH
8000M	5A	2

REFERENCE DESIGNATIONS

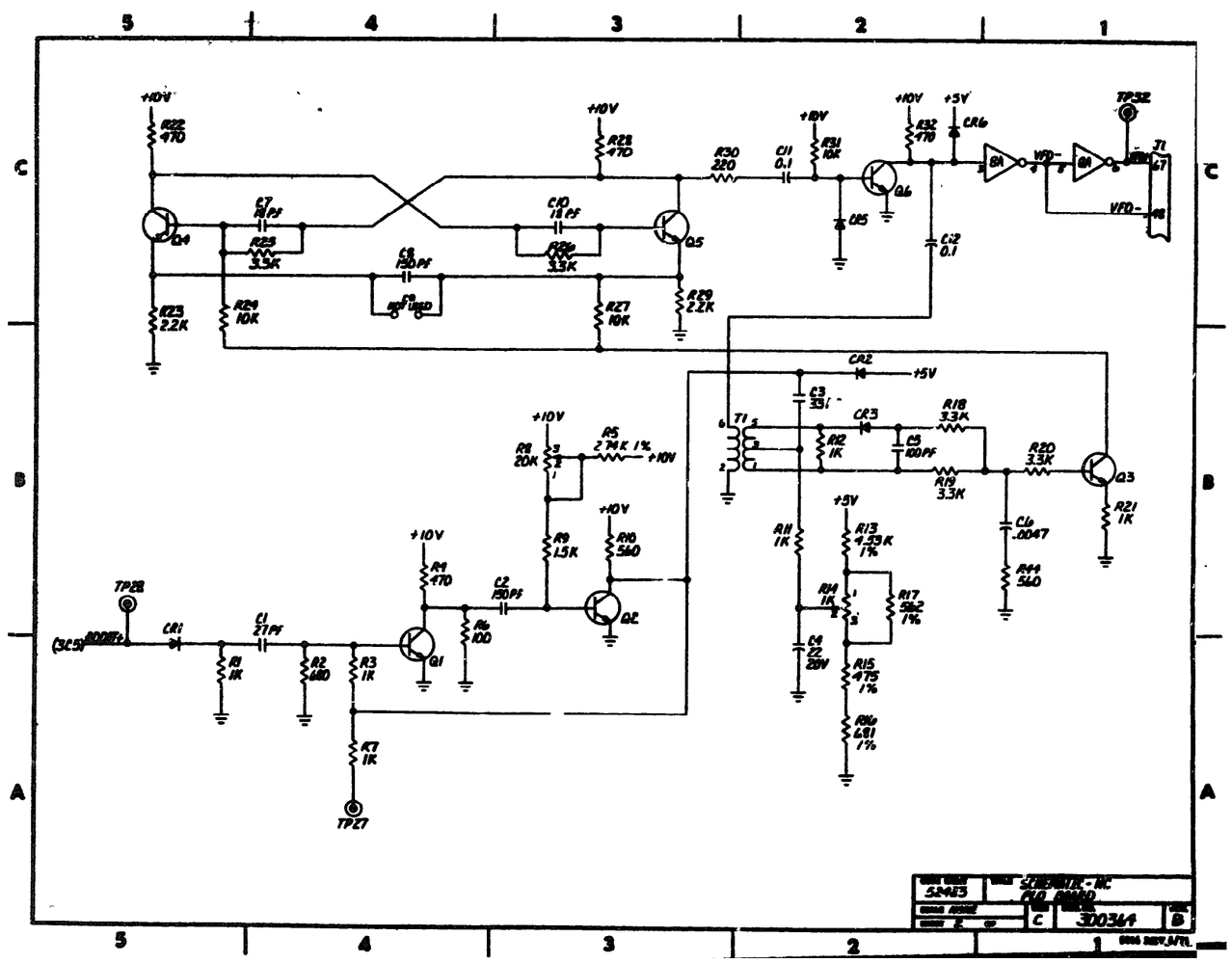
LAST USED	NOT USED
R44	R34
C31	C15 C9
CR8	
Q6	
T1	
TP32	
Z1	

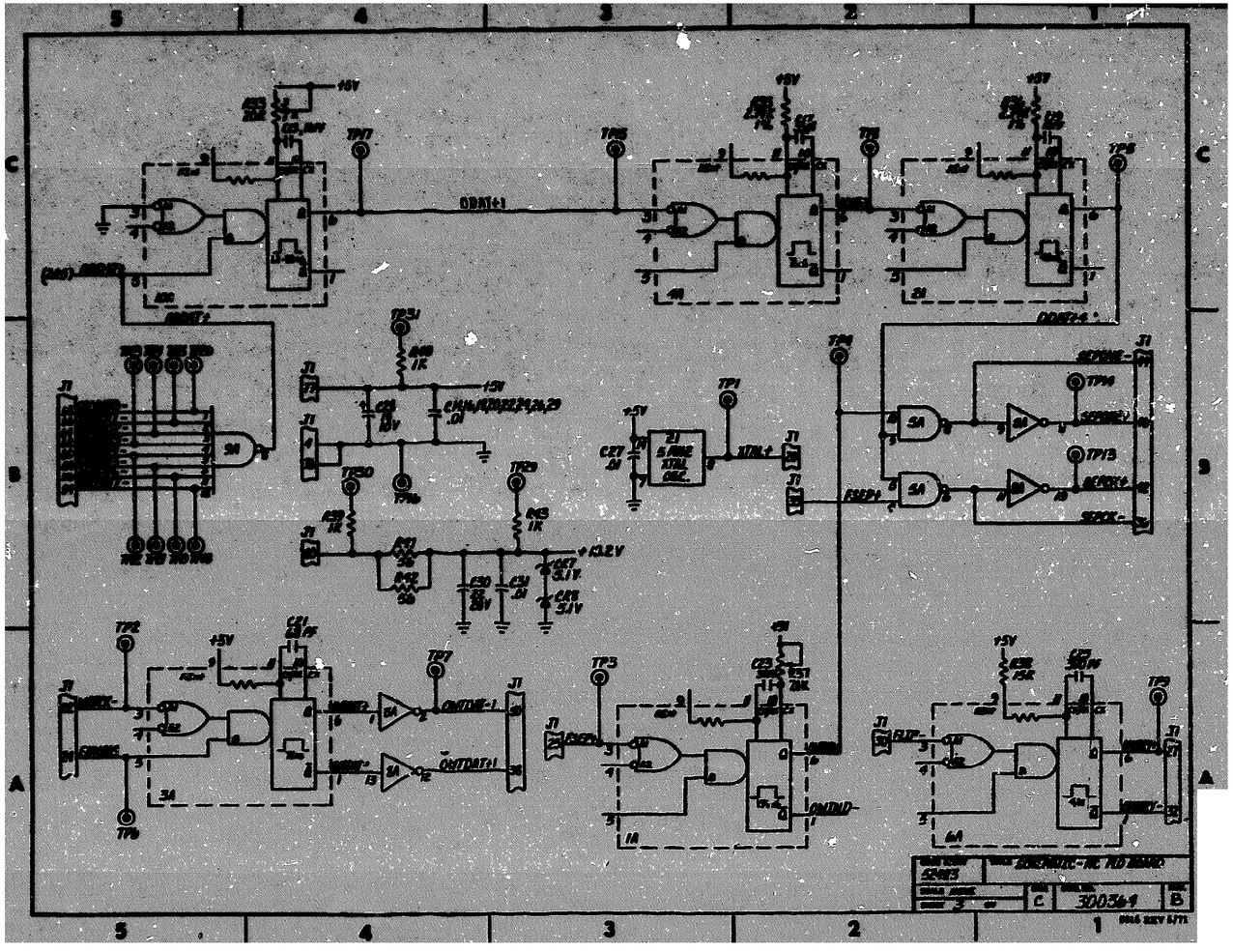
SHEET REVISION STATUS

1	2	3	

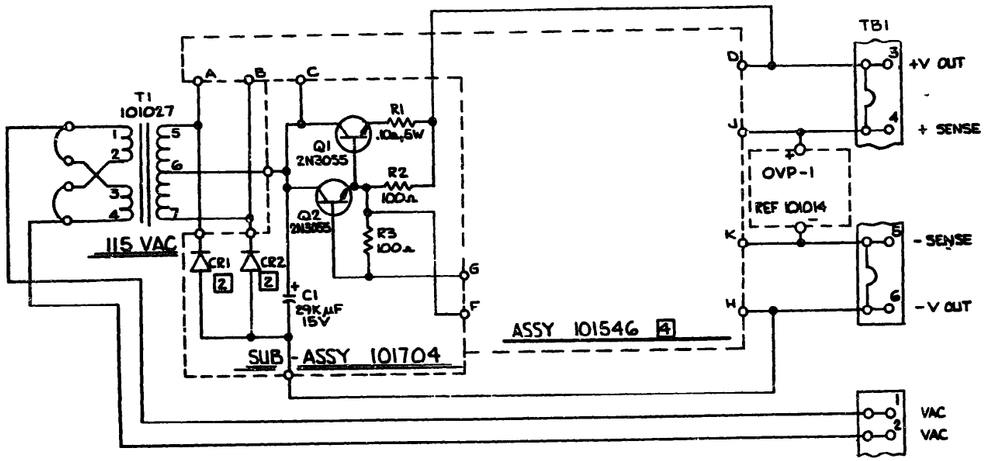
GTE INFORMATION SYSTEMS

SIZE	DRAWING NO.	REV.
52483	SCHEMATIC-MC PLO BOARD	
C	300364	B


5
4
3
2
1
C
B
A
+10V
+5V
R22 470
R28 470
R30 220
C11 0.1
R31 10K
R32 470
CR6
TP32
J1
VFD-
C7 18 PF
C10 18 PF
Q4
Q5
Q6
R25 3.3K
R26 3.3K
C8 150 PF
R24 2.2K
R29 10K
R27 10K
R29 2.2K
C12 0.1
CR2
C3 33
R18 3.3K
CR3
T1
R12 1K
C5 100 PF
R19 3.3K
R20 3.3K
Q3
R21 1K
C6 .0047
R44 560
R5 2.74K 1%
R8 20K
R9 1.5K
R10 560
R11 1K
R13 4.53K 1%
R14 1K
R17 5862 1%
C4 22 20V
R15 475 1%
R16 681 1%
TP28
CR1
C1 27 PF
R1 1K
R2 680
R3 1K
R4 470
C2 150 PF
R6 100
Q1
Q2
K1 1K
TP27
5413
C
30364
B



REV	BY	DESCRIPTION	DATE
A		INITIAL RELEASE	
B		INCORPORATED ECO 10049	
C		INCORPORATED ECO 10109	
D		INCORPORATED ECO 10883	



4 MODIFY ASSY 101546 PER INSTRUCTIONS AT ASSY 101700, REF ECO 10109.
3. REFERENCE ASSEMBIES: 101700, 101704, 101546 & 101014.
2 PART NO. 20F10, INT'L RECTIFIER.
1. CARBON RESISTORS, TOL ±5%, 1/2W.

NOTES:

NEXT ASSY	USED ON	QUAN. REQ'D	ITEM NO.
	M282		
APPLICATION			

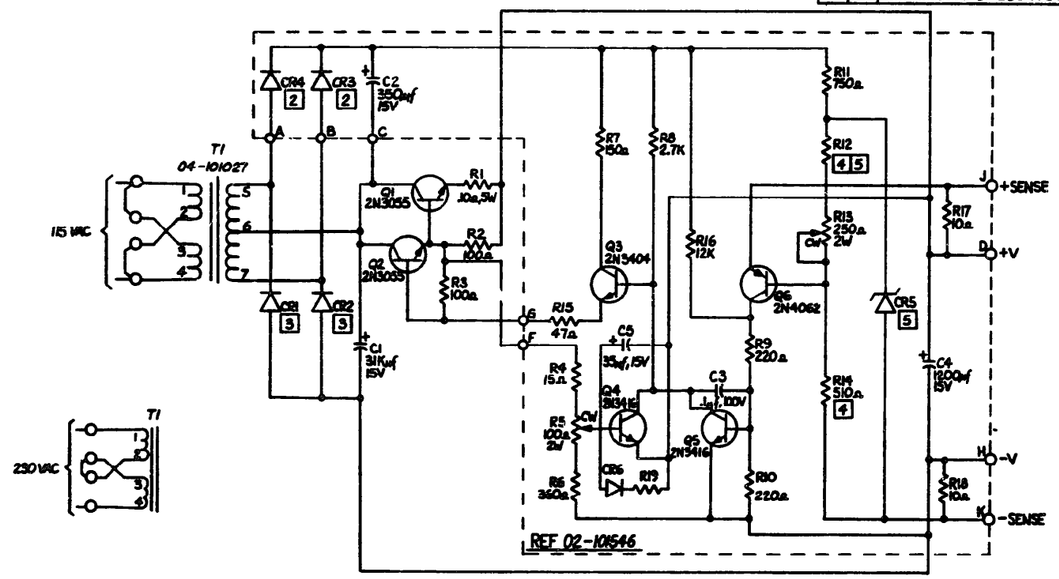
STANDARD POWER, INC.
SANTA ANA, CALIFORNIA

TITLE
SCHEMATIC-POWER SUPPLY
MODEL EPS60-M282

CODE IDENT	SIZE	DWG. NO.	REV.
	C	101701	D

SCALE — WEIGHT — SHEET 1 OF 1

REVISIONS				
REV.	BY	DESCRIPTION	APPD	DATE
A		RELEASE FOR PRODUCTION		
B		INC ECO 10013		
C		INCORPORATED ECO 10066		
D		INCORPORATED ECO 10086		
E		INCORPORATED ECO 10428		
F		INCORPORATED ECO 11328		
G		INCORPORATED ECO 11331		



[5] SELECT: CRS IN4735A, 5.9-6.09V; R12, 82Ω
6.1-6.29V; R12, 100Ω
6.3-6.49V; R12, 120Ω

[4] RESISTOR, ±2%, 1/2W, METAL FILM.

[3] I.R. PART NO. 20F10.

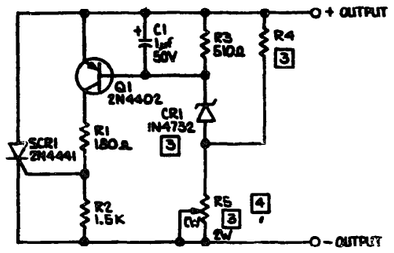
[2] PART NO. IN5391.

1. RESISTORS, ±5%, 1/2W CARBON

NOTES: UNLESS OTHERWISE SPECIFIED.

STANDARD POWER, INC. SANTA ANA, CALIFORNIA			
TITLE: SCHEMATIC- POWER SUPPLY, REMOTE SENSE MODEL 60-5 6A			
CODE IDENT	SIZE	DWG NO.	REV.
	C	12-101550	G
SCALE: —	WEIGHT: —	SHEET	OF

REV.	E.A.	BY	DESCRIPTION	DATE
A			RELEASE FOR PRODUCTION	
B			REVISED	
C			REVISED	
D			R4 WAS 150Ω, R5 WAS 1K	
E			PROVIDED ALTERNATES FOR CR1 & R4	
F			INCORPORATED ECO 10202	
G			INCORPORATED ECO 10246	
H			INCORPORATED ECO 10246	
J			INCORPORATED ECO 10657	



4 ADJUSTABILITY RANGE: MIN 4.3V-5.5V
MAX 35.0V-39.9V

3

SELECT CHART						
CR1	R5	R4	R5	R4	R5	R4
3.70-3.99V	1K	120Ω	2K	220Ω	2.5K	270Ω
4.00-4.09V	↑	130Ω	↑	240Ω	↑	300Ω
4.10-4.39V		150Ω		270Ω		330Ω
4.40-4.59V	↓	180Ω	↓	330Ω	↓	430Ω
4.60-4.69V	1K	200Ω	2K	360Ω	2.5K	470Ω

2 REFERENCE ASSY DWG NO. 101014.
1 RESISTORS ARE IN OHMS ± 5% 1/2W.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY APPLICATION	USED ON
	OVP-1

STANDARD POWER, INC.
SANTA ANA, CALIFORNIA

TITLE
SCHEMATIC, OVP-1

CODE IDENT	SIZE	DWG NO.	REV.
12	C	101017.	J

SCALE: —— WEIGHT: —— SHEET 1 OF 1

GTE INFORMATION SYSTEMS

ENGINEERING ORDER

E.O. NO. 3862

PRODUCT AFFECTED: 104207, 104093

OPER: AN ECR NO: 3750 EO TYPE: REF. CHANGE

DATE 6-14-76 SHT 1 OF 2

E.O. DASH	H	S	D	DOCUMENT – PART NO.	REV. OLD	REV. NEW	TITLE	PER SHT	NEXT ASSEMBLY	DATE INCORP.
01			X	300352	A1	A2	Logic Dia-Disc Controller Interface	2	104095	

TO UPDATE MNEMONIC GLOSSARY.

ECP required!
D.P Ellis
5/27/76

* CHANGE PER SHEET 2.

COGNIZANT ENGINEER Wm Marcoe 6-15-76

COST ANALYSIS REFERENCE: 3750

EFFECT UPON		DESCRIPTION/EFFECTIVITY
FINISHED GOODS	IN FIELD ☐	N/A
	IN HOUSE ☐	
WORK IN PROCESS	IN TEST ☐	
	IN PROD. ☐	
PARTS IN STORES ☐		
PARTS ON ORDER ☐		
FIELD RETURNS ☐		
QUALITY CONTROL ☐		
VENDOR TOOLING ☐		N/A
DOCUMENTS ☒		AS NOTED *
MANUALS ☐		N/A

CCB CHAIRMAN DATE 5/27/76

SERVICE CO. DATE 5/27/76

ENGINEERING DATE

MANUFACTURING R L Burris DATE 5/27/76

QUALITY R Cebula DATE 5/27/76

RECORDED JB DATE 6/17/76

DRAWN S.B DATE 6-14-76

CHECKED JB DATE 6/15/76

RELEASED SC DATE 6/17/76

E.O. NO. 3862

FORM NO. 3029 REV. 1/74

GTE INFORMATION SYSTEMS

ENGINEERING ORDER
CONTINUATION SHEET

E.O. NO: 3862-A

PRODUCT AFFECTED: 104207, 104083

OPER: ALL ECR NO: 3750 ECO TYPE: TEC. CHANGE

DATE 6-19-76 SHT 2 OF

REVISE DOCUMENT 300352:

SHT. 3, MNEMONIC GLOSSARY:

CHANGE DA0-7/7A4,7B4,7C4/ DEVICE ADDRESS TO DA0-7/7A5,7B5,7C5/ DEVICE ADDRESS.

DELETE DA00-07/7A5,7B5,7C5/DEVICE ADDRESS.

CHANGE ENDIX TO ENIDX.

CHANGE IODO-7/8/ TO IODO-7/6,8/.

SHT. 4, CONNECTOR DATA:

CHANGE J3, PINS 5,7,9,11,13,15,17,19 FROM DA00-DA07; TO DA0-DA7:

CHANGE J3, PIN 49, FROM STB- TO STRØBE-.

SHT. 7, DEVICE ADDRESS DECODE:

CHANGE J3, PINS 5,7,9,11,13,15,17,19 FROM DA00-DA07; TO DA0-DA7:

CHANGE J3, PIN 49, FROM STB- TO STRØBE-.

FORM NO. 5025A Rev. 1/74

ENGINEERING ORDER

E.O. NO. 3590

PRODUCT AFFECTED: 104095

DATE 10-29-75 SHT 1 OF 2

ORIG: AN ECR NO: 3361 EO TYPE REL CHNG

O. SIGN	W	S	D	DOCUMENT – PART NO.	REV. OLD	REV. NEW	TITLE	PER SHT	NEXT ASSEMBLY	DATE INCORP.
			X	300352	A	A1	LOGIC D/A DISK CONTROLLER INT.	1	104095	

CLARIFY I.C. LABEL

* ADD "40 X 9 FIFO" TO SHT 11 I.C. 8L.

COGNIZANT ENGINEER R FUNG R. Fung 11/19/75 COST ANALYSIS REFERENCE:

EFFECT UPON		DESCRIPTION/EFFECTIVITY
FINISHED GOODS	IN FIELD ☐	N/A
	IN HOUSE ☐	N/A
WORK IN PROCESS	IN TEST ☐	N/A
	IN PROD. ☐	N/A
PARTS IN STORES	☐	N/A
PARTS ON ORDER	☐	N/A
FIELD RETURNS	☐	N/A
QUALITY CONTROL	☐	N/A
VENDOR TOOLING	☐	N/A
DOCUMENTS	☐	AS NOTED *
MANUALS	☐	N/A

BOARD CHAIRMAN DATE

SERVICE CO. DATE

ENGINEERING DATE Robert Monroe 11-25-5

MANUFACTURING DATE

QUALITY DATE

RECORDED DAT DATE 11-4-75

DRAWN RM DATE 10-29-75

CHECKED DAJ DATE 11/4/75

RELEASED S.B DATE 11/24/75

E.O. NO. 3590

FORM NO. 5028 REV. 1/74

GE INFORMATION SYSTEMS

ENGINEERING ORDER
CONTINUATION SHEET

E.O. NO: 3590

PRODUCT AFFECTED 104093

DATE 10-29-75 SHT 2 OF

OPER: AN ECR NO: 3761 EO TYPE REC CHNG

DOCUMENT CHANGE

300352

SHEET 11
ADD NOMENCLATURE SECTION B.2 I.C. 8L
" 40 x 9 FIFØ "

FORM NO. 3023A Rev. 1/74

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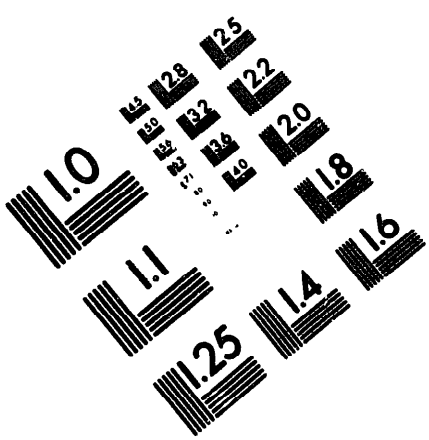

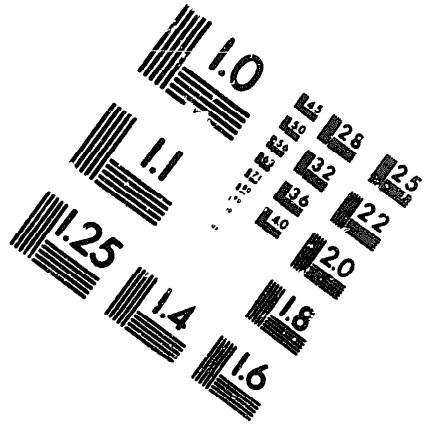

150 MM

10 mm (e= 81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

15 mm (e= 1 09 mm)

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abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

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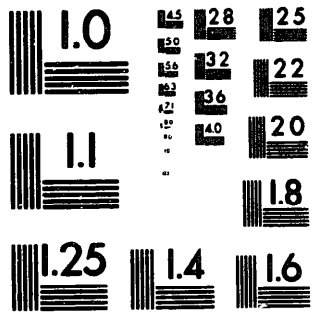
1234567890$¢£/%#½¼¾—=+×&@*



10 mm (e= 81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

15 mm (e= 1 09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1 37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

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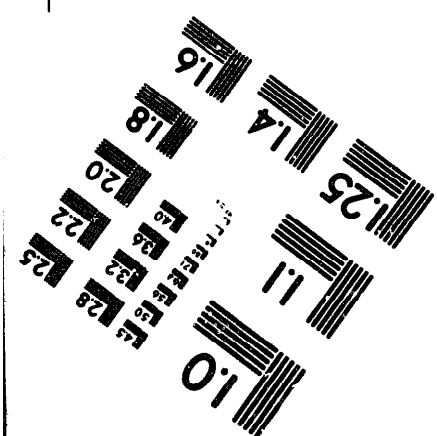
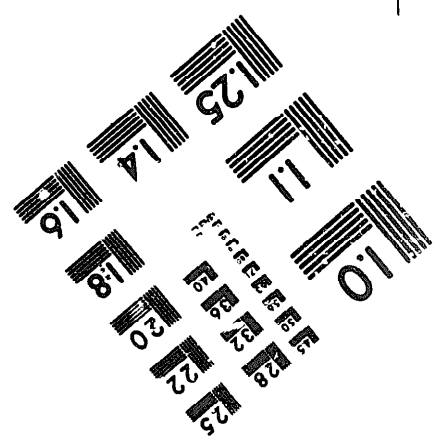
200 MM





250 MM